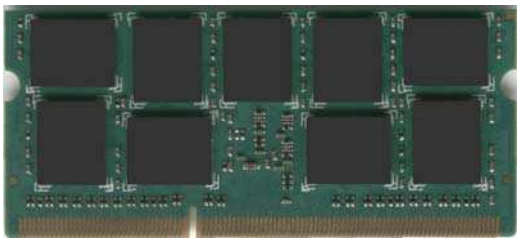
DTM64614A

8GB – 1Gx72, 204-pin ECC, DDR3 Unbuffered SO-DIMM



Identification

DTM64614A 1Gx72

8GB 2Rx8 EP3L-12800U-11-11-D0

Performance range

Clock / Module Speed / CL-t_{RCD} -t_{RP}
800 MHz / PC3-12800 / 11-11-11
667 MHz / PC3-10600 / 10-10-10
667 MHz / PC3-10600 / 9-9-9
533 MHz / PC3-8500 / 8-8-8
533 MHz / PC3-8500 / 7-7-7
400 MHz / PC3-6400 / 6-6-6

Features

- 204-pin SO-DIMM. Dual-sided assembly 67.60 mm [2.661"] wide by 30.0 mm [1.181"] high
- Operating Voltage: VDD = VDDQ = +1.35V (1.283V to 1.45V)
- Backward-compatible to VDD = VDDQ = +1.5V ±0.075V
- I/O Type: SSTL_15
- On-board I^2C temperature sensor with integrated Serial Presence-Detect (SPD) EEPROM
- Data Transfer Rate: 12.8 Gigabytes/sec
- Data Bursts: 8 and burst chop 4 mode
- ZQ Calibration for Output Driver and On-Die Termination (ODT)
- Programmable ODT / Dynamic ODT during Writes
- Programmable CAS Latency: 6, 7, 8, 9, 10 and 11
- Bi-directional Differential Data Strobe signals
- SDRAM Addressing (Row/Col/Bank): 16/10/3
- Fully RoHS Compliant

Description

DTM64614A is an Unbuffered DDR3 1Gx72 memory module with ECC bits. The assembly is comprised of two Ranks. Each Rank is comprised of nine 512Mx8 DDR3 Hynix SDRAMs. One 2K-bit EEPROM with thermal sensor is used for Serial Presence Detect.

A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals.

The assembly is a Small Outline Dual In-line Memory Module intended for mounting into 204-pin edge connector sockets.

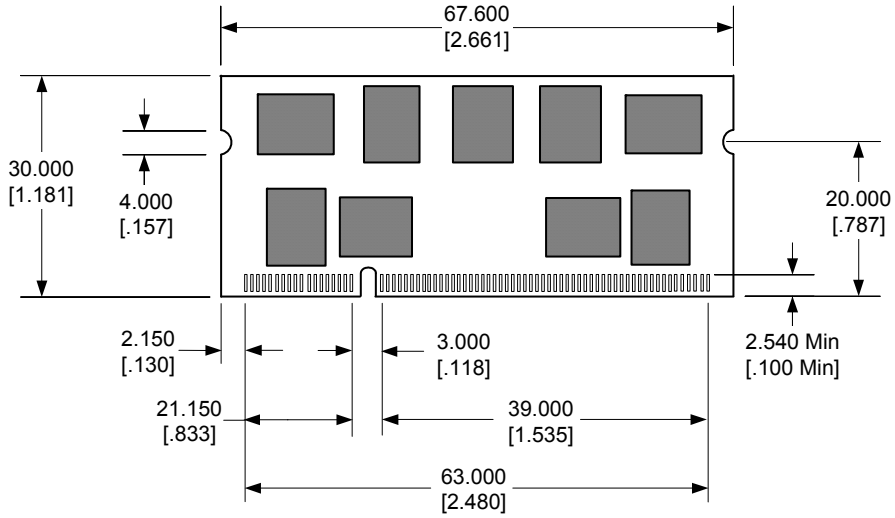
Pin Configuration

Front Side				Back Side			
1 V_{REFDQ}	53 V_{SS}	103 A3	155 V_{SS}	2 V_{SS}	54 DQ28	104 A4	156 DQS5
3 V_{SS}	55 DQ24	105 A1	157 DM5	4 DQ4	56 DQ29	106 A2	158 V_{SS}
5 DQ0	57 DQ25	107 A0	159 DQ42	6 DQ5	58 V_{SS}	108 BA1	160 DQ46
7 DQ1	59 DM3	109 V_{DD}	161 DQ43	8 V_{SS}	60 /DQS3	110 V_{DD}	162 DQ47
9 V_{SS}	61 V_{SS}	111 CK0	163 V_{SS}	10 /DQS0	62 DQS3	112 CK1	164 V_{SS}
11 DM0	63 DQ26	113 /CK0	165 DQ48	12 DQS0	64 V_{SS}	114 /CK1	166 DQ52
13 DQ2	65 DQ27	115 V_{DD}	167 DQ49	14 V_{SS}	66 DQ30	116 V_{DD}	168 DQ53
15 DQ3	67 V_{SS}	117 A10/AP	169 V_{SS}	16 DQ6	68 DQ31	118 /CS3/NC	170 V_{SS}
17 V_{SS}	69 CB0	119 BA0	171 /DQS6	18 DQ7	70 V_{SS}	120 /CS2/NC	172 DM6
19 DQ8	71 CB1	121 /WE	173 DQS6	20 V_{SS}	72 CB4	122 /RAS	174 DQ54
21 DQ9	73 V_{SS}	123 V_{DD}	175 V_{SS}	22 DQ12	74 CB5	124 V_{DD}	176 DQ55
23 V_{SS}	75 /DQS8	125 /CAS	177 DQ50	24 DQ13	76 DM8	126 ODT0	178 V_{SS}
25 /DQS1	77 DQS8	127 /CS0	179 DQ51	26 V_{SS}	78 V_{SS}	128 ODT1	180 DQ60
27 DQS1	79 V_{SS}	129 /CS1	181 V_{SS}	28 DM1	80 CB6	130 A13	182 DQ61
29 V_{SS}	81 CB2	131 V_{DD}	183 DQ56	30 /RESET	82 CB7	132 V_{DD}	184 V_{SS}
31 DQ10	83 CB3	133 DQ32	185 DQ57	32 V_{SS}	84 V_{REFCA}	134 DQ36	186 /DQS7
33 DQ11	85 V_{DD}	135 DQ33	187 V_{SS}	34 DQ14	86 V_{DD}	136 DQ37	188 DQS7
35 V_{SS}	87 CKE0	137 V_{SS}	189 DM7	36 DQ15	88 A15	138 V_{SS}	190 V_{SS}
37 DQ16	89 CKE1	139 /DQS4	191 DQ58	38 V_{SS}	90 A14	140 DM4	192 DQ62
39 DQ17	91 BA2	141 DQS4	193 DQ59	40 DQ20	92 A9	142 DQ38	194 DQ63
41 V_{SS}	93 V_{DD}	143 V_{SS}	195 V_{SS}	42 DQ21	94 V_{DD}	144 DQ39	196 V_{SS}
43 /DQS2	95 A12/ /BC	145 DQ34	197 SA0	44 DM2	96 A11	146 V_{SS}	198 /EVENT
45 DQS2	97 A8	147 DQ35	199 V_{DDSPD}	46 V_{SS}	98 A7	148 DQ44	200 SDA
47 V_{SS}	99 A5	149 V_{SS}	201 SA1	48 DQ22	100 A6	150 DQ45	202 SCL
49 DQ18	101 V_{DD}	151 DQ40	203 V_{TT}	50 DQ23	102 V_{DD}	152 V_{SS}	204 V_{TT}
51 DQ19	A7	153 DQ41		52 V_{SS}		154 /DQS5	

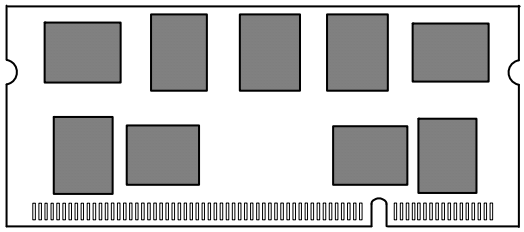
Pin Description

Name	Function
CB[7:0]	Data Check Bits
DQ[63:0]	Data Bits
DQS[8:0], /DQS[8:0]	Differential Data Strobes
DM[8:0]	Data Mask
CK[1:0], /CK[1:0]	Differential Clock Inputs
CKE[1:0]	Clock Enables
/CAS	Column Address Strobe
/RAS	Row Address Strobe
/CS[3:0]	Chip Selects
/WE	Write Enable
A[14:0]	Address Inputs
BA[2:0]	Bank Addresses
A12/BC	Combination input: Addr12/Burst Chop
A10/AP	Combination input: Addr10/Auto-precharge
ODT[1:0]	On Die Termination Inputs
SA[1:0]	SPD Address
SCL	SPD Clock Input
SDA	SPD Data Input/Output
/EVENT	Temperature Sensing
V_{SS}	Ground
V_{DD}	Power
V_{DDSPD}	SPD EEPROM Power
V_{REFDQ}	Reference Voltage for DQ
V_{REFCA}	Reference Voltage for CA
V_{TT}	Termination Voltage
NC	No Connection

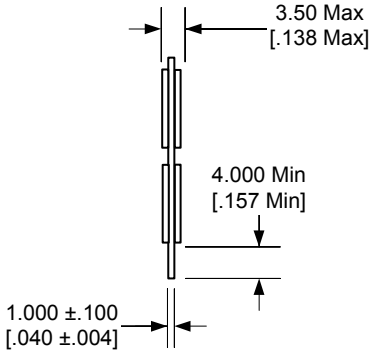
Front view



Back view



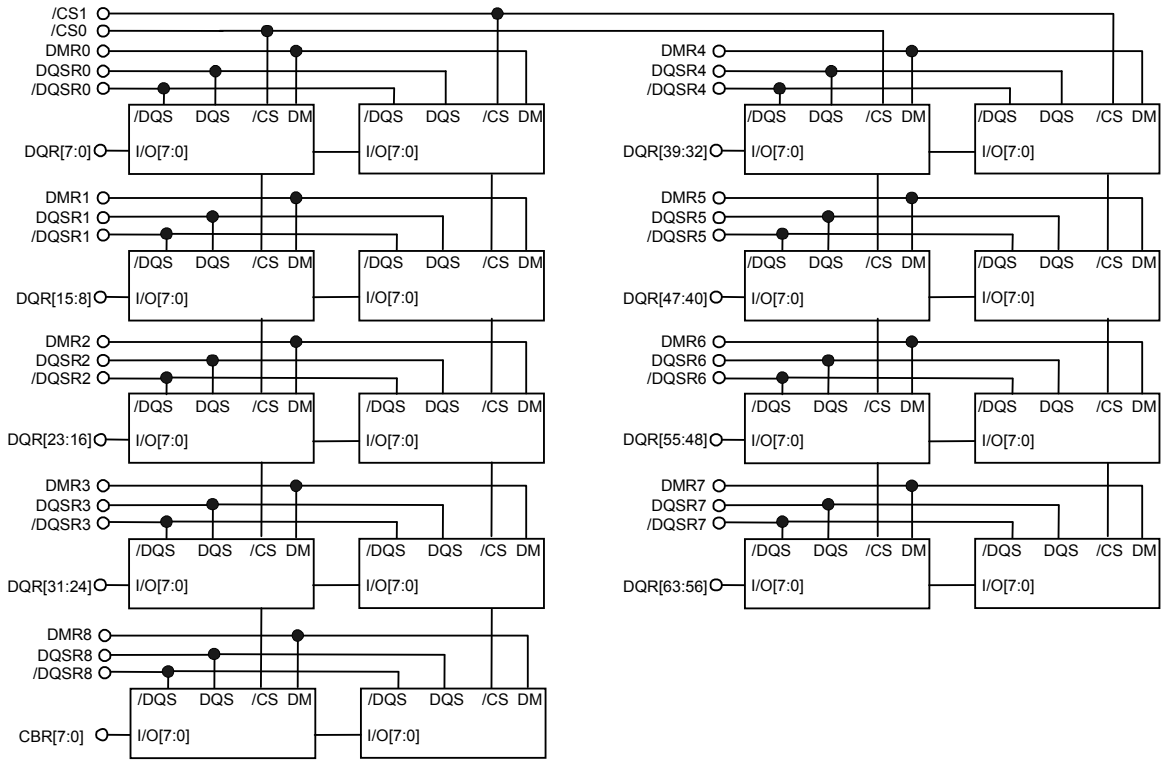
Side view

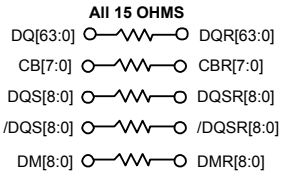


Notes

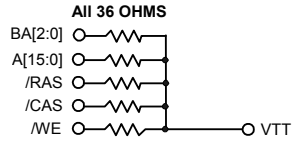
Tolerances on all dimensions except where otherwise indicated are ±.13 (.005).

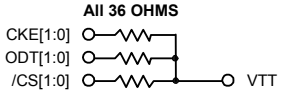
All dimensions are expressed: millimeters [inches]

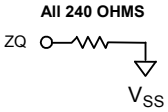


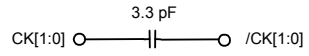


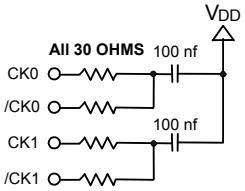
GLOBAL SDRAM CONNECTS

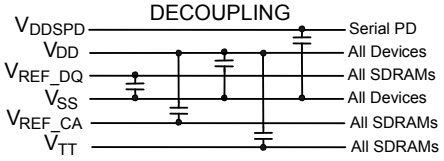


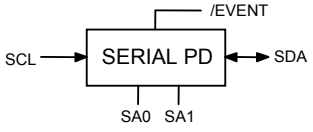












Absolute Maximum Ratings
(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	$T_{STORAGE}$	-55	100	C
Module Ambient Temperature, Operating	T_A	0	85	C
DRAM Case Temperature, Operating	T_{CASE}	0	95	C
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.4	1.975	V
Voltage on Any Pin relative to V_{SS}	V_{IN},V_{OUT}	-0.4	1.975	V

Notes:
DRAM Operating Case Temperature above 85C requires 2X refresh.

Recommended DC Operating Conditions (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Operation Voltage	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V_{DD}	1.35V	1.283	1.35	1.4500	V	
		1.5V	1.425	1.5	1.575		
I/O Reference Voltage	V_{REFDQ}	1.35V	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1
		1.5V					
I/O Reference Voltage	V_{REFCA}	1.35V	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1
		1.5V					

Notes:
The value of V_{REF} is expected to equal one-half V_{DD} and to track variations in the V_{DD} DC level. Peak-to-peak noise on V_{REF} may not exceed ±1% of its DC value. For Reference V_{DD}/2 ± 15 mV.

DC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Operation Voltage	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(DC)}$	1.35V	V_{REF} + 0.09	V_{DD}	V
		1.5V	V_{REF} + 0.1	V_{DD}	
Logical Low (Logic 0)	$V_{IL(DC)}$	1.35V	V_{SS}	V_{REF} - 0.09	V
		1.5V	V_{SS}	V_{REF} - 0.1	

AC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Operation Voltage	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(AC)}$	1.35V	V_{REF} + 0.160	-	V
		1.5V	V_{REF} + 0.175	-	
Logical Low (Logic 0)	$V_{IL(AC)}$	1.35V	-	V_{REF} - 0.160	V
		1.5V	-	V_{REF} - 0.175	

Differential Input Logic Levels (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Differential Input Logic High	$V_{IH.DIFF}$	+0.200	Note 2	V	
Differential Input Logic Low	$V_{IL.DIFF}$	Note 2	-0.200	V	
Differential Input Cross Point Voltage relative to VDD/2	V_{IX}	- 0.150	+ 0.150	V	1

Notes:
1) The relation between Vix Min/Max and VSEL/VSEH should satisfy following.
(VDD/2) + Vix (Min) - VSEL ≥ 25mV
VSEH - ((VDD/2) + Vix (Max)) ≥ 25mV
2) These values are not defined; however, the single-ended signals CK, CK#, DQS, DQS# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Capacitance (T_A = 25 C, f = 100 MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK0, /CK0, CK1, /CK1	C_{CK}	10.5	15.9	pF
Input Capacitance, Address	BA[2:0], A[15:0], /RAS, /CAS, /WE	C_I	13.5	23.4	pF
Input Capacitance Control	/CS0, /CS1, CKE0, CKE1, ODT0, ODT1	C_I	6.75	11.7	pF
Input/Output Capacitance	DQ[63:0], CB[7:0] DQS[8:0], /DQS[8:0], DM[8:0]	C_{IO}	3	5	pF

DC Characteristics (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input 0 V < VIN < VDD)	I_{IL}	-18	+18	µA	1,2
Output Leakage Current (0V < VOUT < VDDQ)	I_{OL}	-10	+10	µA	2,3

Notes:
1) All other pins not under test = 0 V
2) Values are shown per pin
3) DQ's, DQS, DQS and ODT are disabled

I_{DD} Specifications and Conditions (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Test Condition	Max Value	Unit
Operating One Bank Active-Precharge Current	$I_{DD}0$*	Operating current : One bank ACTIVATE-to-PRECHARGE	369	mA
Operating One Bank Active-Read-Precharge Current	$I_{DD}1$*	Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE	432	mA
Precharge Power-Down Current	$I_{DD}2P$**	Precharge power down current: (Slow exit)	144	mA
Precharge Power-Down Current	$I_{DD}2P$**	Precharge power down current: (Fast exit)	216	mA
Precharge Quiet Standby Current	$I_{DD}2Q$**	Precharge quiet standby current	306	mA
Precharge Standby Current	$I_{DD}2N$**	Precharge standby current	306	mA
Active Power-Down Current	$I_{DD}3P$**	Active power-down current	324	mA
Active Standby Current	$I_{DD}3N$**	Active standby current	468	mA
Operating Burst Write Current	$I_{DD}4W$*	Burst write operating current	882	mA
Operating Burst Read Current	$I_{DD}4R$*	Burst read operating current	837	mA
Burst Refresh Current	$I_{DD}5$**	Refresh current	3600	mA
Self Refresh Current	$I_{DD}6$**	Self-refresh temperature current: MAX Tc = 85°C	216	mA
Operating Bank Interleave Read Current	$I_{DD}7$*	All bank interleaved read current	1287	mA

* One module rank in this operation rest in IDD2P slow exit.
** All module ranks in this operation.

AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	t_{AA}	13.125	20	ns
CAS-to-CAS Command Delay	t_{CCD}	4	-	t_{CK}
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	t_{CK}
Clock Cycle Time	t_{CK}	1.25	3.3	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	t_{CK}
Data Input Hold Time after DQS Strobe	t_{DH}	45	-	ps
DQ Input Pulse Width	t_{DIPW}	360	-	ps
DQS Output Access Time from Clock	t_{DQSCK}	-225	+225	ps
Write DQS High Level Width	t_{DQSH}	0.45	0.55	$t_{CK(avg)}$
Write DQS Low Level Width	t_{DQSL}	0.45	0.55	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	t_{DQSQ}	-	120	ps
Data Input Setup Time Before DQS Strobe	t_{DS}	10	-	ps
DQS Falling Edge from Clock, Hold Time	t_{DSH}	0.18	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	t_{DSS}	0.18	-	$t_{CK(avg)}$
Address and Command Hold Time after Clock	t_{IH}	120	-	ps
Address and Command Setup Time before Clock	t_{IS}	45	-	ps
Load Mode Command Cycle Time	t_{MRD}	4	-	t_{CK}
DQ-to-DQS Hold	t_{QH}	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	t_{RAS}	35	$9*t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	t_{RC}	48.125	-	ns
RAS-to-CAS Delay	t_{RCD}	13.125	-	ns
Average Periodic Refresh Interval (0 C ≤ T_{CASE} ≤ 85 C)	t_{REFI}	-	7.8	µs
Average Periodic Refresh Interval (85 C < T_{CASE} ≤ 95 C)			3.9	
Auto Refresh Row Cycle Time	t_{RFC}	260	-	ns
Row Precharge Time	t_{RP}	13.125	-	ns
Read DQS Preamble Time	t_{RPRE}	0.9	Note-1	$t_{CK(avg)}$
Read DQS Postamble Time	t_{RPST}	0.3	Note-2	$t_{CK(avg)}$
Row Active to Row Active Delay	t_{RRD}	Max(4nCK, 6ns)	-	ns
Internal Read to Precharge Command Delay	t_{RTP}	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	t_{WPRE}	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	t_{WPST}	0.3	-	$t_{CK(avg)}$
Write Recovery Time	t_{WR}	15	-	ns
Internal Write to Read Command Delay	t_{WTR}	Max(4nCK, 7.5ns)	-	ns

Notes:
1. The maximum preamble is bound by tLZDQS(min)
2. The maximum postamble is bound by tHZDQS(max)

SERIAL PRESENCE DETECT MATRIX

Byte#	Function.	Value	Hex
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage.		0x92
	Bit 3 ~ Bit 0. SPD Bytes Used -	176	
	Bit 6 ~ Bit 4. SPD Bytes Total -	256	
	Bit 7. CRC Coverage -	Bytes 0-116	
1	SPD Revision.	Rev. 1.1	0x11
2	Key Byte / DRAM Device Type.	DDR3 SDRAM	0x0B
3	Key Byte / Module Type.		0x08
	Bit 3 ~ Bit 0. Module Type -	72b-SO-UDIMM	
	Bit 7 ~ Bit 4. Reserved -	0	
4	SDRAM Density and Banks.		0x04
	Bit 3 ~ Bit 0. Total SDRAM capacity, in megabits -	4Gb	
	Bit 6 ~ Bit 4. Bank Address Bits -	8 banks	
	Bit 7. Reserved -	0	
5	SDRAM Addressing.		0x21
	Bit 2 ~ Bit 0. Column Address Bits -	10	
	Bit 5 ~ Bit 3. Row Address Bits -	16	
	Bit 7, 6. Reserved	0	
6	Module Nominal Voltage, VDD.		0x02
	Bit 0. NOT 1.5 V operable -		
	Bit 1. 1.35 V operable -	X	
	Bit 2. 1.2X V operable -		
	Bit 3. Reserved -		
	Bit 4. Reserved -		
	Bit 5. Reserved -		
	Bit 6. Reserved -		
	Bit 7. Reserved -		
7	Module Organization.		0x09
	Bit 2 ~ Bit 0. SDRAM Device Width -	8-Bits	
	Bit 5 ~ Bit 3. Number of Ranks -	2-Rank	
	Bit 7, 6. Reserved	0	
8	Module Memory Bus Width.		0x0B
	Bit 2 ~ Bit 0. Primary bus width, in bits -	64-Bits	
	Bit 4, Bit 3. Bus width extension, in bits -	8-Bits	
	Bit 7 ~ Bit 5. Reserved -	0	
9	Fine Timebase (FTB) Dividend / Divisor.		0x52
	Bit 3 ~ Bit 0. Fine Timebase (FTB) Divisor	2	
	Bit 7 ~ Bit 4. Fine Timebase (FTB) Dividend	5	
10	Medium Timebase (MTB) Dividend.	1 (MTB = 0.125ns)	0x01

11	Medium Timebase (MTB) Divisor.	8 (MTB = 0.125ns)	0x08
12	SDRAM Minimum Cycle Time (tCKmin).	1.25ns	0x0A
13	Reserved.	UNUSED	0x00
14	CAS Latencies Supported, Least Significant Byte.		0xFC
	Bit 0. CL = 4 -		
	Bit 1. CL = 5 -		
	Bit 2. CL = 6 -	X	
	Bit 3. CL = 7 -	X	
	Bit 4. CL = 8 -	X	
	Bit 5. CL = 9 -	X	
	Bit 6. CL = 10 -	X	
	Bit 7. CL = 11 -	X	
15	CAS Latencies Supported, Most Significant Byte.		0x00
	Bit 0. CL = 12 -		
	Bit 1. CL = 13 -		
	Bit 2. CL =14 -		
	Bit 3. CL = 15 -		
	Bit 4. CL = 16 -		
	Bit 5. CL = 17 -		
	Bit 6. CL = 18 -		
	Bit 7. Reserved.		
16	Minimum CAS Latency Time (tAAmin).	13.125ns	0x69
17	Minimum Write Recovery Time (tWRmin).	15.0ns	0x78
18	Minimum RAS# to CAS# Delay Time (tRCDmin).	13.125ns	0x69
19	Minimum Row Active to Row Active Delay Time (tRRDmin).	6.0ns	0x30
20	Minimum Row Precharge Delay Time (tRPmin).	13.125ns	0x69
21	Upper Nibbles for tRAS and tRC.		0x11
	Bit 3 ~ Bit 0. tRAS Most Significant Nibble -	1	
	Bit 7 ~ Bit 4. tRC Most Significant Nibble -	1	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte.	35.0ns	0x18
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte.	48.125ns	0x81
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte.	260.0ns	0x20
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte.	260.0ns	0x08
26	Minimum Internal Write to Read Command Delay Time (tWTRmin).	7.5ns	0x3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin).	7.5ns	0x3C
28	Upper Nibble for tFAW.		0x00
	Bit 3 ~ Bit 0. tFAW Most Significant Nibble -	0	
	Bit 7 ~ Bit 4. Reserved -	0	

29	Minimum Four Activate Window Delay Time (tFAWmin), Least Significant Byte.	30.0ns	0xF0
30	SDRAM Optional Features.		0x83
	Bit 0. RZQ / 6 -	X	
	Bit 1. RZQ / 7 -	X	
	Bit 2. Reserved -		
	Bit 3. Reserved -		
	Bit 4. Reserved -		
	Bit 5. Reserved -		
	Bit 6. Reserved -		
	Bit 7. DLL-Off Mode Support -	X	
31	SDRAM Drivers Supported.		0x05
	Extended Temperature Range -	X	
	Extended Temperature Refresh Rate -		
	Auto Self Refresh (ASR) -	X	
	On-die Thermal Sensor (ODTS) Readout -		
	Reserved -		
	Reserved -		
	Reserved -		
	Partial Array Self Refresh (PASR) -		
32	Module Thermal Sensor.		0x80
	Bit 6 ~ Bit 0. Thermal Sensor Accuracy -	0	
	Bit 7. Thermal Sensor -	With TS	
33	SDRAM Device Type.		0x00
	Bit 1 ~ Bit 0. Signal Loading -	Not specified	
	Bit 3 ~ Bit 2. Reserved. 0-Undefined -	0	
	Bit 6 ~ Bit 4. Die Count. -	Not specified	
	Bit 7. SDRAM Device Type -	Std Mono	
34	Fine Offset for SDRAM Minimum Cycle Time (tCKmin) -	UNUSED	0x00
35	Fine Offset for Minimum CAS Latency Time (tAAmin) -	UNUSED	0x00
36	Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin) -	UNUSED	0x00
37	Minimum Row Precharge Delay Time (tRPmin) -	UNUSED	0x00
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin) -	UNUSED	0x00
39-59	Reserved	UNUSED	0x00
60	Module Nominal Height.		0x0F
	Bit 4 ~ Bit 0. Module Nominal Height max, in mm -	29<h<=30	
	Bit 7 ~ Bit5. Reserved -	0	
61	Module Maximum Thickness.		0x11
	Bit 3 ~ Bit 0. Front, in mm (baseline thickness = 1 mm) -	1<th<=2	
	Bit 7 ~ Bit 4. Back, in mm (baseline thickness = 1 mm) -	1<th<=2	
62	Reference Raw Card Used.		0x03

	Bit 4 ~ Bit 0. Reference Raw Card -	R/C D	
	Bit 6, Bit 5. Reference Raw Card Revision -	Rev.0	
	Bit 7. Reserved -	A-AL	
63	Address Mapping from Edge Connector to DRAM.		0x00
	Bit 0. Rank 1 Mapping (Registered DIMM - Reserved) -	Standard	
	Bit 7 ~ Bit 1. Reserved -	0	
64-116	Module-Specific Section	UNUSED	0x00
117	Module Manufacturer ID Code, Least Significant Byte	DATARAM	0x01
118	Module Manufacturer ID Code, Most Significant Byte	DATARAM	0x91
119	Module Manufacturing Location		0x00
120,121	Module Manufacturing Date		0x00
122-125	Module Serial Number		0x23
126	Cyclical Redundancy Code (CRC).	CRC	0x1D
127	Cyclical Redundancy Code (CRC).	CRC	0xD6
128-131	Module Part Number		0x20
132	Module Part Number	D	0x44
133	Module Part Number	A	0x41
134	Module Part Number	T	0x54
135	Module Part Number	A	0x41
136	Module Part Number	R	0x52
137	Module Part Number	A	0x41
138	Module Part Number	M	0x4D
139	Module Part Number		0x20
140	Module Part Number	6	0x36
141	Module Part Number	4	0x34
142	Module Part Number	6	0x36
143	Module Part Number	1	0x31
144	Module Part Number	4	0x34
145	Module Part Number		0x20
146,147	Module Revision Code	UNUSED	0x00
148	DRAM Manufacturer ID Code, Least Significant Byte	Not recognized	0x00
149	DRAM Manufacturer ID Code, Most Significant Byte	Not recognized	0x00
150-175	Manufacturer's Specific Data	UNUSED	0x00
176-255	Open for customer use	UNUSED	0x00

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