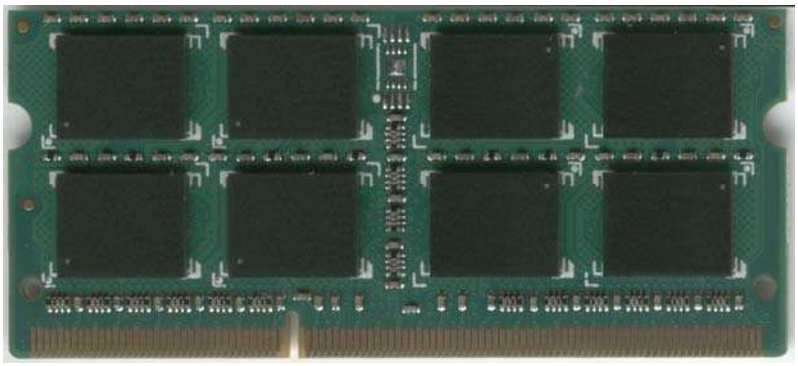
DTM64610C

8GB – 204-pin 2Rx8 Unbuffered Non-ECC DDR3 SODIMM



Identification

DTM64610C 1Gx64

8GB 2Rx8 PC3-12800S-11-11-F3

Performance range

Clock / Module Speed / CL-t_{RCD} -t_{RP}
800 MHz / DDR3-1600 / 11-11-11
667 MHz / DDR3-1333 / 10-10-10
667 MHz / DDR3-1333 / 9-9-9
533 MHz / DDR3-1066 / 8-8-8
533 MHz / DDR3-1066 / 7-7-7
400 MHz / DDR3-800 / 6-6-6
333 MHz / DDR3-667 / 5-5-5

Features

- 204-pin SO-DIMM. Dual-sided assembly 67.60 mm [2.661”] wide by 30.0 mm [1.181”] high
- Operating Voltage: 1.5 V ±0.075 V
- I/O Type: SSTL_15
- Data Transfer Rate: 12.8 Gigabytes/sec
- Data Bursts: 8 and burst chop 4 mode
- ZQ Calibration for Output Driver and On-Die Termination (ODT)
- Programmable ODT / Dynamic ODT during Writes
- Programmable CAS Latency: 5, 6, 7, 8, 9, 10, and 11
- Differential Data Strobe signals
- SDRAM Addressing (Row/Col/Bank): 16/10/3
- Fully RoHS Compliant

Description

DTM64610C is a non-ECC Unbuffered 1Gx64 memory module which conforms to JEDEC’s PC3-12800 standard. The assembly is Dual-Rank. Each Rank is comprised of eight Hynix 512Mx8 DDR3 SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals.

The assembly is a Small Outline Dual In-line Memory Module intended for mounting into 204-pin edge connector sockets.

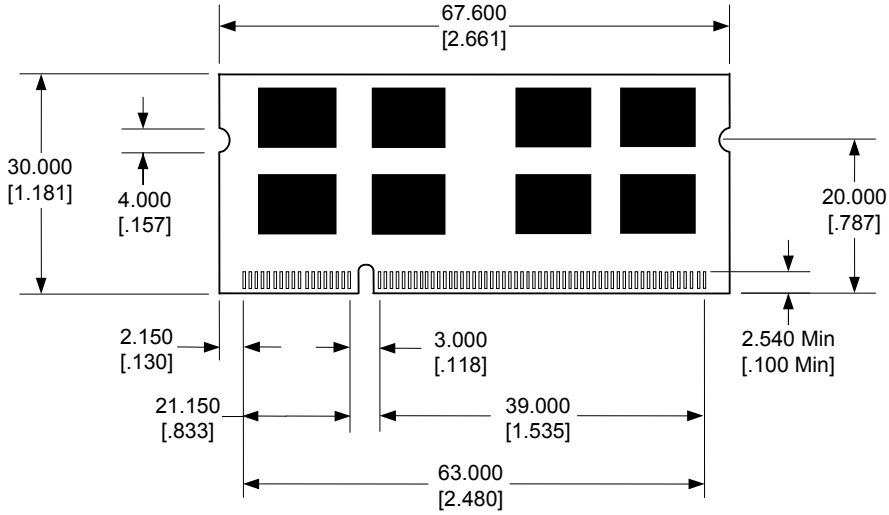
Pin Configuration

Front Side				Back Side			
1 V_{REFDQ}	53 DQ19	105 V_{DD}	157 DQ42	2 V_{SS}	54 V_{SS}	106 V_{DD}	158 DQ46
3 V_{SS}	55 V_{SS}	107 A10/AP	159 DQ43	4 DQ4	56 DQ28	108 BA1	160 DQ47
5 DQ0	57 DQ24	109 BA0	161 V_{SS}	6 DQ5	58 DQ29	110 /RAS	162 V_{SS}
7 DQ1	59 DQ25	111 V_{DD}	163 DQ48	8 V_{SS}	60 V_{SS}	112 V_{DD}	164 DQ52
9 V_{SS}	61 V_{SS}	113 /WE	165 DQ49	10 /DQS0	62 /DQS3	114 /S0	166 DQ53
11 DM0	63 DM3	115 /CAS	167 V_{SS}	12 DQS0	64 DQS3	116 ODT0	168 V_{SS}
13 V_{SS}	65 V_{SS}	117 V_{DD}	169 /DQS6	14 V_{SS}	66 V_{SS}	118 V_{DD}	170 DM6
15 DQ2	67 DQ26	119 A13	171 DQS6	16 DQ6	68 DQ30	120 ODT1	172 V_{SS}
17 DQ3	69 DQ27	121 /S1	173 V_{SS}	18 DQ7	70 DQ31	122 NC	174 DQ54
19 V_{SS}	71 V_{SS}	123 V_{DD}	175 DQ50	20 V_{SS}	72 V_{SS}	124 V_{DD}	176 DQ55
21 DQ8	73 CKE0	125 NC/TEST	177 DQ51	22 DQ12	74 CKE1	126 V_{REFCA}	178 V_{SS}
23 DQ9	75 V_{DD}	127 V_{SS}	179 V_{SS}	24 DQ13	76 V_{DD}	128 V_{SS}	180 DQ60
25 V_{SS}	77 NC	129 DQ32	181 DQ56	26 V_{SS}	78 A15	130 DQ36	182 DQ61
27 /DQS1	79 BA2	131 DQ33	183 DQ57	28 DM1	80 A14	132 DQ37	184 V_{SS}
29 DQS1	81 V_{DD}	133 V_{SS}	185 V_{SS}	30 /RESET	82 V_{DD}	134 V_{SS}	186 /DQS7
31 V_{SS}	83 A12/BC	135 /DQS4	187 DM7	32 V_{SS}	84 A11	136 DM4	188 DQS7
33 DQ10	85 A9	137 DQS4	189 V_{SS}	34 DQ14	86 A7	138 V_{SS}	190 V_{SS}
35 DQ11	87 V_{DD}	139 V_{SS}	191 DQ58	36 DQ15	88 V_{DD}	140 DQ38	192 DQ62
37 V_{SS}	89 A8	141 DQ34	193 DQ59	38 V_{SS}	90 A6	142 DQ39	194 DQ63
39 DQ16	91 A5	143 DQ35	195 V_{SS}	40 DQ20	92 A4	144 V_{SS}	196 V_{SS}
41 DQ17	93 V_{DD}	145 V_{SS}	197 SA0	42 DQ21	94 V_{DD}	146 DQ44	198 NC
43 V_{SS}	95 A3	147 DQ40	199 V_{DDSPD}	44 V_{SS}	96 A2	148 DQ45	200 SDA
45 /DQS2	97 A1	149 DQ41	201 SA1	46 DM2	98 A0	150 V_{SS}	202 SCL
47 DQS2	99 V_{DD}	151 V_{SS}	203 V_{TT}	48 V_{SS}	100 V_{DD}	152 /DQS5	204 V_{TT}
49 V_{SS}	101 CK0	153 DM5		50 DQ22	102 CK1	154 DQS5	
51 DQ18	103 /CK0	155 V_{SS}		52 DQ23	104 /CK1	156 V_{SS}	

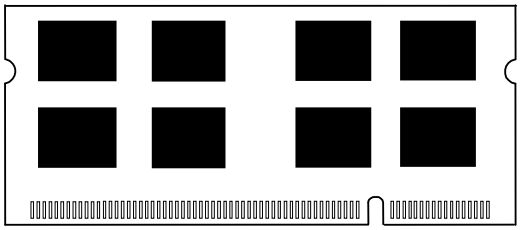
Pin Description

Name	Function
DQ[63:0]	Data Bits
DQS[7:0], /DQS[7:0]	Differential Data Strobes
DM[7:0]	Data Mask
CK[1:0], /CK[1:0]	Differential Clock Inputs
CKE[1:0]	Clock Enables
/CAS	Column Address Strobe
/RAS	Row Address Strobe
/S[1:0]	Chip Selects
/WE	Write Enable
A[15:0]	Address Inputs
BA[2:0]	Bank Addresses
ODT[1:0]	On Die Termination Inputs
SA[1:0]	SPD Address
SCL	SPD Clock Input
SDA	SPD Data Input/Output
TEST	Logic Analyzer specific
V_{SS}	Ground
V_{DD}	Power
V_{DDSPD}	SPD EEPROM Power
V_{REFDQ}	Reference Voltage for DQ
V_{REFCA}	Reference Voltage for CA
V_{TT}	Termination Voltage
NC	No Connection

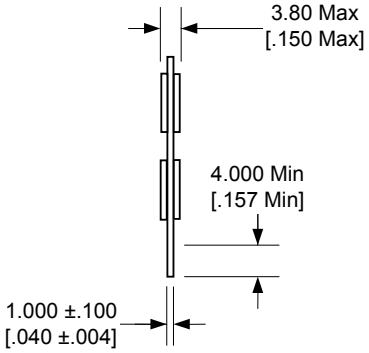
Front view



Back view



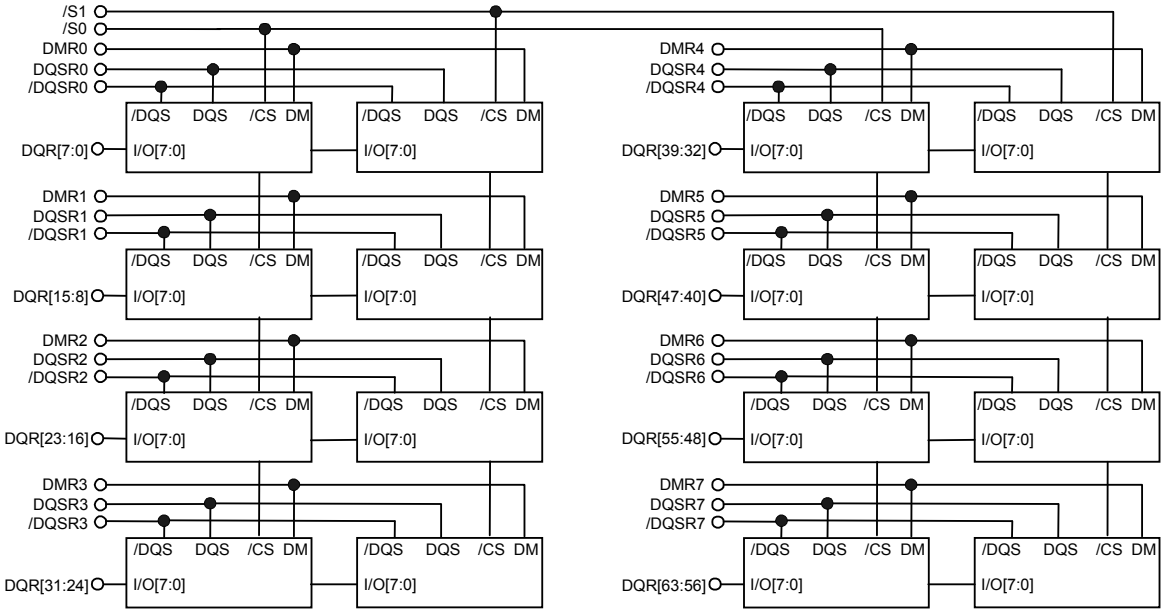
Side view

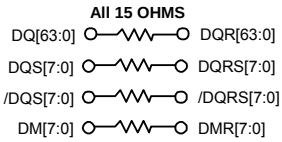


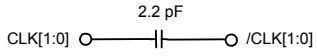
Notes

Tolerances on all dimensions except where otherwise indicated are ±.15 (.0059).

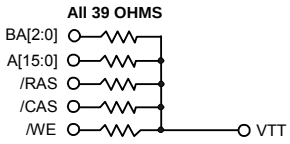
All dimensions are expressed: millimeters [inches]

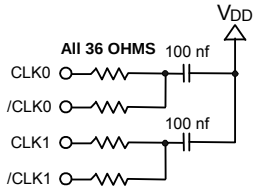


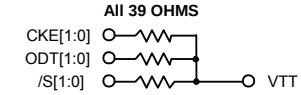


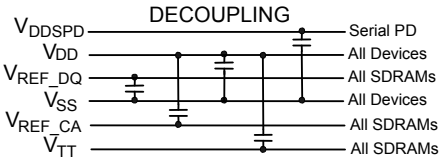


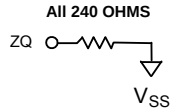
GLOBAL SDRAM CONNECTS

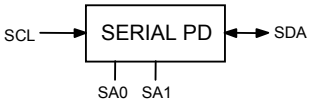












Absolute Maximum Ratings
(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	$T_{STORAGE}$	-55	100	C
Module Ambient Temperature, Operating	T_A	-40	95	C
DRAM Case Temperature, Operating	T_{CASE}	-40	95	C
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.4	1.975	V
Voltage on Any Pin relative to V_{SS}	V_{IN},V_{OUT}	-0.4	1.975	V

Notes:
DRAM Operating Case Temperature above 85C requires 2X refresh.

Recommended DC Operating Conditions (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V_{DD}	1.425	1.5	1.575	V	
I/O Reference Voltage	V_{REFDQ}	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1
I/O Reference Voltage	V_{REFCA}	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1

Notes:
The value of V_{REF} is expected to equal one-half V_{DD} and to track variations in the V_{DD} DC level. Peak-to-peak noise on V_{REF} may not exceed ±1% of its DC value. For Reference: $V_{DD}/2$ ± 15 mV.

DC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(DC)}$	V_{REF} + 0.1	V_{DD}	V
Logical Low (Logic 0)	$V_{IL(DC)}$	V_{SS}	V_{REF} - 0.1	V

AC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(AC)}$	V_{REF} + 0.175	-	V
Logical Low (Logic 0)	$V_{IL(AC)}$	-	V_{REF} - 0.175	V

Differential Input Logic Levels (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Differential Input Logic High	$V_{IH.DIFF}$	+0.200	DC:V_{DD} AC:V_{DD}+0.4	V
Differential Input Logic Low	$V_{IL.DIFF}$	DC:V_{SS} AC:V_{SS}-0.4	-0.200	V
Differential Input Cross Point Voltage relative to VDD/2	V_{IX}	- 0.150	+ 0.150	V

Capacitance (T_A = 25 C, f = 100 MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK[1:0], /CK[1:0]	C_{CK}	6.4	12.8	pF
Input Capacitance, Address	BA[2:0], A[15:0], /RAS, /CAS, /WE	C_I	12	20.8	pF
Input Capacitance Control	/S[1:0], CKE[1:0], ODT[1:0]	C_I	6	10.4	pF
Input/Output Capacitance	DQ[63:0], DQS[7:0], /DQS[7:0], DM[7:0]	C_{IO}	3	5	pF

DC Characteristics (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input 0 V < VIN < VDD)	I_{IL}	-16	+16	µA	1,2
Output Leakage Current (0V < VOUT < VDDQ)	I_{OL}	-10	+10	µA	2,3

Notes:
1) All other pins not under test = 0 V
2) Values are shown per pin
3) DQ's, DQS, DQS and ODT are disabled

I_{DD} Specifications and Conditions (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Test Condition	Max Value	Unit
Operating One Bank Active-Precharge Current	$I_{DD}0$*	Operating current : One bank ACTIVATE-to-PRECHARGE	520	mA
Operating One Bank Active-Read-Precharge Current	$I_{DD}1$*	Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE	600	mA
Precharge Power-Down Current	$I_{DD}2P$**	Precharge power down current: (Slow exit)	240	mA
Precharge Power-Down Current	$I_{DD}2P$**	Precharge power down current: (Fast exit)	240	mA
Precharge Quiet Standby Current	$I_{DD}2Q$**	Precharge quiet standby current	320	mA
Precharge Standby Current	$I_{DD}2N$**	Precharge standby current	320	mA
Active Power-Down Current	$I_{DD}3P$**	Active power-down current	320	mA
Active Standby Current	$I_{DD}3N$**	Active standby current	400	mA
Operating Burst Write Current	$I_{DD}4W$*	Burst write operating current	1040	mA
Operating Burst Read Current	$I_{DD}4R$*	Burst read operating current	960	mA
Burst Refresh Current	$I_{DD}5$**	Refresh current	1320	mA
Self Refresh Current	$I_{DD}6$**	Self-refresh temperature current: MAX Tc = 85°C	240	mA
Operating Bank Interleave Read Current	$I_{DD}7$*	All bank interleaved read current	1560	mA

* One module rank in this operation rest in IDD2P slow exit.
** All module ranks in this operation.

AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	t_{AA}	13.125	20	ns
CAS-to-CAS Command Delay	t_{CCD}	4	-	t_{CK}
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	t_{CK}
Clock Cycle Time	t_{CK}	1.25	2.5	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	t_{CK}
Data Input Hold Time after DQS Strobe	t_{DH}	45	-	ps
DQ Input Pulse Width	t_{DIPW}	360	-	ps
DQS Output Access Time from Clock	t_{DQSCK}	-225	+225	ps
Write DQS High Level Width	t_{DQSH}	0.45	0.55	$t_{CK(avg)}$
Write DQS Low Level Width	t_{DQSL}	0.45	0.55	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	t_{DQSQ}	-	125	ps
Data Input Setup Time Before DQS Strobe	t_{DS}	10	-	ps
DQS Falling Edge from Clock, Hold Time	t_{DSH}	0.18	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	t_{DSS}	0.18	-	$t_{CK(avg)}$
Address and Command Hold Time after Clock	t_{IH}	120	-	ps
Address and Command Setup Time before Clock	t_{IS}	45	-	ps
Load Mode Command Cycle Time	t_{MRD}	4	-	t_{CK}
DQ-to-DQS Hold	t_{QH}	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	t_{RAS}	36	$9*t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	t_{RC}	48.125	-	ns
RAS-to-CAS Delay	t_{RCD}	13.125	-	ns
Average Periodic Refresh Interval $0^o C \leq T_{CASE} < 85^o C$	t_{REFI}	-	7.8	µs
Average Periodic Refresh Interval $85^o C \leq T_{CASE} < 95^o C$	t_{REFI}	-	3.9	µs
Auto Refresh Row Cycle Time	t_{RFC}	260	-	ns
Row Precharge Time	t_{RP}	13.125	-	ns
Read DQS Preamble Time	t_{RPRE}	0.9	Note 1	$t_{CK(avg)}$
Read DQS Postamble Time	t_{RPST}	0.3	Note 2	$t_{CK(avg)}$
Row Active to Row Active Delay	t_{RRD}	Max(4nCK, 6ns)	-	ns
Internal Read to Precharge Command Delay	t_{RTP}	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	t_{WPRE}	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	t_{WPST}	0.3	-	$t_{CK(avg)}$
Write Recovery Time	t_{WR}	15	-	ns
Internal Write to Read Command Delay	t_{WTR}	Max(4nCK, 7.5ns)	-	ns

Notes:
1. The maximum preamble is bound by tLZDQS(min)
2. The maximum postamble is bound by tHZDQS(max)

SPD available upon request.

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