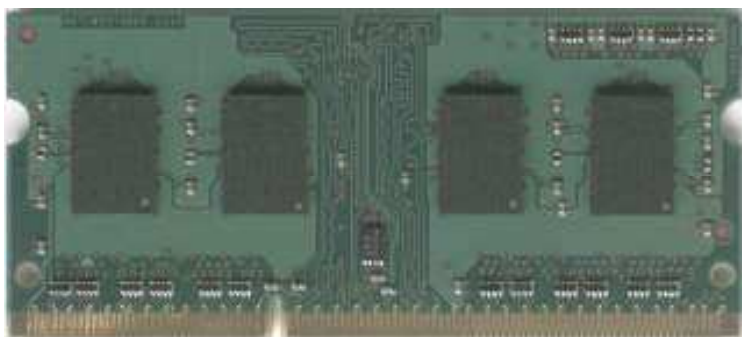




# DTM64605B

2GB - 204-pin 1Rx8 Unbuffered Non-ECC DDR3 SO-DIMM



## Identification

DTM64605B 256Mx64  
2GB 1Rx8 PC3-10600S-9-11-B2

## Performance range

Clock / Module Speed / CL-t<sub>TRCD</sub> -t<sub>TRP</sub>

667 MHz / DDR3-1333 / 9-9-9  
533 MHz / DDR3-1066 / 8-8-8  
533 MHz / DDR3-1066 / 7-7-7  
400 MHz / DDR3-800 / 6-6-6  
333 MHz / DDR3-667 / 5-5-5

## Features

204-pin SO-DIMM. Dual-sided assembly 67.60 mm [2.661"] wide by 30.0 mm [1.181"] high

Operating Voltage: 1.5 V ±0.075 V

I/O Type: SSTL\_15

Data Transfer Rate: 10.6 Gigabytes/sec

Data Bursts: 8 and burst chop 4 mode

ZQ Calibration for Output Driver and On-Die Termination (ODT)

Programmable ODT / Dynamic ODT during Writes

Programmable CAS Latency: 5, 6, 7, 8 and 9

Bi-directional Differential Data Strobe signals

SDRAM Addressing (Row/Col/Bank): 15/10/3

Fully RoHS Compliant

## Description

DTM64605B is a non-ECC Unbuffered DDR3-1333, 256Mx64 memory module. The assembly is a one rank SO-DIMM comprised of eight Samsung 256Mx8 DDR3 SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals.

The assembly is a Small Outline Dual In-line Memory Module intended for mounting into 204-pin edge connector sockets.

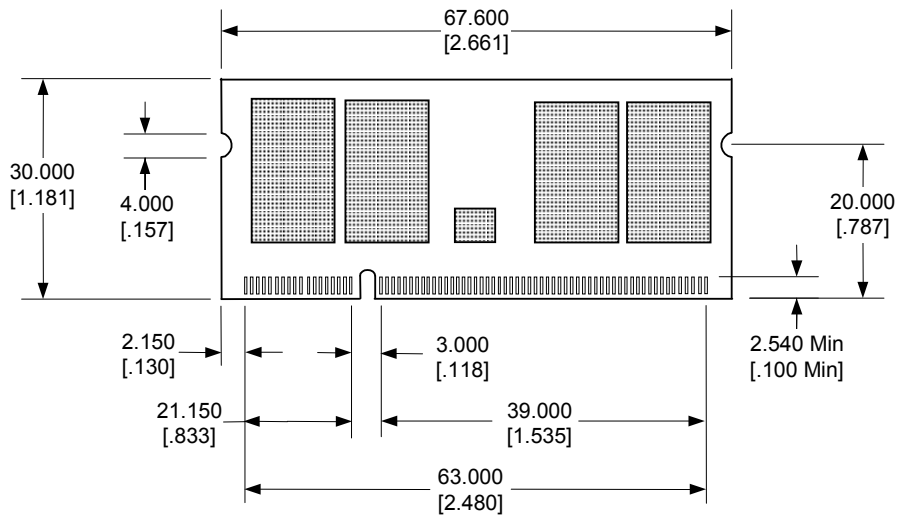
## Pin Configuration

## Pin Description

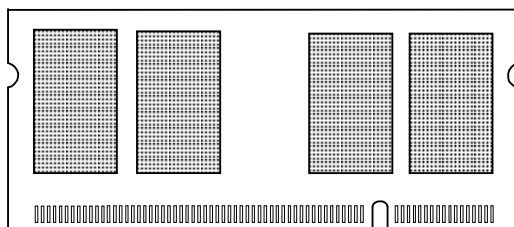
| Front Side           |                    |                     |                        | Back Side          |                     |                        |                     | Name                | Function                     |
|----------------------|--------------------|---------------------|------------------------|--------------------|---------------------|------------------------|---------------------|---------------------|------------------------------|
| 1 V <sub>REFDQ</sub> | 53 DQ19            | 105 V <sub>DD</sub> | 157 DQ42               | 2 V <sub>SS</sub>  | 54 V <sub>SS</sub>  | 106 V <sub>DD</sub>    | 158 DQ46            | DQ[63:0]            | Data Bits                    |
| 3 V <sub>SS</sub>    | 55 V <sub>SS</sub> | 107 A10/AP          | 159 DQ43               | 4 DQ4              | 56 DQ28             | 108 BA1                | 160 DQ47            | DQS[7:0], /DQS[7:0] | Differential Data Strobes    |
| 5 DQ0                | 57 DQ24            | 109 BA0             | 161 V <sub>SS</sub>    | 6 DQ5              | 58 DQ29             | 110 /RAS               | 162 V <sub>SS</sub> | DM[7:0]             | Data Mask                    |
| 7 DQ1                | 59 DQ25            | 111 V <sub>DD</sub> | 163 DQ48               | 8 V <sub>SS</sub>  | 60 V <sub>SS</sub>  | 112 V <sub>DD</sub>    | 164 DQ52            | CK[1:0], /CK[1:0]   | Differential Clock Inputs    |
| 9 V <sub>SS</sub>    | 61 V <sub>SS</sub> | 113 /WE             | 165 DQ49               | 10 /DQS0           | 62 /DQS3            | 114 /S0                | 166 DQ53            | CKE0                | Clock Enables                |
| 11 DM0               | 63 DM3             | 115 /CAS            | 167 V <sub>SS</sub>    | 12 DQS0            | 64 DQS3             | 116 ODT0               | 168 V <sub>SS</sub> | /CAS                | Column Address Strobe        |
| 13 V <sub>SS</sub>   | 65 V <sub>SS</sub> | 117 V <sub>DD</sub> | 169 /DQS6              | 14 V <sub>SS</sub> | 66 V <sub>SS</sub>  | 118 V <sub>DD</sub>    | 170 DM6             | /RAS                | Row Address Strobe           |
| 15 DQ2               | 67 DQ26            | 119 A13             | 171 DQS6               | 16 DQ6             | 68 DQ30             | 120 NC                 | 172 V <sub>SS</sub> | /S0                 | Chip Selects                 |
| 17 DQ3               | 69 DQ27            | 121 NC              | 173 V <sub>SS</sub>    | 18 DQ7             | 70 DQ31             | 122 NC                 | 174 DQ54            | /WE                 | Write Enable                 |
| 19 V <sub>SS</sub>   | 71 V <sub>SS</sub> | 123 V <sub>DD</sub> | 175 DQ50               | 20 V <sub>SS</sub> | 72 V <sub>SS</sub>  | 124 V <sub>DD</sub>    | 176 DQ55            | A[15:0]             | Address Inputs               |
| 21 DQ8               | 73 CKE0            | 125 NC/TEST         | 177 DQ51               | 22 DQ12            | 74 NC               | 126 V <sub>REFCA</sub> | 178 V <sub>SS</sub> | BA[2:0]             | Bank Addresses               |
| 23 DQ9               | 75 V <sub>DD</sub> | 127 V <sub>SS</sub> | 179 V <sub>SS</sub>    | 24 DQ13            | 76 V <sub>DD</sub>  | 128 V <sub>SS</sub>    | 180 DQ60            | ODT0                | On Die Termination Inputs    |
| 25 V <sub>SS</sub>   | 77 NC              | 129 DQ32            | 181 DQ56               | 26 V <sub>SS</sub> | 78 A15*             | 130 DQ36               | 182 DQ61            | SA[1:0]             | SPD Address                  |
| 27 /DQS1             | 79 BA2             | 131 DQ33            | 183 DQ57               | 28 DM1             | 80 A14              | 132 DQ37               | 184 V <sub>SS</sub> | SCL                 | SPD Clock Input              |
| 29 DQS1              | 81 V <sub>DD</sub> | 133 V <sub>SS</sub> | 185 V <sub>SS</sub>    | 30 /RESET          | 82 V <sub>DD</sub>  | 134 V <sub>SS</sub>    | 186 /DQS7           | SDA                 | SPD Data Input/Output        |
| 31 V <sub>SS</sub>   | 83 A12/BC          | 135 /DQS4           | 187 DM7                | 32 V <sub>SS</sub> | 84 A11              | 136 DM4                | 188 DQS7            | TEST                | Logic Analyzer specific      |
| 33 DQ10              | 85 A9              | 137 DQS4            | 189 V <sub>SS</sub>    | 34 DQ14            | 86 A7               | 138 V <sub>SS</sub>    | 190 V <sub>SS</sub> | EVENT               | Output of the Thermal Sensor |
| 35 DQ11              | 87 V <sub>DD</sub> | 139 V <sub>SS</sub> | 191 DQ58               | 36 DQ15            | 88 V <sub>DD</sub>  | 140 DQ38               | 192 DQ62            | V <sub>SS</sub>     | Ground                       |
| 37 V <sub>SS</sub>   | 89 A8              | 141 DQ34            | 193 DQ59               | 38 V <sub>SS</sub> | 90 A6               | 142 DQ39               | 194 DQ63            | V <sub>DD</sub>     | Power                        |
| 39 DQ16              | 91 A5              | 143 DQ35            | 195 V <sub>SS</sub>    | 40 DQ20            | 92 A4               | 144 V <sub>SS</sub>    | 196 V <sub>SS</sub> | V <sub>DDSPD</sub>  | SPD EEPROM Power             |
| 41 DQ17              | 93 V <sub>DD</sub> | 145 V <sub>SS</sub> | 197 SA0                | 42 DQ21            | 94 V <sub>DD</sub>  | 146 DQ44               | 198 EVENT*          | V <sub>REFDQ</sub>  | Reference Voltage for DQ     |
| 43 V <sub>SS</sub>   | 95 A3              | 147 DQ40            | 199 V <sub>DDSPD</sub> | 44 V <sub>SS</sub> | 96 A2               | 148 DQ45               | 200 SDA             | V <sub>REFCA</sub>  | Reference Voltage for CA     |
| 45 /DQS2             | 97 A1              | 149 DQ41            | 201 SA1                | 46 DM2             | 98 A0               | 150 V <sub>SS</sub>    | 202 SCL             | V <sub>TT</sub>     | Termination Voltage          |
| 47 DQS2              | 99 V <sub>DD</sub> | 151 V <sub>SS</sub> | 203 V <sub>TT</sub>    | 48 V <sub>SS</sub> | 100 V <sub>DD</sub> | 152 /DQS5              | 204 V <sub>TT</sub> | NC                  | No Connection                |
| 49 V <sub>SS</sub>   | 101 CK0            | 153 DM5             |                        | 50 DQ22            | 102 CK1*            | 154 DQS5               |                     |                     |                              |
| 51 DQ18              | 103 /CK0           | 155 V <sub>SS</sub> |                        | 52 DQ23            | 104 /CK1*           | 156 V <sub>SS</sub>    |                     |                     |                              |

\* = Not Used

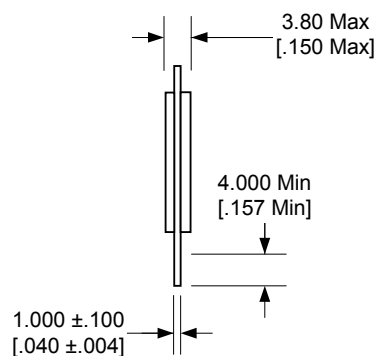
### Front view



### Back view



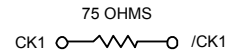
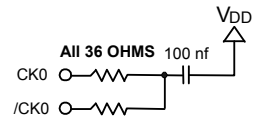
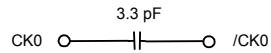
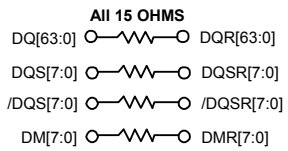
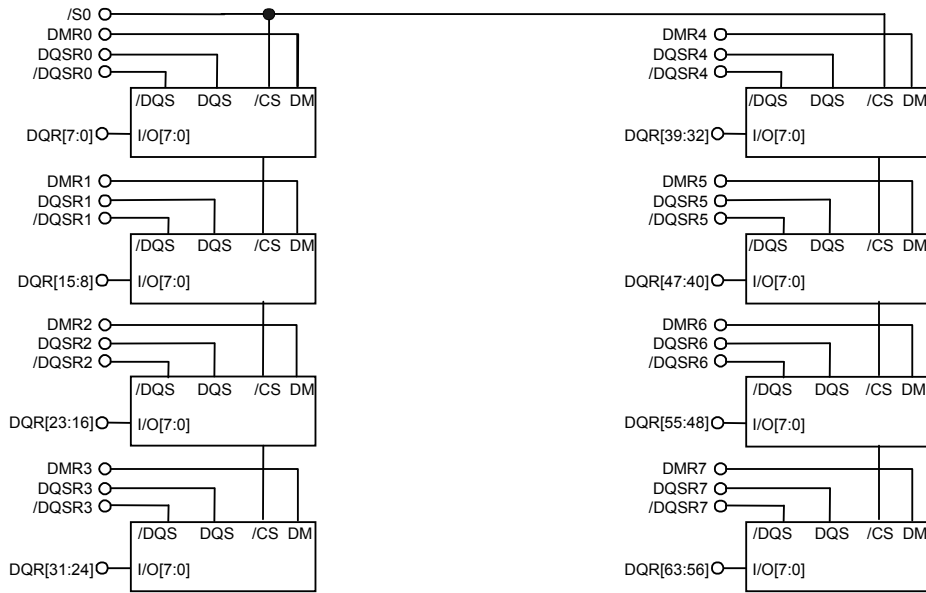
### Side view



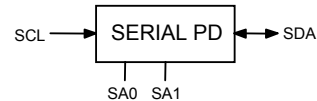
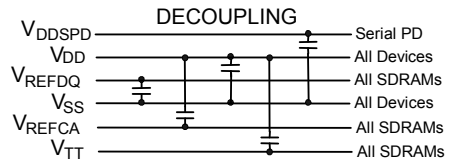
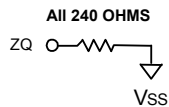
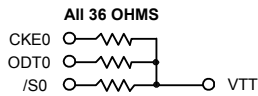
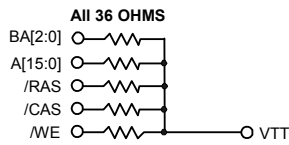
### Notes

Tolerances on all dimensions except where otherwise indicated are  $\pm .13$  (.005).

All dimensions are expressed: millimeters [inches]



### GLOBAL SDRAM CONNECTS





# DTM64605B

2GB - 204-pin 1Rx8 Unbuffered Non-ECC DDR3 SO-DIMM

## Absolute Maximum Ratings

(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

| PARAMETER                                | Symbol            | Minimum | Maximum | Unit |
|--|-------------------|---------|---------|------|
| Temperature, non-Operating               | $T_{STORAGE}$     | -55     | 100     | C    |
| Module Ambient Temperature, Operating    | $T_A$             | 0       | 85      | C    |
| DRAM Case Temperature, Operating         | $T_{CASE}$        | 0       | 95      | C    |
| Voltage on $V_{DD}$ relative to $V_{SS}$ | $V_{DD}$          | -0.4    | 1.975   | V    |
| Voltage on Any Pin relative to $V_{SS}$  | $V_{IN}, V_{OUT}$ | -0.4    | 1.975   | V    |

Notes:

DRAM Operating Case Temperature above 85C requires 2X refresh.

## Recommended DC Operating Conditions ( $T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

| PARAMETER             | Symbol      | Minimum       | Typical       | Maximum       | Unit | Note |
|-----------------------|-------------|---------------|---------------|---------------|------|------|
| Power Supply Voltage  | $V_{DD}$    | 1.425         | 1.5           | 1.575         | V    |      |
| I/O Reference Voltage | $V_{REFDQ}$ | 0.49 $V_{DD}$ | 0.50 $V_{DD}$ | 0.51 $V_{DD}$ | V    | 1    |
| I/O Reference Voltage | $V_{REFCA}$ | 0.49 $V_{DD}$ | 0.50 $V_{DD}$ | 0.51 $V_{DD}$ | V    | 1    |

Notes:

The value of  $V_{REF}$  is expected to equal one-half  $V_{DD}$  and to track variations in the  $V_{DD}$  DC level. Peak-to-peak noise on  $V_{REF}$  may not exceed  $\pm 1\%$  of its DC value. For Reference  $V_{DD}/2 \pm 15$  mV.

## DC Input Logic Levels, Single-Ended ( $T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

| PARAMETER              | Symbol       | Minimum         | Maximum         | Unit |
|------------------------|--------------|-----------------|-----------------|------|
| Logical High (Logic 1) | $V_{IH(DC)}$ | $V_{REF} + 0.1$ | $V_{DD}$        | V    |
| Logical Low (Logic 0)  | $V_{IL(DC)}$ | $V_{SS}$        | $V_{REF} - 0.1$ | V    |

## AC Input Logic Levels, Single-Ended ( $T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

| PARAMETER              | Symbol       | Minimum           | Maximum           | Unit |
|------------------------|--------------|-------------------|-------------------|------|
| Logical High (Logic 1) | $V_{IH(AC)}$ | $V_{REF} + 0.175$ | -                 | V    |
| Logical Low (Logic 0)  | $V_{IL(AC)}$ | -                 | $V_{REF} - 0.175$ | V    |



# DTM64605B

2GB - 204-pin 1Rx8 Unbuffered Non-ECC DDR3 SO-DIMM

## Differential Input Logic Levels ( $T_A = 0$ to $70$ C, Voltage referenced to $V_{SS} = 0$ V)

| PARAMETER   | Symbol        | Minimum                       | Maximum                       | Unit |
|---|---------------|-------------------------------|-------------------------------|------|
| Differential Input Logic High                                 | $V_{IH,DIFF}$ | +0.200                        | DC: $V_{DD}$ AC: $V_{DD}+0.4$ | V    |
| Differential Input Logic Low                                  | $V_{IL,DIFF}$ | DC: $V_{SS}$ AC: $V_{SS}-0.4$ | -0.200                        | V    |
| Differential Input Cross Point Voltage relative to $V_{DD}/2$ | $V_{IX}$      | - 0.150                       | + 0.150                       | V    |

## Capacitance ( $T_A = 25$ C, $f = 100$ MHz)

| PARAMETER                  | Pin                                    | Symbol   | Minimum | Maximum | Unit |
|----------------------------|--|----------|---------|---------|------|
| Input Capacitance, Clock   | CK0, /CK0                              | $C_{CK}$ | 7.2     | 11.2    | pF   |
| Input Capacitance, Address | BA[2:0], A[14:0], /RAS, /CAS, /WE      | $C_I$    | 6.0     | 10.4    | pF   |
| Input Capacitance Control  | /S0, CKE0, ODT0                        | $C_I$    | 6.0     | 10.4    |      |
| Input/Output Capacitance   | DQ[63:0], DQS[7:0], /DQS[7:0], DM[7:0] | $C_{IO}$ | 1.5     | 2.5     | pF   |

## DC Characteristics ( $T_A = 0$ to $70$ C, Voltage referenced to $V_{SS} = 0$ V)

| PARAMETER   | Symbol   | Minimum | Maximum | Unit    | Note |
|---|----------|---------|---------|---------|------|
| Input Leakage Current<br>(Any input $0$ V < $V_{IN}$ < $V_{DD}$ ) | $I_{IL}$ | -18     | +18     | $\mu$ A | 1,2  |
| Output Leakage Current<br>( $0$ V < $V_{OUT}$ < $V_{DDQ}$ )       | $I_{OL}$ | -10     | +10     | $\mu$ A | 2,3  |

Notes:

- 1) All other pins not under test = 0 V
- 2) Values are shown per pin
- 3) DQ's, DQS, DQS and ODT are disabled



# DTM64605B

2GB - 204-pin 1Rx8 Unbuffered Non-ECC DDR3 SO-DIMM

I<sub>DD</sub> Specifications and Conditions (TA = 0 to 70 C, Voltage referenced to V<sub>SS</sub> = 0 V)

| PARAMETER  | Symbol            | Test Condition  | Max Value | Unit |
|--|-------------------|---|-----------|------|
| Operating One Bank Active-Precharge Current      | I <sub>DD0</sub>  | Operating current : One bank ACTIVATE-to-PRECHARGE          | 320       | mA   |
| Operating One Bank Active-Read-Precharge Current | I <sub>DD1</sub>  | Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE  | 400       | mA   |
| Precharge Power-Down Current                     | I <sub>DD2P</sub> | Precharge power down current: (Slow exit)                   | 96        | mA   |
| Precharge Power-Down Current                     | I <sub>DD2P</sub> | Precharge power down current: (Fast exit)                   | 120       | mA   |
| Precharge Quiet Standby Current                  | I <sub>DD2Q</sub> | Precharge quiet standby current                             | 160       | mA   |
| Precharge Standby Current                        | I <sub>DD2N</sub> | Precharge standby current                                   | 160       | mA   |
| Active Power-Down Current                        | I <sub>DD3P</sub> | Active power-down current                                   | 136       | mA   |
| Active Standby Current                           | I <sub>DD3N</sub> | Active standby current                                      | 280       | mA   |
| Operating Burst Write Current                    | I <sub>DD4W</sub> | Burst write operating current                               | 640       | mA   |
| Operating Burst Read Current                     | I <sub>DD4R</sub> | Burst read operating current                                | 600       | mA   |
| Burst Refresh Current                            | I <sub>DD5</sub>  | Refresh current   | 920       | mA   |
| Self Refresh Current                             | I <sub>DD6</sub>  | Self-refresh temperature current: MAX T <sub>c</sub> = 85°C | 96        | mA   |
| Operating Bank Interleave Read Current           | I <sub>DD7</sub>  | All bank interleaved read current                           | 1080      | mA   |



# DTM64605B

2GB - 204-pin 1Rx8 Unbuffered Non-ECC DDR3 SO-DIMM

## AC Operating Conditions

| PARAMETER   | Symbol        | Min              | Max                | Unit          |
|---|---------------|------------------|--------------------|---------------|
| Internal read command to first data   | $t_{AA}$      | 13.125           | 20                 | ns            |
| CAS-to-CAS Command Delay  | $t_{CCD}$     | 4                | -                  | $t_{CK}$      |
| Clock High Level Width  | $t_{CH(avg)}$ | 0.47             | 0.53               | $t_{CK}$      |
| Clock Cycle Time  | $t_{CK}$      | 1.5              | 2.5                | ns            |
| Clock Low Level Width   | $t_{CL(avg)}$ | 0.47             | 0.53               | $t_{CK}$      |
| Data Input Hold Time after DQS Strobe   | $t_{DH}$      | 65               | -                  | ps            |
| DQ Input Pulse Width  | $t_{DIPW}$    | 400              | -                  | ps            |
| DQS Output Access Time from Clock   | $t_{DQSCK}$   | -255             | +255               | ps            |
| Write DQS High Level Width  | $t_{DQSH}$    | 0.45             | 0.55               | $t_{CK(avg)}$ |
| Write DQS Low Level Width   | $t_{DQSL}$    | 0.45             | 0.55               | $t_{CK(avg)}$ |
| DQS-Out Edge to Data-Out Edge Skew  | $t_{DQSQ}$    | -                | 125                | ps            |
| Data Input Setup Time Before DQS Strobe                                       | $t_{DS}$      | 30               | -                  | ps            |
| DQS Falling Edge from Clock, Hold Time  | $t_{DSH}$     | 0.2              | -                  | $t_{CK(avg)}$ |
| DQS Falling Edge to Clock, Setup Time   | $t_{DSS}$     | 0.2              | -                  | $t_{CK(avg)}$ |
| Address and Command Hold Time after Clock                                     | $t_{IH}$      | 140              | -                  | ps            |
| Address and Command Setup Time before Clock                                   | $t_{IS}$      | 65               | -                  | ps            |
| Load Mode Command Cycle Time  | $t_{MRD}$     | 4                | -                  | $t_{CK}$      |
| DQ-to-DQS Hold  | $t_{QH}$      | 0.38             | -                  | $t_{CK(avg)}$ |
| Active-to-Precharge Time  | $t_{RAS}$     | 36               | $9 \cdot t_{REFI}$ | ns            |
| Active-to-Active / Auto Refresh Time  | $t_{RC}$      | 49.125           | -                  | ns            |
| RAS-to-CAS Delay  | $t_{RCD}$     | 13.125           | -                  | ns            |
| Average Periodic Refresh Interval $0^{\circ} C \leq T_{CASE} < 85^{\circ} C$  | $t_{REFI}$    | -                | 7.8                | $\mu s$       |
| Average Periodic Refresh Interval $85^{\circ} C \leq T_{CASE} < 95^{\circ} C$ | $t_{REFI}$    | -                | 3.9                | $\mu s$       |
| Auto Refresh Row Cycle Time   | $t_{RFC}$     | 160              | -                  | ns            |
| Row Precharge Time  | $t_{RP}$      | 13.125           | -                  | ns            |
| Read DQS Preamble Time  | $t_{RPRE}$    | 0.9              | Note 1             | $t_{CK(avg)}$ |
| Read DQS Postamble Time   | $t_{RPST}$    | 0.3              | Note 2             | $t_{CK(avg)}$ |
| Row Active to Row Active Delay  | $t_{RRD}$     | Max(4nCK, 6ns)   | -                  | ns            |
| Internal Read to Precharge Command Delay                                      | $t_{RTP}$     | Max(4nCK, 7.5ns) | -                  | ns            |
| Write DQS Preamble Setup Time   | $t_{WPRE}$    | 0.9              | -                  | $t_{CK(avg)}$ |
| Write DQS Postamble Time  | $t_{WPST}$    | 0.3              | -                  | $t_{CK(avg)}$ |
| Write Recovery Time   | $t_{WR}$      | 15               | -                  | ns            |
| Internal Write to Read Command Delay  | $t_{WTR}$     | Max(4nCK, 7.5ns) | -                  | ns            |

Notes:

1. The maximum preamble is bound by  $t_{LZDQS}(\min)$
2. The maximum postamble is bound by  $t_{HZDQS}(\max)$



# DTM64605B

2GB - 204-pin 1Rx8 Unbuffered Non-ECC DDR3 SO-DIMM

## SERIAL PRESENCE DETECT MATRIX

| Byte#             | Function.  | Value             | Hex  |
|-------------------|--|-------------------|------|
| 0                 | Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage. |                   | 0x92 |
|                   | Bit 3 ~ Bit 0. SPD Bytes Used -                                      | 176               |      |
|                   | Bit 6 ~ Bit 4. SPD Bytes Total -                                     | 256               |      |
|                   | Bit 7. CRC Coverage -  | Bytes 0-116       |      |
| 1                 | SPD Revision.  | Rev. 1.1          | 0x11 |
| 2                 | Key Byte / DRAM Device Type.   | DDR3 SDRAM        | 0x0B |
| 3                 | Key Byte / Module Type.  |                   | 0x03 |
|                   | Bit 3 ~ Bit 0. Module Type -   | SO-DIMM           |      |
|                   | Bit 7 ~ Bit 4. Reserved -  | 0                 |      |
| 4                 | SDRAM Density and Banks.   |                   | 0x03 |
|                   | Bit 3 ~ Bit 0. Total SDRAM capacity, in megabits -                   | 2Gb               |      |
|                   | Bit 6 ~ Bit 4. Bank Address Bits -                                   | 8 banks           |      |
|                   | Bit 7. Reserved -  | 0                 |      |
| 5                 | SDRAM Addressing.  |                   | 0x19 |
|                   | Bit 2 ~ Bit 0. Column Address Bits -                                 | 10                |      |
|                   | Bit 5 ~ Bit 3. Row Address Bits -                                    | 15                |      |
|                   | Bit 7, 6. Reserved   | 0                 |      |
| 6                 | Module Nominal Voltage, VDD.   |                   | 0x00 |
|                   | Bit 0. NOT 1.5 V operable -  |                   |      |
|                   | Bit 1. 1.35 V operable -   |                   |      |
|                   | Bit 2. 1.2X V operable -   |                   |      |
|                   | Bit 3. Reserved -  |                   |      |
|                   | Bit 4. Reserved -  |                   |      |
|                   | Bit 5. Reserved -  |                   |      |
|                   | Bit 6. Reserved -  |                   |      |
| Bit 7. Reserved - |  |                   |      |
| 7                 | Module Organization.   |                   | 0x01 |
|                   | Bit 2 ~ Bit 0. SDRAM Device Width -                                  | 8-Bits            |      |
|                   | Bit 5 ~ Bit 3. Number of Ranks -                                     | 1-Rank            |      |
|                   | Bit 7, 6. Reserved   | 0                 |      |
| 8                 | Module Memory Bus Width.   |                   | 0x03 |
|                   | Bit 2 ~ Bit 0. Primary bus width, in bits -                          | 64-Bits           |      |
|                   | Bit 4, Bit 3. Bus width extension, in bits -                         | 0-Bits            |      |
|                   | Bit 7 ~ Bit 5. Reserved -  | 0                 |      |
| 9                 | Fine Timebase (FTB) Dividend / Divisor.                              |                   | 0x11 |
|                   | Bit 3 ~ Bit 0. Fine Timebase (FTB) Divisor                           | 1                 |      |
|                   | Bit 7 ~ Bit 4. Fine Timebase (FTB) Dividend                          | 1                 |      |
| 10                | Medium Timebase (MTB) Dividend.                                      | 1 (MTB = 0.125ns) | 0x01 |



# DTM64605B

2GB - 204-pin 1Rx8 Unbuffered Non-ECC DDR3 SO-DIMM

|    |   |                   |      |
|----|---|-------------------|------|
| 11 | Medium Timebase (MTB) Divisor.  | 8 (MTB = 0.125ns) | 0x08 |
| 12 | SDRAM Minimum Cycle Time (tCKmin).  | 1.5ns             | 0x0C |
| 13 | Reserved.   | UNUSED            | 0x00 |
| 14 | CAS Latencies Supported, Least Significant Byte.                              |                   | 0x3E |
|    | Bit 0. CL = 4 -   |                   |      |
|    | Bit 1. CL = 5 -   | X                 |      |
|    | Bit 2. CL = 6 -   | X                 |      |
|    | Bit 3. CL = 7 -   | X                 |      |
|    | Bit 4. CL = 8 -   | X                 |      |
|    | Bit 5. CL = 9 -   | X                 |      |
|    | Bit 6. CL = 10 -<br>Bit 7. CL = 11 -  |                   |      |
| 15 | CAS Latencies Supported, Most Significant Byte.                               |                   | 0x00 |
|    | Bit 0. CL = 12 -  |                   |      |
|    | Bit 1. CL = 13 -  |                   |      |
|    | Bit 2. CL = 14 -  |                   |      |
|    | Bit 3. CL = 15 -  |                   |      |
|    | Bit 4. CL = 16 -  |                   |      |
|    | Bit 5. CL = 17 -  |                   |      |
|    | Bit 6. CL = 18 -<br>Bit 7. Reserved.  |                   |      |
| 16 | Minimum CAS Latency Time (tAmin).   | 13.125ns          | 0x69 |
| 17 | Minimum Write Recovery Time (tWRmin).   | 15.0ns            | 0x78 |
| 18 | Minimum RAS# to CAS# Delay Time (tRCDmin).                                    | 13.125ns          | 0x69 |
| 19 | Minimum Row Active to Row Active Delay Time (tRRDmin).                        | 6.0ns             | 0x30 |
| 20 | Minimum Row Precharge Delay Time (tRPmin).                                    | 13.125ns          | 0x69 |
| 21 | Upper Nibbles for tRAS and tRC.   |                   | 0x11 |
|    | Bit 3 ~ Bit 0. tRAS Most Significant Nibble -                                 | 1                 |      |
|    | Bit 7 ~ Bit 4. tRC Most Significant Nibble -                                  | 1                 |      |
| 22 | Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte.     | 36.0ns            | 0x20 |
| 23 | Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte. | 49.125ns          | 0x89 |
| 24 | Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte.        | 160.0ns           | 0x00 |
| 25 | Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte.         | 160.0ns           | 0x05 |
| 26 | Minimum Internal Write to Read Command Delay Time (tWTRmin).                  | 7.5ns             | 0x3C |
| 27 | Minimum Internal Read to Precharge Command Delay Time (tRTPmin).              | 7.5ns             | 0x3C |
| 28 | Upper Nibble for tFAW.  |                   | 0x00 |
|    | Bit 3 ~ Bit 0. tFAW Most Significant Nibble -                                 | 0                 |      |



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|         |  |          |      |
|---------|--|----------|------|
|         | Bit 7 ~ Bit 4. Reserved -  | 0        |      |
| 29      | Minimum Four Activate Window Delay Time (tFAWmin), Least Significant Byte. | 30.0ns   | 0xF0 |
| 30      | SDRAM Optional Features.   |          | 0x83 |
|         | Bit 0. RZQ / 6 -   | X        |      |
|         | Bit 1. RZQ / 7 -   | X        |      |
|         | Bit 6 ~ Bit 2. Reserved -<br>Bit 7. DLL-Off Mode Support                   |          |      |
| 31      | SDRAM Drivers Supported.   |          | 0x01 |
|         | Extended Temperature Range -   | X        |      |
|         | Extended Temperature Refresh Rate -  |          |      |
|         | Auto Self Refresh (ASR) -  |          |      |
|         | On-die Thermal Sensor (ODTS) Readout -                                     |          |      |
|         | Reserved -   |          |      |
|         | Reserved -   |          |      |
|         | Reserved -   |          |      |
| 32      | Module Thermal Sensor.   |          | 0x00 |
|         | Bit 6 ~ Bit 0. Thermal Sensor Accuracy -                                   | 0        |      |
|         | Bit 7. Thermal Sensor -  | No TS    |      |
| 33      | SDRAM Device Type.   |          | 0x00 |
|         | Bit 6 ~ Bit 0. Non-Standard Device Description -                           | 0        |      |
|         | Bit 7. SDRAM Device Type -   | Std Mono |      |
| 34-59   | Reserved   | UNUSED   | 0x00 |
| 60      | Module Nominal Height.   |          | 0x0F |
|         | Bit 4 ~ Bit 0. Module Nominal Height max, in mm -                          | 29<h<=30 |      |
|         | Bit 7 ~ Bit5. Reserved -   | 0        |      |
| 61      | Module Maximum Thickness.  |          | 0x11 |
|         | Bit 3 ~ Bit 0. Front, in mm (baseline thickness = 1 mm) -                  | 1<th<=2  |      |
|         | Bit 7 ~ Bit 4. Back, in mm (baseline thickness = 1 mm) -                   | 1<th<=2  |      |
| 62      | Reference Raw Card Used.   |          | 0x41 |
|         | Bit 4 ~ Bit 0. Reference Raw Card -  | R/C B    |      |
|         | Bit 6, Bit 5. Reference Raw Card Revision -                                | Rev.2    |      |
|         | Bit 7. Reserved -  | 0        |      |
| 63      | Address Mapping from Edge Connector to DRAM.                               |          | 0x00 |
|         | Bit 0. Rank 1 Mapping (Registered DIMM - Reserved) -                       | Standard |      |
|         | Bit 7 ~ Bit 1. Reserved -  | 0        |      |
| 64-112  | Module-Specific Section  | UNUSED   | 0x00 |
| 113     | Module-Specific Section.   | UNUSED   | 0x00 |
| 114-116 | Module-Specific Section  | UNUSED   | 0x00 |
| 117     | Module Manufacturer ID Code, Least Significant Byte                        |          | 0x80 |
| 118     | Module Manufacturer ID Code, Most Significant Byte                         |          | 0xCE |



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|         |   |        |      |
|---------|---|--------|------|
| 119     | Module Manufacturing Location                     |        | 0x02 |
| 120     | Module Manufacturing Date                         |        | 0x11 |
| 121     | Module Manufacturing Date                         |        | 0x15 |
| 122     | Module Serial Number                              | #      | 0x23 |
| 123     | Module Serial Number                              | #      | 0x23 |
| 124     | Module Serial Number                              | #      | 0x23 |
| 125     | Module Serial Number                              | #      | 0x23 |
| 126     | Cyclical Redundancy Code (CRC).                   | CRC    | 0x50 |
| 127     | Cyclical Redundancy Code (CRC).                   | CRC    | 0xA2 |
| 128     | Module Part Number                                | M      | 0x4D |
| 129     | Module Part Number                                | 4      | 0x34 |
| 130     | Module Part Number                                | 7      | 0x37 |
| 131     | Module Part Number                                | 1      | 0x31 |
| 132     | Module Part Number                                | B      | 0x42 |
| 133     | Module Part Number                                | 5      | 0x35 |
| 134     | Module Part Number                                | 7      | 0x37 |
| 135     | Module Part Number                                | 7      | 0x37 |
| 136     | Module Part Number                                | 3      | 0x33 |
| 137     | Module Part Number                                | D      | 0x44 |
| 138     | Module Part Number                                | H      | 0x48 |
| 139     | Module Part Number                                | 0      | 0x30 |
| 140     | Module Part Number                                | -      | 0x2D |
| 141     | Module Part Number                                | C      | 0x43 |
| 142     | Module Part Number                                | H      | 0x48 |
| 143     | Module Part Number                                | 9      | 0x39 |
| 144,145 | Module Part Number                                |        | 0x20 |
| 146,147 | Module Revision Code                              | UNUSED | 0x00 |
| 148     | DRAM Manufacturer ID Code, Least Significant Byte | €      | 0x80 |
| 149     | DRAM Manufacturer ID Code, Most Significant Byte  | î      | 0xCE |
| 150-175 | Manufacturer's Specific Data                      | UNUSED | 0x00 |
| 176-255 | Open for customer use                             | UNUSED | 0x00 |



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