

# DTM64430A

## 4GB - 240-Pin 1Rx8 Registered ECC DDR3 DIMM



### Identification

DTM64430A 512Mx72  
 4GB 1Rx8 PC3-14900R-13-11-A1

### Performance range

Clock / Module Speed / CL-t<sub>RCD</sub> -t<sub>RP</sub>

933 MHz / PC3-14900 / 13-13-13  
 800 MHz / PC3-12800 / 11-11-11  
 667 MHz / PC3-10600 / 10-10-10  
 667 MHz / PC3-10600 / 9-9-9  
 533 MHz / PC3-8500 / 8-8-8  
 533 MHz / PC3-8500 / 7-7-7  
 400 MHz / PC3-6400 / 6-6-6

### Features

240-pin JEDEC-compliant DIMM, 133.35mm wide by 30mm high  
 Operating Voltage: V<sub>DD</sub> = V<sub>DDQ</sub> = +1.5V ±0.075V

I/O Type: SSTL\_15

On-board I<sup>2</sup>C temperature sensor with integrated serial presence-detect (SPD) EEPROM

Data Transfer Rate: 14.9 Gigabytes/sec

Data Bursts: 8 and burst chop 4 mode

ZQ Calibration for Output Driver and On-Die Termination (ODT)

Programmable ODT / Dynamic ODT during Writes

Programmable CAS Latency: 6, 7, 8, 9, 10, 11 and 13

Bi-Directional Differential Data Strobe signals

SDRAM Addressing (Row/Col/Bank): 16/10/3

Fully RoHS Compliant

### Description

DTM64430A is a registered 512Mx72 memory module, which conforms to JEDEC's DDR3-1866, PC3-14900 standard. The assembly is a Single-Rank and comprised of nine Hynix 512Mx8 DDR3 SDRAMs.

One 2K-bit EEPROM is used for Serial Presence Detect and a combination register/PLL, with Address and Command Parity, is also used.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals in a Fly-by topology.

A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.

### Pin Configuration

### Pin Description

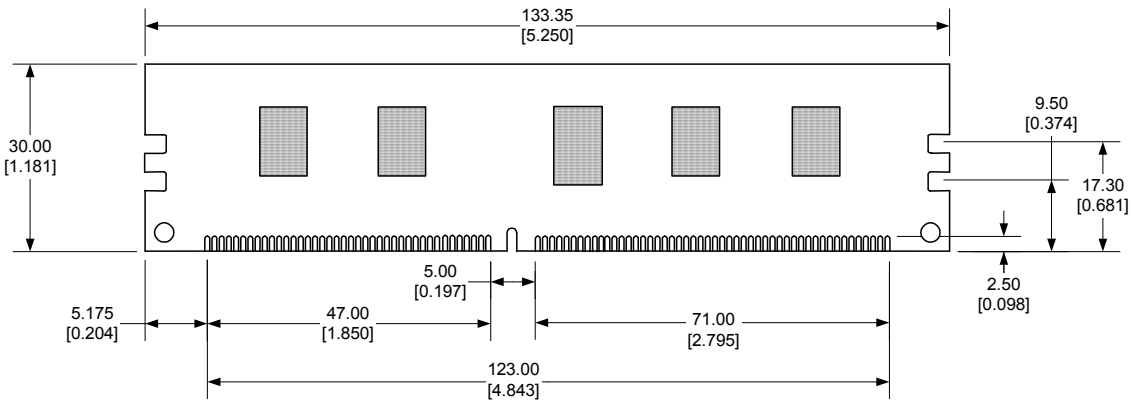
Front Side				Back Side				Name	Function
1 V <sub>REFDQ</sub>	31 DQ25	61 A2	91 DQ41	121 V <sub>SS</sub>	151 V <sub>SS</sub>	181 A1	211 V <sub>SS</sub>	CB[7:0]	Data Check Bits
2 V <sub>SS</sub>	32 V <sub>SS</sub>	62 V <sub>DD</sub>	92 V <sub>SS</sub>	122 DQ4	152 DM3	182 V <sub>DD</sub>	212 DM5	DQ[63:0]	Data Bits
3 DQ0	33 /DQS3	63 CK1**	93 /DQS5	123 DQ5	153 /TDQS12	183 V <sub>DD</sub>	213 /TDQS14	DQS[8:0], /DQS[8:0]	Differential Data Strobes
4 DQ1	34 DQS3	64 /CK1**	94 DQS5	124 V <sub>SS</sub>	154 V <sub>SS</sub>	184 CK0	214 V <sub>SS</sub>	DM[8:0]	Data Mask
5 V <sub>SS</sub>	35 V <sub>SS</sub>	65 V <sub>DD</sub>	95 V <sub>SS</sub>	125 DM0	155 DQ30	185 /CK0	215 DQ46	/TDQS[17:9]	Termination strobes
6 /DQS0	36 DQ26	66 V <sub>DD</sub>	96 DQ42	126 /TDQS9	156 DQ31	186 V <sub>DD</sub>	216 DQ47	CK[1:0], /CK[1:0]	Differential Clock Inputs
7 DQS0	37 DQ27	67 V <sub>REFCA</sub>	97 DQ43	127 V <sub>SS</sub>	157 V <sub>SS</sub>	187 /EVENT	217 V <sub>SS</sub>	CKE[1:0]	Clock Enables
8 V <sub>SS</sub>	38 V <sub>SS</sub>	68 PAR <sub>IN</sub>	98 V <sub>SS</sub>	128 DQ6	158 CB4	188 A0	218 DQ52	/CAS	Column Address Strobe
9 DQ2	39 CB0	69 V <sub>DD</sub>	99 DQ48	129 DQ7	159 CB5	189 V <sub>DD</sub>	219 DQ53	/RAS	Row Address Strobe
10 DQ3	40 CB1	70 A10/AP	100 DQ49	130 V <sub>SS</sub>	160 V <sub>SS</sub>	190 BA1	220 V <sub>SS</sub>	/S[3:0]	Chip Selects
11 V <sub>SS</sub>	41 V <sub>SS</sub>	71 BA0	101 V <sub>SS</sub>	131 DQ12	161 DM8	191 V <sub>DD</sub>	221 DM6	/WE	Write Enable
12 DQ8	42 /DQS8	72 V <sub>DD</sub>	102 /DQS6	132 DQ13	162 /TDQS17	192 /RAS	222 /TDQS15	A[15:0]	Address Inputs
13 DQ9	43 DQS8	73 /WE	103 DQS6	133 V <sub>SS</sub>	163 V <sub>SS</sub>	193 /S0	223 V <sub>SS</sub>	BA[2:0]	Bank Addresses
14 V <sub>SS</sub>	44 V <sub>SS</sub>	74 /CAS	104 V <sub>SS</sub>	134 DM1	164 CB6	194 V <sub>DD</sub>	224 DQ54	ODT[1:0]	On Die Termination Inputs
15 /DQS1	45 CB2	75 V <sub>DD</sub>	105 DQ50	135 /TDQS10	165 CB7	195 OD0	225 DQ55	SA[2:0]	SPD Address
16 DQS1	46 CB3	76 /S1**	106 DQ51	136 V <sub>SS</sub>	166 V <sub>SS</sub>	196 A13	226 V <sub>SS</sub>	SCL	SPD Clock Input
17 V <sub>SS</sub>	47 V <sub>SS</sub>	77 ODT1**	107 V <sub>SS</sub>	137 DQ14	167 NC (TEST)	197 V <sub>DD</sub>	227 DQ60	SDA	SPD Data Input/Output
18 DQ10	48 V <sub>TT</sub>	78 V <sub>DD</sub>	108 DQ56	138 DQ15	168 /RESET	198 /S3, NC**	228 DQ61	/EVENT	Temperature Sensing
19 DQ11	49 V <sub>TT</sub>	79 /S2, NC**	109 DQ57	139 V <sub>SS</sub>	169 CKE1**	199 V <sub>SS</sub>	229 V <sub>SS</sub>	/RESET	Reset for register and DRAMs
20 V <sub>SS</sub>	50 CKE0	80 V <sub>SS</sub>	110 V <sub>SS</sub>	140 DQ20	170 V <sub>DD</sub>	200 DQ36	230 DM7	PAR <sub>IN</sub>	Parity bit for Addr/Ctrl
21 DQ16	51 V <sub>DD</sub>	81 DQ32	111 /DQS7	141 DQ21	171 A15	201 DQ37	231 /TDQS16	/ERR_OUT	Error bit for Parity Error
22 DQ17	52 BA2	82 DQ33	112 DQS7	142 V <sub>SS</sub>	172 A14	202 V <sub>SS</sub>	232 V <sub>SS</sub>	A12/BC	Combination input: Addr12/Burst Chop
23 V <sub>SS</sub>	53 /E <sub>PR_OUT</sub>	83 V <sub>SS</sub>	113 V <sub>SS</sub>	143 DM2	173 V <sub>DD</sub>	203 DM4	233 DQ62	A10/AP	Combination input: Addr10/Auto-precharge
24 /DQS2	54 V <sub>DD</sub>	84 /DQS4	114 DQ58	144 /TDQS11	174 A12/BC	204 /TDQS13	234 DQ63	V <sub>SS</sub>	Ground
25 DQS2	55 A11	85 DQS4	115 DQ59	145 V <sub>SS</sub>	175 A9	205 V <sub>SS</sub>	235 V <sub>SS</sub>	V <sub>DD</sub>	Power
26 V <sub>SS</sub>	56 A7	86 V <sub>SS</sub>	116 V <sub>SS</sub>	146 DQ22	176 V <sub>DD</sub>	206 DQ38	236 V <sub>DDSPD</sub>	V <sub>DDSPD</sub>	SPD EEPROM Power
27 DQ18	57 V <sub>DD</sub>	87 DQ34	117 SA0	147 DQ23	177 A8	207 DQ39	237 SA1	V <sub>REFDQ</sub>	Reference Voltage for DQ's
28 DQ19	58 A5	88 DQ35	118 SCL	148 V <sub>SS</sub>	178 A6	208 V <sub>SS</sub>	238 SDA	V <sub>REFCA</sub>	Reference Voltage for CA
29 V <sub>SS</sub>	59 A4	89 V <sub>SS</sub>	119 SA2	149 DQ28	179 V <sub>DD</sub>	209 DQ44	239 V <sub>SS</sub>	V <sub>TT</sub>	Termination Voltage
30 DQ24	60 V <sub>DD</sub>	90 DQ40	120 V <sub>TT</sub>	150 DQ29	180 A3	210 DQ45	240 V <sub>TT</sub>	NC	No Connection

\*\* Not used

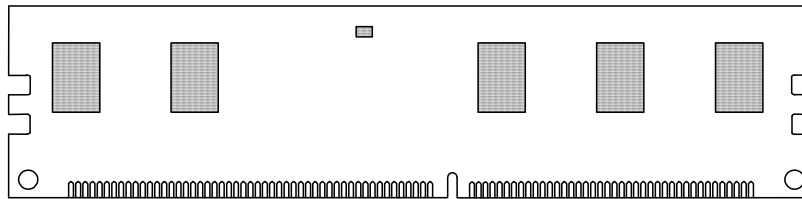
# DTM64430A

4GB - 240-Pin 1Rx8 Registered ECC DDR3 DIMM

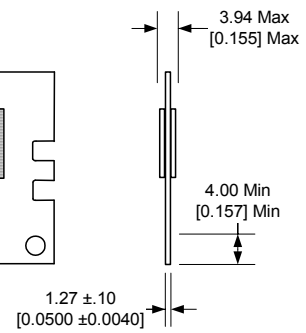
## Front view



## Back view



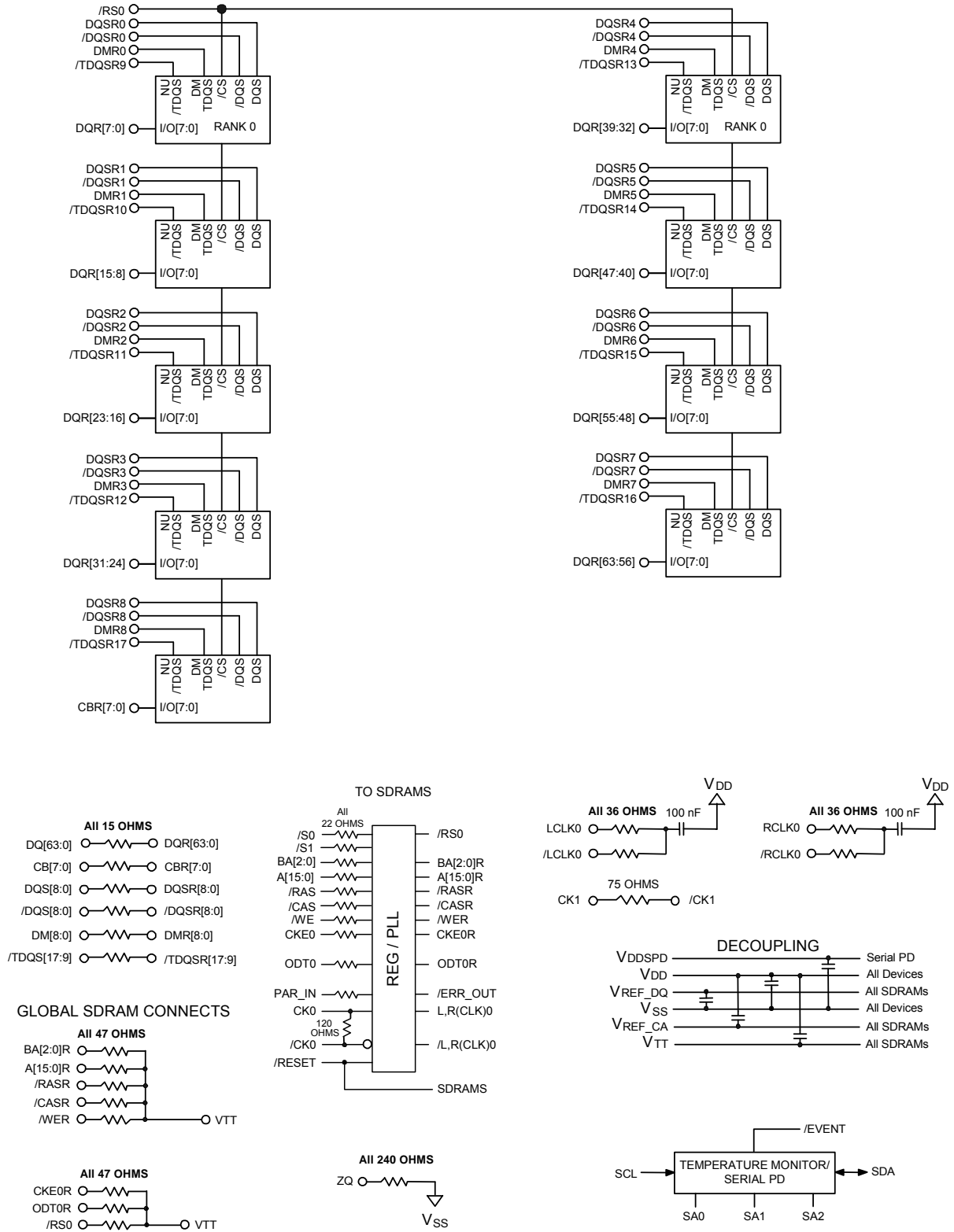
## Side view



## Notes

Tolerances on all dimensions except where otherwise indicated are  $\pm 0.13$  (.005).

All dimensions are expressed: millimeters [inches]



### Absolute Maximum Ratings

(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	T <sub>STORAGE</sub>	-55	100	C
Ambient Temperature, Operating	T <sub>A</sub>	0	70	C
DRAM Case Temperature, Operating	T <sub>CASE</sub>	0	95	C
Voltage on V <sub>DD</sub> relative to V <sub>SS</sub>	V <sub>DD</sub>	-0.4	1.975	V
Voltage on Any Pin relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.4	1.975	V

Notes:

DRAM Operating Case Temperature above 85C requires 2X refresh.

### Recommended DC Operating Conditions (T<sub>A</sub> = 0 to 70 C, Voltage referenced to V<sub>SS</sub> = 0 V)

PARAMETER	Symbol	Operation Voltage	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V <sub>DD</sub>	1.5V	1.425	1.5	1.575	V	
I/O Reference Voltage	V <sub>REFDQ</sub>	1.5V	0.49 V <sub>DD</sub>	0.50 V <sub>DD</sub>	0.51 V <sub>DD</sub>	V	1
I/O Reference Voltage	V <sub>REFCA</sub>	1.5V		0.50 V <sub>DD</sub>	0.51 V <sub>DD</sub>	V	1

Notes:

1. For Reference V<sub>DD</sub>/2 ± 15 mV. The value of VREF is expected to equal one-half VDD and to track variations in the VDD DC level. Peak-to-peak noise on VREF may not exceed ±1% of its DC value. For Reference: VREF = VDD/2 ± 15 mV.

### DC Input Logic Levels, Single-Ended (T<sub>A</sub> = 0 to 70 C, Voltage referenced to V<sub>SS</sub> = 0 V)

PARAMETER	Symbol	Operation Voltage	Minimum	Maximum	Unit
Logical High (Logic 1)	V <sub>IH(DC)</sub>	1.5V	V <sub>REF</sub> + 0.1	V <sub>DD</sub>	V
Logical Low (Logic 0)	V <sub>IL(DC)</sub>	1.5V	V <sub>SS</sub>	V <sub>REF</sub> - 0.1	V

### AC Input Logic Levels, Single-Ended (T<sub>A</sub> = 0 to 70 C, Voltage referenced to V<sub>SS</sub> = 0 V)

PARAMETER	Symbol	Operation Voltage	Minimum	Maximum	Unit
Logical High (Logic 1)	V <sub>IH(AC)</sub>	1.5V	V <sub>REF</sub> + 0.175	-	V
Logical Low (Logic 0)	V <sub>IL(AC)</sub>	1.5V	-	V <sub>REF</sub> - 0.175	V

### Differential Input Logic Levels ( $T_A = 0$ to $70$ C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Differential Input Logic High	$V_{IH,DIFF}$	+0.200	DC: $V_{DD}$ AC: $V_{DD}+0.4$	V
Differential Input Logic Low	$V_{IL,DIFF}$	DC: $V_{SS}$ AC: $V_{SS}-0.4$	-0.200	V
Differential Input Cross Point Voltage relative to $V_{DD}/2$	$V_{IX}$	- 0.150	+ 0.150	V

### Capacitance ( $T_A = 25$ C, $f = 100$ MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK0, /CK0	$C_{CK}$	1.5	2.5	pF
Input Capacitance, Address	BA[2:0], A[15:0], /RAS, /CAS, /WE	$C_i$	1.5	2.5	pF
Input Capacitance Control	/S0, CKE0, ODT0	$C_i$	1.5	2.5	pF
Input/Output Capacitance	DQ[63:0], CB[7:0] DQS[8:0], /DQS[8:0], DM[8:0], /TDQS[17:9]	$C_{IO}$	1.5	2.5	pF

### DC Characteristics ( $T_A = 0$ to $70$ C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input $0$ V < $V_{IN}$ < $V_{DD}$ )	$I_{IL}$	-18	+18	$\mu$ A	1,2
Output Leakage Current ( $0$ V < $V_{OUT}$ < $V_{DDQ}$ )	$I_{OL}$	-10	+10	$\mu$ A	2,3

Notes:

- 1) All other pins not under test = 0 V
- 2) Values are shown per pin
- 3) DQ, DQS, DQS and ODT are disabled

**I<sub>DD</sub> Specifications and Conditions** (T<sub>A</sub> = 0 to 70 C, Voltage referenced to V<sub>SS</sub> = 0 V)

PARAMETER	Symbol	Test Condition	Max Value	Unit
Operating One Bank Active-Precharge Current	I <sub>DD0</sub>	Operating current : One bank ACTIVATE-to-PRECHARGE	351	mA
Operating One Bank Active-Read-Precharge Current	I <sub>DD1</sub>	Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE	432	mA
Precharge Power-Down Current	I <sub>DD2P</sub>	Precharge power down current: (Slow exit)	99	mA
Precharge Power-Down Current	I <sub>DD2P</sub>	Precharge power down current: (Fast exit)	126	mA
Precharge Quiet Standby Current	I <sub>DD2Q</sub>	Precharge quiet standby current	189	mA
Precharge Standby Current	I <sub>DD2N</sub>	Precharge standby current	198	mA
Active Power-Down Current	I <sub>DD3P</sub>	Active power-down current	189	mA
Active Standby Current	I <sub>DD3N</sub>	Active standby current	288	mA
Operating Burst Write Current	I <sub>DD4W</sub>	Burst write operating current	1035	mA
Operating Burst Read Current	I <sub>DD4R</sub>	Burst read operating current	990	mA
Burst Refresh Current	I <sub>DD5</sub>	Refresh current	1800	mA
Self Refresh Current	I <sub>DD6</sub>	Self-refresh temperature current: MAX T <sub>C</sub> = 85°C	135	mA
Operating Bank Interleave Read Current	I <sub>DD7</sub>	All bank interleaved read current	1440	mA

### AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	$t_{AA}$	13.125	20	ns
CAS-to-CAS Command Delay	$t_{CCD}$	4	-	$t_{CK}$
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	$t_{CK}$
Clock Cycle Time	$t_{CK}$	1.07	1.875	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	$t_{CK}$
Data Input Hold Time after DQS Strobe	$t_{DH}$	-	-	ps
DQ Input Pulse Width	$t_{DIPW}$	320	-	ps
DQS Output Access Time from Clock	$t_{DQSCK}$	-195	+195	ps
Write DQS High Level Width	$t_{DQSH}$	0.45	0.55	$t_{CK(avg)}$
Write DQS Low Level Width	$t_{DQSL}$	0.45	0.55	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	$t_{DQSQ}$	-	85	ps
Data Input Setup Time Before DQS Strobe	$t_{DS}$	-	-	ps
DQS Falling Edge from Clock, Hold Time	$t_{DSH}$	0.18	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	$t_{DSS}$	0.18	-	$t_{CK(avg)}$
Clock Half Period	$t_{HP}$	minimum of $t_{CH}$ or $t_{CL}$	-	ns
Address and Command Hold Time after Clock	$t_{IH}$	100	-	ps
Address and Command Setup Time before Clock	$t_{IS}$	-	-	ps
Load Mode Command Cycle Time	$t_{MRD}$	4	-	$t_{CK}$
DQ-to-DQS Hold	$t_{QH}$	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	$t_{RAS}$	34	$9 \cdot t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	$t_{RC}$	47.125	-	ns
RAS-to-CAS Delay	$t_{RCD}$	13.125	-	ns
Average Periodic Refresh Interval $0^{\circ}C \leq T_{CASE} < 85^{\circ}C$	$t_{REFI}$	-	7.8	$\mu s$
Average Periodic Refresh Interval $0^{\circ}C \leq T_{CASE} < 95^{\circ}C$	$t_{REFI}$	-	3.9	$\mu s$
Auto Refresh Row Cycle Time	$t_{RFC}$	260	-	ns
Row Precharge Time	$t_{RP}$	13.125	-	ns
Read DQS Preamble Time	$t_{RPRE}$	0.9	Note-1	$t_{CK(avg)}$
Read DQS Postamble Time	$t_{RPST}$	0.3	Note-2	$t_{CK(avg)}$
Row Active to Row Active Delay	$t_{RRD}$	Max(4nCK, 5ns)	-	ns
Internal Read to Precharge Command Delay	$t_{RTP}$	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	$t_{WPRE}$	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	$t_{WPST}$	0.3	-	$t_{CK(avg)}$
Write Recovery Time	$t_{WR}$	15	-	ns
Internal Write to Read Command Delay	$t_{WTR}$	Max(4nCK, 7.5ns)	-	ns

Notes:

1. The maximum preamble is bound by  $t_{LZDQS}(\min)$
2. The maximum postamble is bound by  $t_{HZDQS}(\max)$



# DTM64430A

4GB - 240-Pin 1Rx8 Registered ECC DDR3 DIMM

---



DATARAM CORPORATION, USA Corporate Headquarters, P.O. Box 7528, Princeton, NJ 08543-7528;  
Voice: 609-799-0071, Fax: 609-799-6734; [www.dataram.com](http://www.dataram.com)

All rights reserved.

The information contained in this document has been carefully checked and is believed to be reliable. However, Dataram assumes no responsibility for inaccuracies.

The information contained in this document does not convey any license under the copyrights, patent rights or trademarks claimed and owned by Dataram.

No part of this publication may be copied or reproduced in any form or by any means, or transferred to any third party without prior written consent of Dataram.