

DTM64401C

16GB - 240-Pin 2Rx4 Registered ECC LV DDR3 DIMM



Identification

DTM64401C 2Gx72
 16GB 2Rx4 PC3L-12800R-11-11-E2

Performance range

Clock / Module Speed / CL-t_{RCD}-t_{RP}

800 MHz / PC3L-12800 / 11-11-11
 667 MHz / PC3L-10600 / 10-10-10
 667 MHz / PC3L-10600 / 9-9-9
 533 MHz / PC3L-8500 / 8-8-8
 533 MHz / PC3L-8500 / 7-7-7
 400 MHz / PC3L-6400 / 6-6-6

Features

240-pin JEDEC-compliant DIMM, 133.35 mm wide by 30 mm high

Operating Voltage: V_{DD} = V_{DDQ} = +1.35V (1.283V to 1.45V)

Backward-compatible to V_{DD} = V_{DDQ} = +1.5V ±0.075V

I/O Type: SSTL_15

On-board I²C temperature sensor with integrated Serial Presence-Detect (SPD) EEPROM

Data Transfer Rate: 12.8 Gigabytes/sec

Data Bursts: 8 and burst chop 4 mode

ZQ Calibration for Output Driver and On-Die Termination (ODT)

Programmable ODT / Dynamic ODT during Writes

Programmable CAS Latency: 6, 7, 8, 9, 10, and 11

Bi-directional Differential Data Strobe signals

SDRAM Addressing (Row/Col/Bank): 16/11/3

Fully RoHS Compliant

Description

DTM64401C is a registered 2Gx72 memory module, which conforms to the JEDEC PC3L-12800 standard. The assembly is Dual-Rank. Each Rank is comprised of eighteen Samsung 1Gx4 DDR3L-1600 SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect and a combination register/PLL, with Address and Command Parity, is also used.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals in a Fly-by topology. A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.

Pin Configuration

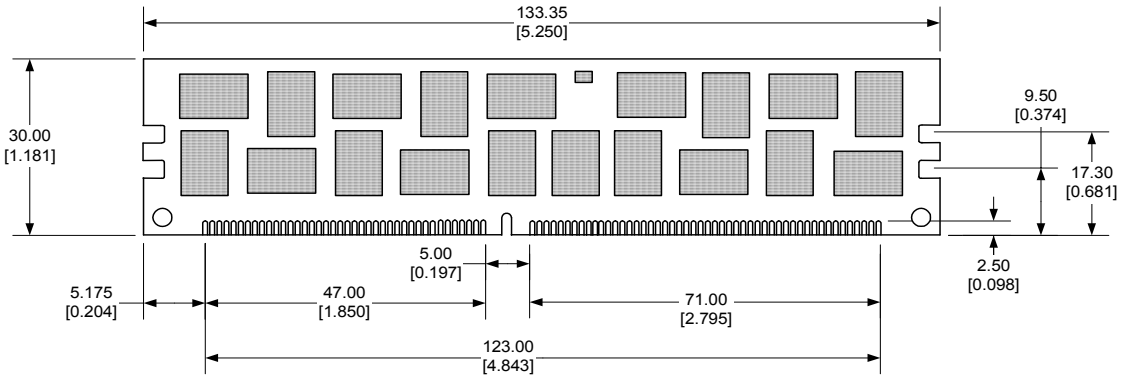
Pin Description

Front Side				Back Side				Name	Function
1 V _{REFDQ}	31 DQ25	61 A2	91 DQ41	121 V _{SS}	151 V _{SS}	181 A1	211 V _{SS}	CB[7:0]	Data Check Bits
2 V _{SS}	32 V _{SS}	62 V _{DD}	92 V _{SS}	122 DQ4	152 DQS12	182 V _{DD}	212 DQS14	DQ[63:0]	Data Bits
3 DQ0	33 /DQS3	63 CK1*	93 /DQS5	123 DQ5	153 /DQS12	183 V _{DD}	213 /DQS14	DQS[17:0], /DQS[17:0]	Differential Data Strobes
4 DQ1	34 DQS3	64 /CK1*	94 DQS5	124 V _{SS}	154 V _{SS}	184 CK0	214 V _{SS}	CK[1:0], /CK[1:0]	Differential Clock Inputs
5 V _{SS}	35 V _{SS}	65 V _{DD}	95 V _{SS}	125 DQS9	155 DQ30	185 /CK0	215 DQ46	CKE[1:0]	Clock Enables
6 /DQS0	36 DQ26	66 V _{DD}	96 DQ42	126 /DQS9	156 DQ31	186 V _{DD}	216 DQ47	/CAS	Column Address Strobe
7 DQS0	37 DQ27	67 V _{REFCA}	97 DQ43	127 V _{SS}	157 V _{SS}	187 /EVENT	217 V _{SS}	/RAS	Row Address Strobe
8 V _{SS}	38 V _{SS}	68 PAR_IN	98 V _{SS}	128 DQ6	158 CB4	188 A0	218 DQ52	/S[3:0]	Chip Selects
9 DQ2	39 CB0	69 V _{DD}	99 DQ48	129 DQ7	159 CB5	189 V _{DD}	219 DQ53	/WE	Write Enable
10 DQ3	40 CB1	70 A10/AP	100 DQ49	130 V _{SS}	160 V _{SS}	190 BA1	220 V _{SS}	A[15:0]	Address Inputs
11 V _{SS}	41 V _{SS}	71 BA0	101 V _{SS}	131 DQ12	161 DQS17	191 V _{DD}	221 DQS15	BA[2:0]	Bank Addresses
12 DQ8	42 /DQS8	72 V _{DD}	102 /DQS6	132 DQ13	162 /DQS17	192 /RAS	222 /DQS15	ODT[1:0]	On Die Termination Inputs
13 DQ9	43 DQS8	73 /WE	103 DQS6	133 V _{SS}	163 V _{SS}	193 /S0	223 V _{SS}	SA[2:0]	SPD Address
14 V _{SS}	44 V _{SS}	74 /CAS	104 V _{SS}	134 DQS10	164 CB6	194 V _{DD}	224 DQ54	SCL	SPD Clock Input
15 /DQS1	45 CB2	75 V _{DD}	105 DQ50	135 /DQS10	165 CB7	195 ODT0	225 DQ55	SDA	SPD Data Input/Output
16 DQS1	46 CB3	76 /S1	106 DQ51	136 V _{SS}	166 V _{SS}	196 A13	226 V _{SS}	/EVENT	Temperature Sensing
17 V _{SS}	47 V _{SS}	77 ODT1	107 V _{SS}	137 DQ14	167 NC (TEST)	197 V _{DD}	227 DQ60	/RESET	Reset for register and DRAMs
18 DQ10	48 V _{TT}	78 V _{DD}	108 DQ56	138 DQ15	168 /RESET	198 /S3, NC	228 DQ61	PAR_IN	Parity bit for Addr/Ctrl
19 DQ11	49 V _{TT}	79 /S2, NC	109 DQ57	139 V _{SS}	169 CKE1	199 V _{SS}	229 V _{SS}	/ERR_OUT	Error bit for Parity Error
20 V _{SS}	50 CKE0	80 V _{SS}	110 V _{SS}	140 DQ20	170 V _{DD}	200 DQ36	230 DQS16	A12/BC	Combination input: Addr12/Burst Chop
21 DQ16	51 V _{DD}	81 DQ32	111 /DQS7	141 DQ21	171 A15	201 DQ37	231 /DQS16	A10/AP	Combination input: Addr10/Auto-precharge
22 DQ17	52 BA2	82 DQ33	112 DQS7	142 V _{SS}	172 A14	202 V _{SS}	232 V _{SS}	V _{SS}	Ground
23 V _{SS}	53 /ERR_OUT	83 V _{SS}	113 V _{SS}	143 DQS11	173 V _{DD}	203 DQS13	233 DQ62	V _{DD}	Power
24 /DQS2	54 V _{DD}	84 /DQS4	114 DQ58	144 /DQS11	174 A12/BC	204 /DQS13	234 DQ63	V _{DDSPD}	SPD EEPROM Power
25 DQS2	55 A11	85 DQS4	115 DQ59	145 V _{SS}	175 A9	205 V _{SS}	235 V _{SS}	V _{REFDQ}	Reference Voltage for DRAM's
26 V _{SS}	56 A7	86 V _{SS}	116 V _{SS}	146 DQ22	176 V _{DD}	206 DQ38	236 V _{DDSPD}	V _{REFCA}	Reference Voltage for CA
27 DQ18	57 V _{DD}	87 DQ34	117 SA0	147 DQ23	177 A8	207 DQ39	237 SA1	V _{TT}	Termination Voltage
28 DQ19	58 A5	88 DQ35	118 SCL	148 V _{SS}	178 A6	208 V _{SS}	238 SDA	NC	No Connection
29 V _{SS}	59 A4	89 V _{SS}	119 SA2	149 DQ28	179 V _{DD}	209 DQ44	239 V _{SS}		* not used
30 DQ24	60 V _{DD}	90 DQ40	120 V _{TT}	150 DQ29	180 A3	210 DQ45	240 V _{TT}		

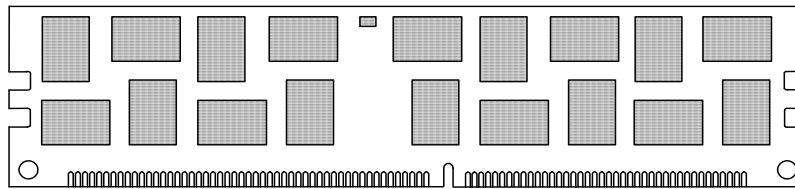
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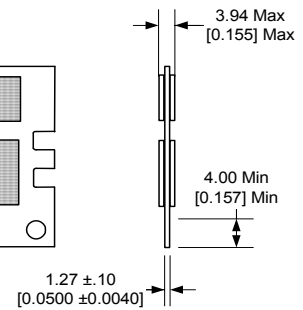
Front view



Back view



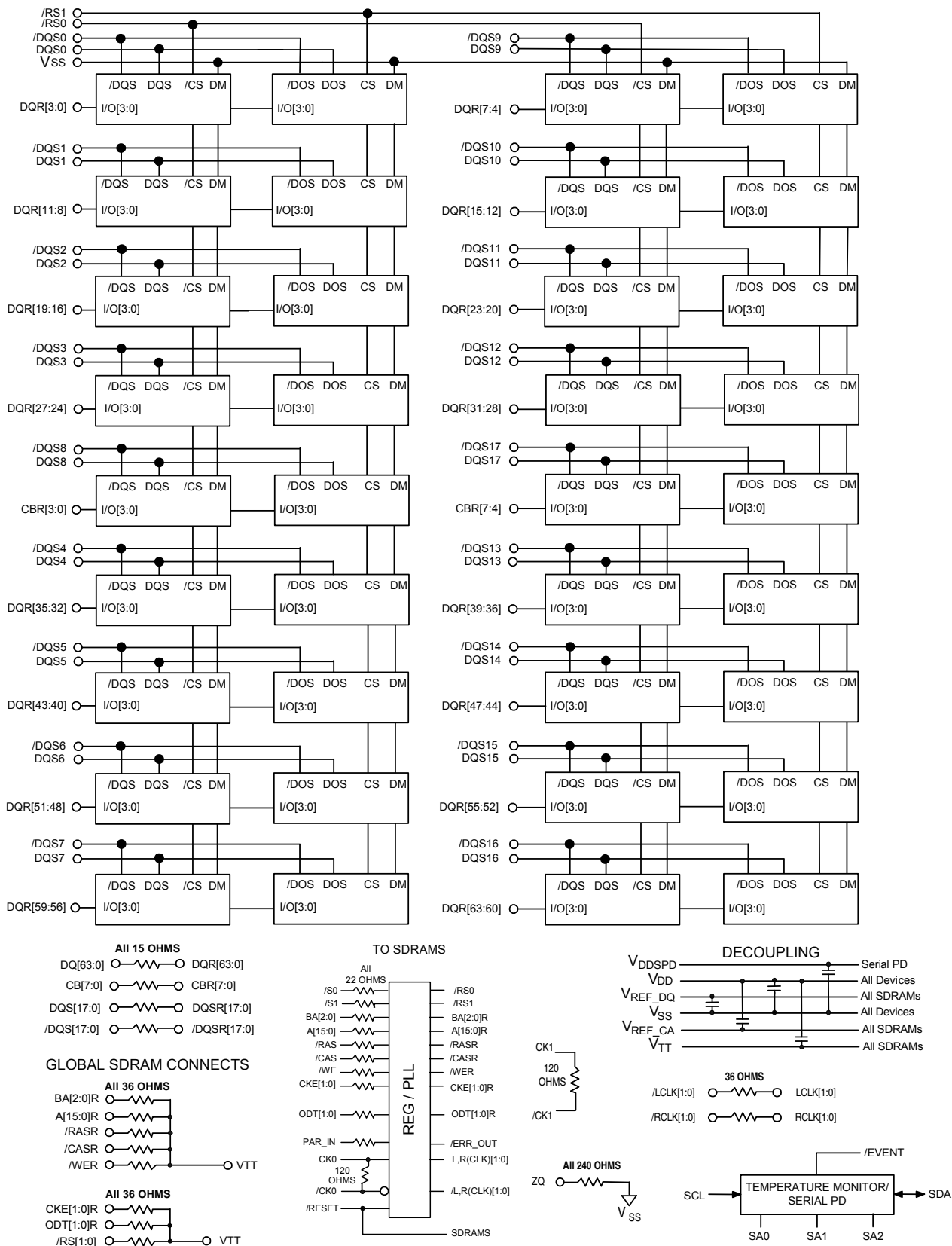
Side view



Notes

Tolerances on all dimensions except where otherwise indicated are ± 0.13 (.005).

All dimensions are expressed: millimeters [inches]



Absolute Maximum Ratings

(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	T _{STORAGE}	-55	100	C
Ambient Temperature, Operating	T _A	0	70	C
DRAM Case Temperature, Operating	T _{CASE}	0	95	C
Voltage on V _{DD} relative to V _{SS}	V _{DD}	-0.4	1.975	V
Voltage on Any Pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.4	1.975	V

Notes:

DRAM Operating Case Temperature above 85C requires 2X refresh.

Recommended DC Operating Conditions (T_A = 0 to 70 C, Voltage referenced to V_{SS} = 0 V)

PARAMETER	Symbol	Operation Voltage	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V _{DD}	1.35V	1.283	1.35	1.4500	V	
		1.5V	1.425	1.5	1.575		
I/O Reference Voltage	V _{REFDQ}	1.35V	0.49 V _{DD}	0.50 V _{DD}	0.51 V _{DD}	V	1
		1.5V					
I/O Reference Voltage	V _{REFCA}	1.35V	0.49 V _{DD}	0.50 V _{DD}	0.51 V _{DD}	V	1
		1.5V					

Notes:

The value of V_{REF} is expected to equal one-half V_{DD} and to track variations in the V_{DD} DC level. Peak-to-peak noise on V_{REF} may not exceed ±1% of its DC value. For Reference V_{DD}/2 ± 15 mV.

DC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{SS} = 0 V)

PARAMETER	Symbol	Operation Voltage	Minimum	Maximum	Unit
Logical High (Logic 1)	V _{IH(DC)}	1.35V	V _{REF} + 0.09	V _{DD}	V
		1.5V	V _{REF} + 0.1	V _{DD}	
Logical Low (Logic 0)	V _{IL(DC)}	1.35V	V _{SS}	V _{REF} - 0.09	V
		1.5V	V _{SS}	V _{REF} - 0.1	

AC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{SS} = 0 V)

PARAMETER	Symbol	Operation Voltage	Minimum	Maximum	Unit
Logical High (Logic 1)	V _{IH(AC)}	1.35V	V _{REF} + 0.160	-	V
		1.5V	V _{REF} + 0.175	-	
Logical Low (Logic 0)	V _{IL(AC)}	1.35V	-	V _{REF} - 0.160	V
		1.5V	-	V _{REF} - 0.175	

Differential Input Logic Levels ($T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Differential Input Logic High	$V_{IH,DIFF}$	+0.200	DC: V_{DD} AC: $V_{DD}+0.4$	V
Differential Input Logic Low	$V_{IL,DIFF}$	DC: V_{SS} AC: $V_{SS}-0.4$	-0.200	V
Differential Input Cross Point Voltage relative to $V_{DD}/2$	V_{IX}	- 0.150	+ 0.150	V

Capacitance ($T_A = 25$ C, $f = 100$ MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK0, /CK0	C_{CK}	1.5	2.5	pF
Input Capacitance, Address	BA[2:0], A[15:0], /RAS, /CAS, /WE	C_I	1.5	2.5	pF
Input Capacitance Control	/S[1:0], CKE[1:0], ODT[1:0]	C_I	1.5	2.5	pF
Input/Output Capacitance	DQ[63:0], CB[7:0], DQS[17:0], /DQS[17:0].	C_{IO}	3	5	pF

DC Characteristics ($T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input 0 V < V_{IN} < V_{DD})	I_{IL}	-18	+18	μ A	1,2
Output Leakage Current (0 V < V_{OUT} < V_{DDQ})	I_{OL}	-10	+10	μ A	2,3

Notes:

- 1) All other pins not under test = 0 V
- 2) Values are shown per pin
- 3) DQ, DQS, DQS and ODT are disabled

I_{DD} Specifications and Conditions (T_A = 0 to 70 C, Voltage referenced to V_{SS} = 0 V)

PARAMETER	Symbol	Test Condition	Max Value		Unit
			1.35V	1.5V	
Operating One Bank Active-Precharge Current	I _{DD0} *	Operating current : One bank ACTIVATE-to-PRECHARGE	1750	1890	mA
Operating One Bank Active-Read-Precharge Current	I _{DD1} *	Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE	2020	2070	mA
Precharge Power-Down Current	I _{DD2P} **	Precharge power down current: (Slow exit)	1130	1170	mA
Precharge Power-Down Current	I _{DD2P} **	Precharge power down current: (Fast exit)	1130	1170	mA
Precharge Standby Current	I _{DD2N} **	Precharge standby current	1360	1410	mA
Active Power-Down Current	I _{DD3P} **	Active power-down current	1310	1350	mA
Active Standby Current	I _{DD3N} **	Active standby current	1710	1760	mA
Operating Burst Write Current	I _{DD4W} *	Burst write operating current	2650	2800	mA
Operating Burst Read Current	I _{DD4R} *	Burst read operating current	2560	2610	mA
Burst Refresh Current	I _{DD5B} **	Refresh current	3600	3650	mA
Self Refresh Current	I _{DD6} **	Self-refresh temperature current: MAX T _C = 85°C	570	570	mA
Operating Bank Interleave Read Current	I _{DD7} *	All bank interleaved read current	3990	4050	mA

* One module rank in this operation, the rest in IDD2N slow exit.

** All module ranks in this operation.

AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	t_{AA}	13.125	20	ns
CAS-to-CAS Command Delay	t_{CCD}	4	-	t_{CK}
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	t_{CK}
Clock Cycle Time	t_{CK}	1.25	2.500	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	t_{CK}
Data Input Hold Time after DQS Strobe	t_{DH}	45	-	ps
DQ Input Pulse Width	t_{DIPW}	360	-	ps
DQS Output Access Time from Clock	t_{DQSCK}	-225	+225	ps
Write DQS High Level Width	t_{DQSH}	0.45	0.55	$t_{CK(avg)}$
Write DQS Low Level Width	t_{DQSL}	0.45	0.55	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	t_{DQSQ}	-	100	ps
Data Input Setup Time Before DQS Strobe	t_{DS}	10	-	ps
DQS Falling Edge from Clock, Hold Time	t_{DSH}	0.18	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	t_{DSS}	0.18	-	$t_{CK(avg)}$
Clock Half Period	t_{HP}	minimum of t_{CH} or t_{CL}	-	ns
Address and Command Hold Time after Clock	t_{IH}	120	-	ps
Address and Command Setup Time before Clock	t_{IS}	45	-	ps
Load Mode Command Cycle Time	t_{MRD}	4	-	t_{CK}
DQ-to-DQS Hold	t_{QH}	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	t_{RAS}	35	$9 \cdot t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	t_{RC}	48.125	-	ns
RAS-to-CAS Delay	t_{RCD}	13.125	-	ns
Average Periodic Refresh Interval $0^{\circ}C \leq T_{CASE} < 85^{\circ}C$	t_{REFI}	-	7.8	μs
Average Periodic Refresh Interval $0^{\circ}C \leq T_{CASE} < 95^{\circ}C$	t_{REFI}	-	3.9	μs
Auto Refresh Row Cycle Time	t_{RFC}	260	-	ns
Row Precharge Time	t_{RP}	13.125	-	ns
Read DQS Preamble Time	t_{RPRE}	0.9	Note-1	$t_{CK(avg)}$
Read DQS Postamble Time	t_{RPST}	0.3	Note-2	$t_{CK(avg)}$
Row Active to Row Active Delay	t_{RRD}	Max(4nCK, 6ns)	-	ns
Internal Read to Precharge Command Delay	t_{RTP}	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	t_{WPRE}	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	t_{WPST}	0.3	-	$t_{CK(avg)}$
Write Recovery Time	t_{WR}	15	-	ns
Internal Write to Read Command Delay	t_{WTR}	Max(4nCK, 7.5ns)	-	ns

Notes:

1. The maximum preamble is bound by $t_{LZDQS}(\min)$
2. The maximum postamble is bound by $t_{HZDQS}(\max)$



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