



### Identification

DTM64379A 512Mx64  
4GB 2Rx8 PC3-12800U-11-11-B1

### Performance range

Clock / Module Speed / CL-t<sub>RCD</sub> -t<sub>RP</sub>

800 MHz / PC3-12800 / 11-11-11  
667 MHz / PC3-10600 / 10-10-10  
667 MHz / PC3-10600 / 9-9-9  
533 MHz / PC3-8500 / 8-8-8  
533 MHz / PC3-8500 / 7-7-7  
400 MHz / PC3-6400 / 6-6-6

### Features

240-pin JEDEC-compliant DIMM, 133.35 mm wide by 30 mm high

Operating Voltage: 1.5 V ±0.075 V

I/O Type: SSTL\_15

Data Transfer Rate: 12.8 Gigabytes/sec

Data Bursts: 8 and burst chop 4 mode

ZQ Calibration for Output Driver and On-Die Termination (ODT)

Programmable ODT / Dynamic ODT during Writes

Programmable CAS Latency: 6, 7, 8, 9, 10 and 11

Differential Data Strobe signals

SDRAM Addressing (Row/Col/Bank): 15/10/3

Fully RoHS Compliant

### Description

DTM64379A is an Unbuffered 512Mx64 memory module, which conforms to JEDEC's DDR3, PC3-12800 standard. The assembly is Dual-Rank. Each Rank consists of eight 256Mx8 DDR3 Samsung SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals.

### Pin Configuration

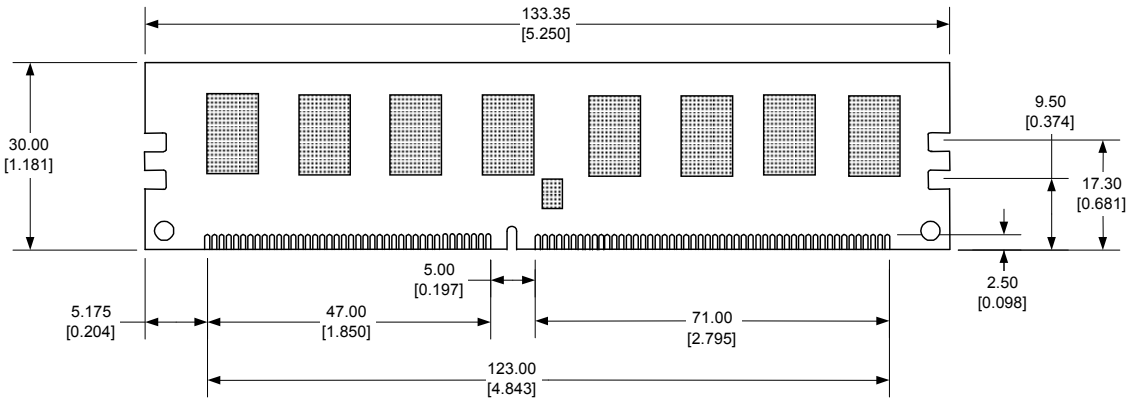
Front Side				Back Side				Pin Description	
Name	Function	Name	Function	Name	Function	Name	Function	Name	Function
1 V <sub>REFDQ</sub>	31 DQ25	61 A2	91 DQ41	121 V <sub>SS</sub>	151 V <sub>SS</sub>	181 A1	211 V <sub>SS</sub>	CB[7:0]	Data Check Bits
2 V <sub>SS</sub>	32 V <sub>SS</sub>	62 V <sub>DD</sub>	92 V <sub>SS</sub>	122 DQ4	152 DM3	182 V <sub>DD</sub>	212 DM5	DQ[63:0]	Data Bits
3 DQ0	33 /DQS3	63 CK1	93 /DQS5	123 DQ5	153 NC	183 V <sub>DD</sub>	213 NC	DQS[8:0], /DQS[8:0]	Differential Data Strobes
4 DQ1	34 DQS3	64 /CK1	94 DQS5	124 V <sub>SS</sub>	154 V <sub>SS</sub>	184 CK0	214 V <sub>SS</sub>	DM[8:0]	Data Mask
5 V <sub>SS</sub>	35 V <sub>SS</sub>	65 V <sub>DD</sub>	95 V <sub>SS</sub>	125 DM0	155 DQ30	185 /CK0	215 DQ46	CK[1:0], /CK[1:0]	Differential Clock Inputs
6 /DQS0	36 DQ26	66 V <sub>DD</sub>	96 DQ42	126 NC	156 DQ31	186 V <sub>DD</sub>	216 DQ47	CKE[1:0]	Clock Enables
7 DQS0	37 DQ27	67 V <sub>REFCA</sub>	97 DQ43	127 V <sub>SS</sub>	157 V <sub>SS</sub>	187 /Event, NC	217 V <sub>SS</sub>	/CAS	Column Address Strobe
8 V <sub>SS</sub>	38 V <sub>SS</sub>	68 NC	98 V <sub>SS</sub>	128 DQ6	158 CB4, NC*	188 A0	218 DQ52	/RAS	Row Address Strobe
9 DQ2	39 CB0, NC*	69 VDD	99 DQ48	129 DQ7	159 CB5, NC*	189 V <sub>DD</sub>	219 DQ53	/S[3:0]	Chip Selects
10 DQ3	40 CB1, NC*	70 A10/AP	100 DQ49	130 V <sub>SS</sub>	160 V <sub>SS</sub>	190 BA1	220 V <sub>SS</sub>	/WE	Write Enable
11 V <sub>SS</sub>	41 V <sub>SS</sub>	71 BA0	101 V <sub>SS</sub>	131 DQ12	161 DM8, NC*	191 V <sub>DD</sub>	221 DM6	A[15:0]	Address Inputs
12 DQ8	42 /DQS8*	72 V <sub>DD</sub>	102 /DQS6	132 DQ13	162 NC	192 /RAS	222 NC	BA[2:0]	Bank Addresses
13 DQ9	43 DQS8*	73 /WE	103 DQS6	133 V <sub>SS</sub>	163 V <sub>SS</sub>	193 /S0	223 V <sub>SS</sub>	ODT[1:0]	On Die Termination Inputs
14 V <sub>SS</sub>	44 V <sub>SS</sub>	74 /CAS	104 V <sub>SS</sub>	134 DM1	164 CB6, NC*	194 V <sub>DD</sub>	224 DQ54	SA[2:0]	SPD Address
15 /DQS1	45 CB2, NC*	75 V <sub>DD</sub>	105 DQ50	135 NC	165 CB7, NC*	195 ODT0	225 DQ55	SCL	SPD Clock Input
16 DQS1	46 CB3, NC*	76 /S1	106 DQ51	136 V <sub>SS</sub>	166 V <sub>SS</sub>	196 A13	226 V <sub>SS</sub>	SDA	SPD Data Input/Output
17 V <sub>SS</sub>	47 V <sub>SS</sub>	77 ODT1	107 V <sub>SS</sub>	137 DQ14	167 NC (TEST)	197 V <sub>DD</sub>	227 DQ60	/EVENT	Temperature Sensing
18 DQ10	48 V <sub>TT</sub>	78 V <sub>DD</sub>	108 DQ56	138 DQ15	168 /RESET	198 /S3, NC*	228 DQ61	/RESET	Reset for DRAMs
19 DQ11	49 V <sub>TT</sub>	79 /S2, NC*	109 DQ57	139 V <sub>SS</sub>	169 CKE1	199 V <sub>SS</sub>	229 V <sub>SS</sub>	A12/BC	Combination input: Addr12/Burst Chop
20 V <sub>SS</sub>	50 CKE0	80 V <sub>SS</sub>	110 V <sub>SS</sub>	140 DQ20	170 V <sub>DD</sub>	200 DQ36	230 DM7	A10/AP	Combination input: Addr10/Auto-precharge
21 DQ16	51 V <sub>DD</sub>	81 DQ32	111 /DQS7	141 DQ21	171 A15 *	201 DQ37	231 NC	V <sub>SS</sub>	Ground
22 DQ17	52 BA2	82 DQ33	112 DQS7	142 V <sub>SS</sub>	172 A14	202 V <sub>SS</sub>	232 V <sub>SS</sub>	V <sub>DD</sub>	Power
23 V <sub>SS</sub>	53 NC	83 V <sub>SS</sub>	113 V <sub>SS</sub>	143 DM2	173 V <sub>DD</sub>	203 DM4	233 DQ62	V <sub>DDSPD</sub>	SPD EEPROM Power
24 /DQS2	54 V <sub>DD</sub>	84 /DQS4	114 DQ58	144 NC	174 A12 /BC	204 NC	234 DQ63	V <sub>REFDQ</sub>	Reference Voltage for DQ's
25 DQS2	55 A11	85 DQS4	115 DQ59	145 V <sub>SS</sub>	175 A9	205 V <sub>SS</sub>	235 V <sub>SS</sub>	V <sub>REFCA</sub>	Reference Voltage for CA
26 V <sub>SS</sub>	56 A7	86 V <sub>SS</sub>	116 V <sub>SS</sub>	146 DQ22	176 V <sub>DD</sub>	206 DQ38	236 V <sub>DDSPD</sub>	V <sub>TT</sub>	Termination Voltage
27 DQ18	57 V <sub>DD</sub>	87 DQ34	117 SA0	147 DQ23	177 A8	207 DQ39	237 SA1	NC	No Connection
28 DQ19	58 A5	88 DQ35	118 SCL	148 V <sub>SS</sub>	178 A6	208 V <sub>SS</sub>	238 SDA		
29 V <sub>SS</sub>	59 A4	89 V <sub>SS</sub>	119 SA2	149 DQ28	179 V <sub>DD</sub>	209 DQ44	239 V <sub>SS</sub>		
30 DQ24	60 V <sub>DD</sub>	90 DQ40	120 V <sub>TT</sub>	150 DQ29	180 A3	210 DQ45	240 V <sub>TT</sub>		

\* Not used

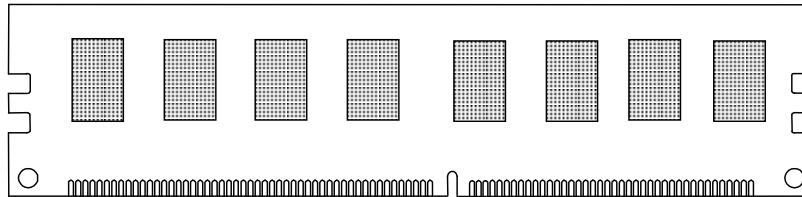
# DTM64379A

4GB - 240-Pin 2Rx8 Unbuffered Non-ECC DDR3 DIMM

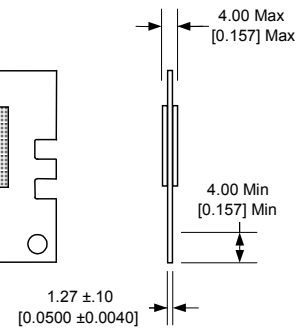
## Front view



## Back view



## Side view



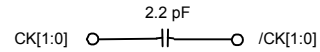
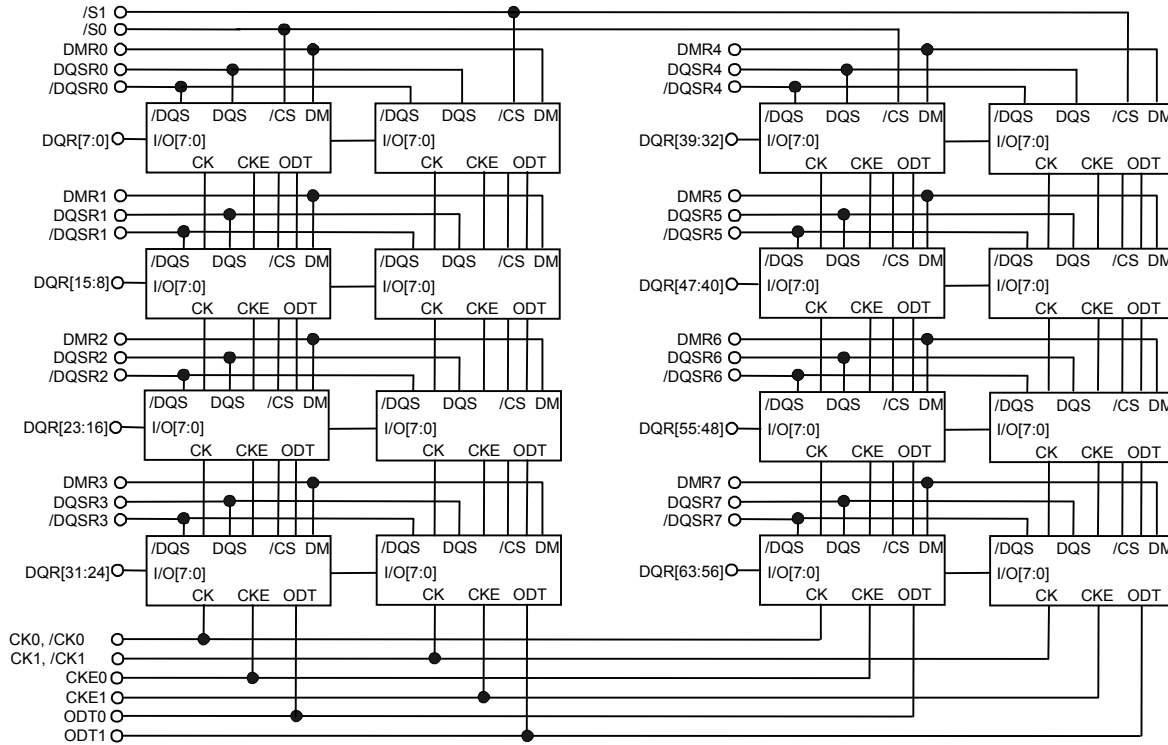
## Notes

Tolerances on all dimensions except where otherwise indicated are  $\pm 0.13$  (.005).

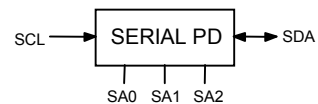
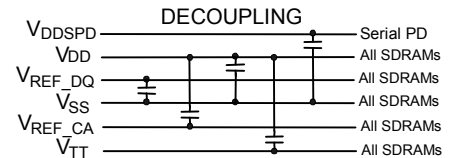
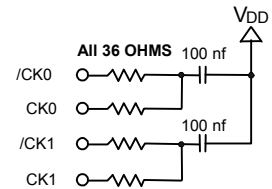
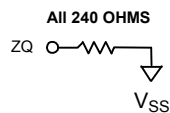
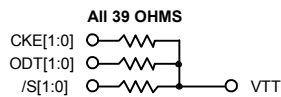
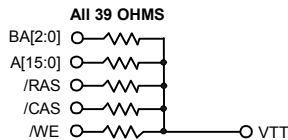
All dimensions are expressed: millimeters [inches]

# DTM64379A

4GB - 240-Pin 2Rx8 Unbuffered Non-ECC DDR3 DIMM



**GLOBAL SDRAM CONNECTS**



### Absolute Maximum Ratings

(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	$T_{STORAGE}$	-55	100	C
Ambient Temperature, Operating	$T_A$	0	70	C
DRAM Case Temperature, Operating	$T_{CASE}$	0	95	C
Voltage on $V_{DD}$ relative to $V_{SS}$	$V_{DD}$	-0.4	1.975	V
Voltage on Any Pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.4	1.975	V

Notes:

DRAM Operating Case Temperature above 85C requires 2X refresh.

### Recommended DC Operating Conditions ( $T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	$V_{DD}$	1.425	1.5	1.575	V	
I/O Reference Voltage	$V_{REFDQ}$	0.49 $V_{DD}$	0.50 $V_{DD}$	0.51 $V_{DD}$	V	1
I/O Reference Voltage	$V_{REFCA}$	0.49 $V_{DD}$	0.50 $V_{DD}$	0.51 $V_{DD}$	V	1

Notes:

1) The value of  $V_{REF}$  is expected to equal one-half  $V_{DD}$  and to track variations in the  $V_{DD}$  DC level. Peak-to-peak noise on  $V_{REF}$  may not exceed  $\pm 1\%$  of its DC value. For Reference  $V_{DD}/2 \pm 15$  mV.

### DC Input Logic Levels, Single-Ended ( $T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(DC)}$	$V_{REF} + 0.1$	$V_{DD}$	V
Logical Low (Logic 0)	$V_{IL(DC)}$	$V_{SS}$	$V_{REF} - 0.1$	V

### AC Input Logic Levels, Single-Ended ( $T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(AC)}$	$V_{REF} + 0.175$	-	V
Logical Low (Logic 0)	$V_{IL(AC)}$	-	$V_{REF} - 0.175$	V

### Differential Input Logic Levels ( $T_A = 0$ to $70$ C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Differential Input Logic High	$V_{IH,DIFF}$	+0.200	DC: $V_{DD}$ AC: $V_{DD}+0.4$	V
Differential Input Logic Low	$V_{IL,DIFF}$	DC: $V_{SS}$ AC: $V_{SS}-0.4$	-0.200	V
Differential Input Cross Point Voltage relative to $V_{DD}/2$	$V_{IX}$	- 0.150	+ 0.150	V

### Capacitance ( $T_A = 25$ C, $f = 100$ MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK0, /CK0, CK1, /CK1	$C_{CK}$	8.6	13.4	pF
Input Capacitance, Address	BA[2:0], A[14:0], /RAS, /CAS, /WE	$C_i$	12	20.8	pF
Input Capacitance Control	/S[1:0], CKE[1:0], ODT[1:0]	$C_i$	6	10.4	
Input/Output Capacitance	DQ[63:0], DQS[7:0], /DQS[7:0], DM[7:0]	$C_{DIO}$	3	5	pF

### DC Characteristics ( $T_A = 0$ to $70$ C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input $0$ V < $V_{IN}$ < $V_{DD}$ )	$I_{IL}$	-16	+32	$\mu$ A	1,2
Output Leakage Current ( $0$ V < $V_{OUT}$ < $V_{DDQ}$ )	$I_{OL}$	-10	+10	$\mu$ A	2,3

Notes:

- 1) All other pins not under test =  $0$  V
- 2) Values are shown per pin
- 3) DQ, DQS, DQS and ODT are disabled

### I<sub>DD</sub> Specifications and Conditions (T<sub>A</sub> = 0 to 70 C, Voltage referenced to V<sub>SS</sub> = 0 V)

PARAMETER	Symbol	Test Condition	Max Value	Unit
Operating One Bank Active-Precharge Current	I <sub>DD0</sub> *	Operating current : One bank ACTIVATE-to-PRECHARGE	522	mA
Operating One Bank Active-Read-Precharge Current	I <sub>DD1</sub> *	Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE	600	mA
Precharge Power-Down Current	I <sub>DD2P</sub> **	Precharge power down current: Fast exit	240	mA
Precharge Quiet Standby Current	I <sub>DD2Q</sub> **	Precharge quiet standby current	320	mA
Precharge Standby Current	I <sub>DD2N</sub> **	Precharge standby current	320	mA
Active Power-Down Current	I <sub>DD3P</sub> **	Active power-down current	320	mA
Active Standby Current	I <sub>DD3N</sub> **	Active standby current	440	mA
Operating Burst Write Current	I <sub>DD4W</sub> *	Burst write operating current	920	mA
Operating Burst Read Current	I <sub>DD4R</sub> *	Burst read operating current	880	mA
Burst Refresh Current	I <sub>DD5</sub> **	Refresh current	1120	mA
Self Refresh Current	I <sub>DD6</sub> **	Self-refresh temperature current: MAX T <sub>c</sub> = 85°C	192	mA
Operating Bank Interleave Read Current	I <sub>DD7</sub> **	All bank interleaved read current	1280	mA

\* One module rank in this operation, the other in IDD2P.

\*\* All module ranks in this operation.

### AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	$t_{AA}$	13.125	20	ns
CAS-to-CAS Command Delay	$t_{CCD}$	4	-	$t_{CK}$
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	$t_{CK}$
Clock Cycle Time	$t_{CK}$	1.25	1.5	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	$t_{CK}$
Data Input Hold Time after DQS Strobe	$t_{DH}$	45	-	ps
DQ Input Pulse Width	$t_{DIPW}$	360	-	ps
DQS Output Access Time from Clock	$t_{DQSCK}$	-225	+225	ps
Write DQS High Level Width	$t_{DQSH}$	0.45	0.55	$t_{CK(avg)}$
Write DQS Low Level Width	$t_{DQSL}$	0.45	0.55	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	$t_{DQSQ}$	-	100	ps
Data Input Setup Time Before DQS Strobe	$t_{DS}$	10	-	ps
DQS Falling Edge from Clock, Hold Time	$t_{DSH}$	0.18	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	$t_{DSS}$	0.18	-	$t_{CK(avg)}$
Clock Half Period	$t_{HP}$	minimum of $t_{CH}$ or $t_{CL}$	-	ns
Address and Command Hold Time after Clock	$t_{IH}$	120	-	ps
Address and Command Setup Time before Clock	$t_{IS}$	45	-	ps
Load Mode Command Cycle Time	$t_{MRD}$	4	-	$t_{CK}$
DQ-to-DQS Hold	$t_{QH}$	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	$t_{RAS}$	35	$9 \cdot t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	$t_{RC}$	48.125	-	ns
RAS-to-CAS Delay	$t_{RCD}$	13.125	-	ns
Average Periodic Refresh Interval $0^{\circ}C \leq T_{CASE} < 85^{\circ}C$	$t_{REFI}$	-	7.8	$\mu s$
Average Periodic Refresh Interval $0^{\circ}C \leq T_{CASE} < 95^{\circ}C$	$t_{REFI}$	-	3.9	$\mu s$
Auto Refresh Row Cycle Time	$t_{RFC}$	160	-	ns
Row Precharge Time	$t_{RP}$	13.125	-	ns
Read DQS Preamble Time	$t_{RPRE}$	0.9	Note-1	$t_{CK(avg)}$
Read DQS Postamble Time	$t_{RPST}$	0.3	Note-2	$t_{CK(avg)}$
Row Active to Row Active Delay	$t_{RRD}$	Max(4nCK, 6ns)	-	ns
Internal Read to Precharge Command Delay	$t_{RTP}$	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	$t_{WPRE}$	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	$t_{WPST}$	0.3	-	$t_{CK(avg)}$
Write Recovery Time	$t_{WR}$	15	-	ns
Internal Write to Read Command Delay	$t_{WTR}$	Max(4nCK, 7.5ns)	-	ns

Notes:

1. The maximum preamble is bound by  $t_{LZDQS}(\min)$ .
2. The maximum postamble is bound by  $t_{HZDQS}(\max)$ .

### SERIAL PRESENCE DETECT MATRIX

Byte#	Function.	Value	Hex
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage.		0x92
	Bit 3 ~ Bit 0. SPD Bytes Used -	176	
	Bit 6 ~ Bit 4. SPD Bytes Total -	256	
	Bit 7. CRC Coverage -	Bytes 0-116	
1	SPD Revision.	Rev. 1.1	0x11
2	Key Byte / DRAM Device Type.	DDR3 SDRAM	0x0B
3	Key Byte / Module Type.		0x02
	Bit 3 ~ Bit 0. Module Type -	UDIMM	
	Bit 7 ~ Bit 4. Reserved -	0	
4	SDRAM Density and Banks.		0x03
	Bit 3 ~ Bit 0. Total SDRAM capacity, in megabits -	2Gb	
	Bit 6 ~ Bit 4. Bank Address Bits -	8 banks	
	Bit 7. Reserved -	0	
5	SDRAM Addressing.		0x19
	Bit 2 ~ Bit 0. Column Address Bits -	10	
	Bit 5 ~ Bit 3. Row Address Bits -	15	
	Bit 7, 6. Reserved	0	
6	Module Nominal Voltage, VDD.		0x00
	Bit 0. NOT 1.5 V operable -		
	Bit 1. 1.35 V operable -		
	Bit 2. 1.2X V operable -		
	Bit 3. Reserved -		
	Bit 4. Reserved -		
	Bit 5. Reserved -		
	Bit 6. Reserved -		
Bit 7. Reserved -			
7	Module Organization.		0x09
	Bit 2 ~ Bit 0. SDRAM Device Width -	8-Bits	
	Bit 5 ~ Bit 3. Number of Ranks -	2-Rank	
	Bit 7, 6. Reserved	0	
8	Module Memory Bus Width.		0x03
	Bit 2 ~ Bit 0. Primary bus width, in bits -	64-Bits	
	Bit 4, Bit 3. Bus width extension, in bits -	0-Bits	
	Bit 7 ~ Bit 5. Reserved -	0	
9	Fine Timebase (FTB) Dividend / Divisor.		0x11
	Bit 3 ~ Bit 0. Fine Timebase (FTB) Divisor	1	
	Bit 7 ~ Bit 4. Fine Timebase (FTB) Dividend	1	
10	Medium Timebase (MTB) Dividend.	1 (MTB = 0.125ns)	0x01

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11	Medium Timebase (MTB) Divisor.	8 (MTB = 0.125ns)	0x08
12	SDRAM Minimum Cycle Time (tCKmin).	1.25ns	0x0A
13	Reserved.	UNUSED	0x00
14	CAS Latencies Supported, Least Significant Byte.		0xFC
		Bit 0. CL = 4 -	
		Bit 1. CL = 5 -	
		Bit 2. CL = 6 - X	
		Bit 3. CL = 7 - X	
		Bit 4. CL = 8 - X	
		Bit 5. CL = 9 - X	
		Bit 6. CL = 10 - X	
	Bit 7. CL = 11 - X		
15	CAS Latencies Supported, Most Significant Byte.		0x00
		Bit 0. CL = 12 -	
		Bit 1. CL = 13 -	
		Bit 2. CL = 14 -	
		Bit 3. CL = 15 -	
		Bit 4. CL = 16 -	
		Bit 5. CL = 17 -	
		Bit 6. CL = 18 -	
	Bit 7. Reserved.		
16	Minimum CAS Latency Time (tAAmin).	13.125ns	0x69
17	Minimum Write Recovery Time (tWRmin).	15.0ns	0x78
18	Minimum RAS# to CAS# Delay Time (tRCDmin).	13.125ns	0x69
19	Minimum Row Active to Row Active Delay Time (tRRDmin).	6.0ns	0x30
20	Minimum Row Precharge Delay Time (tRPmin).	13.125ns	0x69
21	Upper Nibbles for tRAS and tRC.		0x11
		Bit 3 ~ Bit 0. tRAS Most Significant Nibble - 1	
		Bit 7 ~ Bit 4. tRC Most Significant Nibble - 1	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte.	35.0ns	0x18
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte.	48.125ns	0x81
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte.	160.0ns	0x00
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte.	160.0ns	0x05
26	Minimum Internal Write to Read Command Delay Time (tWTRmin).	7.5ns	0x3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin).	7.5ns	0x3C
28	Upper Nibble for tFAW.		0x00
		Bit 3 ~ Bit 0. tFAW Most Significant Nibble - 0	
		Bit 7 ~ Bit 4. Reserved - 0	

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## 4GB - 240-Pin 2Rx8 Unbuffered Non-ECC DDR3 DIMM

29	Minimum Four Activate Window Delay Time (tFAWmin), Least Significant Byte.	30.0ns	0xF0
30	SDRAM Optional Features.		0x83
	Bit 0. RZQ / 6 -	X	
	Bit 1. RZQ / 7 -	X	
	Bit 6 ~ Bit 2. Reserved - Bit 7. DLL-Off Mode Support		
31	SDRAM Drivers Supported.		0x01
	Extended Temperature Range -	X	
	Extended Temperature Refresh Rate -		
	Auto Self Refresh (ASR) -		
	On-die Thermal Sensor (ODTS) Readout -		
	Reserved -		
	Reserved -		
	Reserved -		
32	Module Thermal Sensor.		0x00
	Bit 6 ~ Bit 0. Thermal Sensor Accuracy -	0	
	Bit 7. Thermal Sensor -	No TS	
33	SDRAM Device Type.		0x00
	Bit 6 ~ Bit 0. Non-Standard Device Description -	0	
	Bit 7. SDRAM Device Type -	Std Mono	
34-59	Reserved	UNUSED	0x00
60	Module Nominal Height.		0x0F
	Bit 4 ~ Bit 0. Module Nominal Height max, in mm -	29<h<=30	
	Bit 7 ~ Bit5. Reserved -	0	
61	Module Maximum Thickness.		0x11
	Bit 3 ~ Bit 0. Front, in mm (baseline thickness = 1 mm) -	1<th<=2	
	Bit 7 ~ Bit 4. Back, in mm (baseline thickness = 1 mm) -	1<th<=2	
62	Reference Raw Card Used.		0x21
	Bit 4 ~ Bit 0. Reference Raw Card -	R/C B	
	Bit 6, Bit 5. Reference Raw Card Revision -	Rev.1	
	Bit 7. Reserved -	0	
63	Address Mapping from Edge Connector to DRAM.		0x01
	Bit 0. Rank 1 Mapping (Registered DIMM - Reserved) -	Mirrored	
	Bit 7 ~ Bit 1. Reserved -	0	
64 - 116	Module-Specific Section	UNUSED	0x00
117	Module Manufacturer ID Code, Least Significant Byte		0x80
118	Module Manufacturer ID Code, Most Significant Byte		0xCE
119	Module Manufacturing Location		0x01
120	Module Manufacturing Date		0x11
121	Module Manufacturing Date		0x15



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## 4GB - 240-Pin 2Rx8 Unbuffered Non-ECC DDR3 DIMM

122	Module Serial Number		0x47
123	Module Serial Number		0x19
124	Module Serial Number		0xEE
125	Module Serial Number		0xE8
126	Cyclical Redundancy Code (CRC).	CRC	0xBC
127	Cyclical Redundancy Code (CRC).	CRC	0xC0
128	Module Part Number	M	0x4D
129	Module Part Number	3	0x33
130	Module Part Number	7	0x37
131	Module Part Number	8	0x38
132	Module Part Number	B	0x42
133	Module Part Number	5	0x35
134	Module Part Number	2	0x32
135	Module Part Number	7	0x37
136	Module Part Number	3	0x33
137	Module Part Number	D	0x44
138	Module Part Number	H	0x48
139	Module Part Number	0	0x30
140	Module Part Number	-	0x2D
141	Module Part Number	C	0x43
142	Module Part Number	K	0x4B
143	Module Part Number	0	0x30
144, 145	Module Part Number		0x20
146, 147	Module Revision Code	UNUSED	0x00
148	DRAM Manufacturer ID Code, Least Significant Byte		0x80
149	DRAM Manufacturer ID Code, Most Significant Byte		0xCE
150- 175	Manufacturer's Specific Data		0x00
176- 255	Open for customer use	UNUSED	0x00

Note: Bytes 119 – 125 and 150 - 255 may be different then shown.



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4GB - 240-Pin 2Rx8 Unbuffered Non-ECC DDR3 DIMM

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