DTM64361B

2 GB - 240-Pin 1Rx8 Unbuffered ECC DDR3 DIMM

Identification

DTM64361B 256Mx72
2GB 1Rx8 PC3-10600E-9-11-D0

Performance range

Clock / Module Speed / CL-t_{RCD} -t_{RP}

667 MHz / PC3-10600 / 9-9-9
533 MHz / PC3-8500 / 8-8-8
533 MHz / PC3-8500 / 7-7-7
400 MHz / PC3-6400 / 6-6-6

Features

- 240-pin JEDEC-compliant DIMM, 133.35 mm wide by 30 mm high
- Operating Voltage: 1.5 V ±0.075, I/O Type: SSTL_15
- On-board I^2C temperature sensor with integrated Serial Presence-Detect (SPD) EEPROM
- Data Transfer Rate: 10.6 Gigabytes/sec
- Data Bursts: 8 and burst chop 4 mode
- ZQ Calibration for Output Driver and On-Die Termination (ODT)
- Programmable ODT / Dynamic ODT during Writes
- Programmable CAS Latency: 6, 7, 8, and 9
- Differential Data Strobe signals
- SDRAM Addressing (Row/Col/Bank): 15/10/3
- Fully RoHS Compliant

Description

DTM64361B is an Unbuffered 256Mx72 memory module, which conforms to JEDEC's DDR3, PC3-10600 standard.

The assembly is one Rank. The Rank is comprised of nine 256Mx8 DDR3-1333 Hynix SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect.

A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.

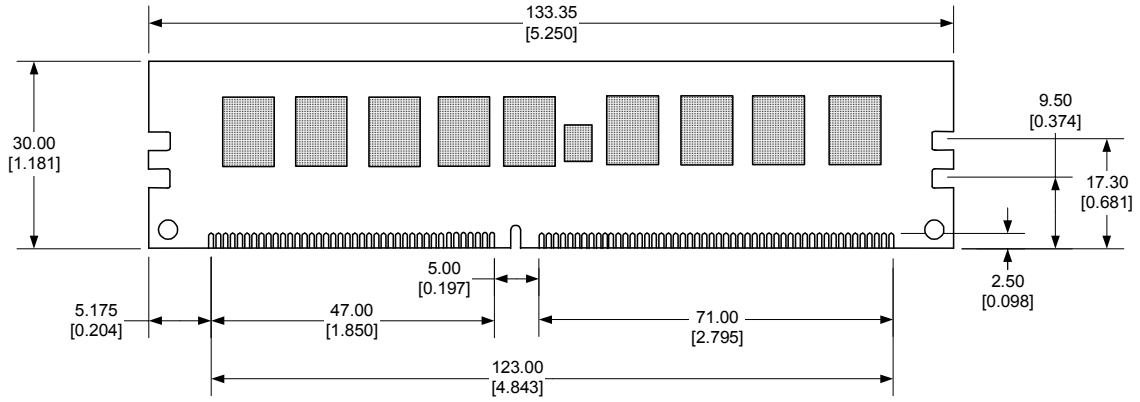
Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals.

Pin Configuration

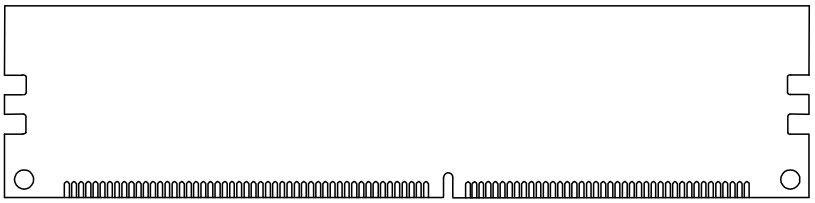
Front Side				Back Side				Pin Description	
								Name	**Function**
1 VREFDQ	31 DQ25	61 A2	91 DQ41	121 VSS	151 VSS	181 A1	211 VSS	CB[7:0]	Data Check Bits
2 VSS	32 VSS	62 VDD	92 VSS	122 DQ4	152 DM3	182 VDD	212 DM5	DQ[63:0]	Data Bits
3 DQ0	33 /DQS3	63 CK1*	93 /DQS5	123 DQ5	153 NC	183 VDD	213 NC	DQS[8:0], /DQS[8:0]	Differential Data Strobes
4 DQ1	34 DQS3	64 /CK1*	94 DQS5	124 VSS	154 VSS	184 CK0	214 VSS	DM[8:0]	Data Mask
5 VSS	35 VSS	65 VDD	95 VSS	125 DM0	155 DQ30	185 /CK0	215 DQ46	CK[1:0], /CK[1:0]	Differential Clock Inputs
6 /DQS0	36 DQ26	66 VDD	96 DQ42	126 NC	156 DQ31	186 VDD	216 DQ47	CKE[1:0]	Clock Enables
7 DQS0	37 DQ27	67 VREFCA	97 DQ43	127 VSS	157 VSS	187 /EVENT	217 VSS	/CAS	Column Address Strobe
8 VSS	38 VSS	68 PAR_IN, NC*	98 VSS	128 DQ6	158 CB4	188 A0	218 DQ52	/RAS	Row Address Strobe
9 DQ2	39 CB0	69 VDD	99 DQ48	129 DQ7	159 CB5	189 VDD	219 DQ53	/S[3:0]	Chip Selects
10 DQ3	40 CB1	70 A10/AP	100 DQ49	130 VSS	160 VSS	190 BA1	220 VSS	/WE	Write Enable
11 VSS	41 VSS	71 BA0	101 VSS	131 DQ12	161 DM8	191 VDD	221 DM6	A[15:0]	Address Inputs
12 DQ8	42 /DQS8	72 VDD	102 /DQS6	132 DQ13	162 NC	192 /RAS	222 NC	BA[2:0]	Bank Addresses
13 DQ9	43 DQS8	73 /WE	103 DQS6	133 VSS	163 VSS	193 /S0	223 VSS	ODT[1:0]	On Die Termination Inputs
14 VSS	44 VSS	74 /CAS	104 VSS	134 DM1	164 CB6	194 VDD	224 DQ54	SA[2:0]	SPD Address
15 /DQS1	45 CB2	75 VDD	105 DQ50	135 NC	165 CB7	195 ODT0	225 DQ55	SCL	SPD Clock Input
16 DQS1	46 CB3	76 /S1, NC*	106 DQ51	136 VSS	166 VSS	196 A13	226 VSS	SDA	SPD Data Input/Output
17 VSS	47 VSS	77 ODT1, NC*	107 VSS	137 DQ14	167 TEST, NC*	197 VDD	227 DQ60	/EVENT	Temperature Sensing
18 DQ10	48 VTT, NC	78 VDD	108 DQ56	138 DQ15	168 /RESET	198 /S3, NC*	228 DQ61	/RESET	Reset for register and DRAMs
19 DQ11	49 VTT, NC	79 /S2, NC*	109 DQ57	139 VSS	169 CKE1, NC*	199 VSS	229 VSS	PAR_IN	Parity bit for Addr/Ctrl
20 VSS	50 CKE0	80 VSS	110 VSS	140 DQ20	170 VDD	200 DQ36	230 DM7	/ERR_OUT	Error bit for Parity Error
21 DQ16	51 VDD	81 DQ32	111 /DQS7	141 DQ21	171 A15*	201 DQ37	231 NC	A12/BC	Combination input: Addr12/Burst Chop
22 DQ17	52 BA2	82 DQ33	112 DQS7	142 VSS	172 A14*	202 VSS	232 VSS	A10/AP	Combination input: Addr10/Auto-precharge
23 VSS	53 /ERR_OUT, NC*	83 VSS	113 VSS	143 DM2	173 VDD	203 DM4	233 DQ62	V_{SS}	Ground
24 /DQS2	54 VDD	84 /DQS4	114 DQ58	144 NC	174 A12/BC	204 NC	234 DQ63	V_{DD}	Power
25 DQS2	55 A11	85 DQS4	115 DQ59	145 VSS	175 A9	205 VSS	235 VSS	V_{DDSPD}	SPD EEPROM Power
26 VSS	56 A7	86 VSS	116 VSS	146 DQ22	176 VDD	206 DQ38	236 VDDSPD	V_{REFDQ}	Reference Voltage for DQ's
27 DQ18	57 VDD	87 DQ34	117 SA0	147 DQ23	177 A8	207 DQ39	237 SA1	V_{REFCA}	Reference Voltage for CA
28 DQ19	58 A5	88 DQ35	118 SCL	148 VSS	178 A6	208 VSS	238 SDA	V_{TT}	Termination Voltage
29 VSS	59 A4	89 VSS	119 SA2	149 DQ28	179 VDD	209 DQ44	239 VSS	NC	No Connection
30 DQ24	60 VDD	90 DQ40	120 VTT	150 DQ29	180 A3	210 DQ45	240 VTT		

* Not used

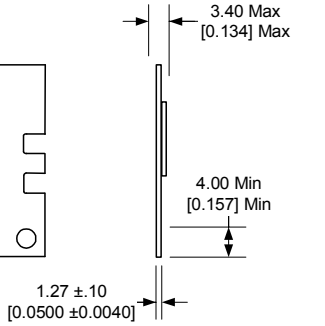
Front view



Back view



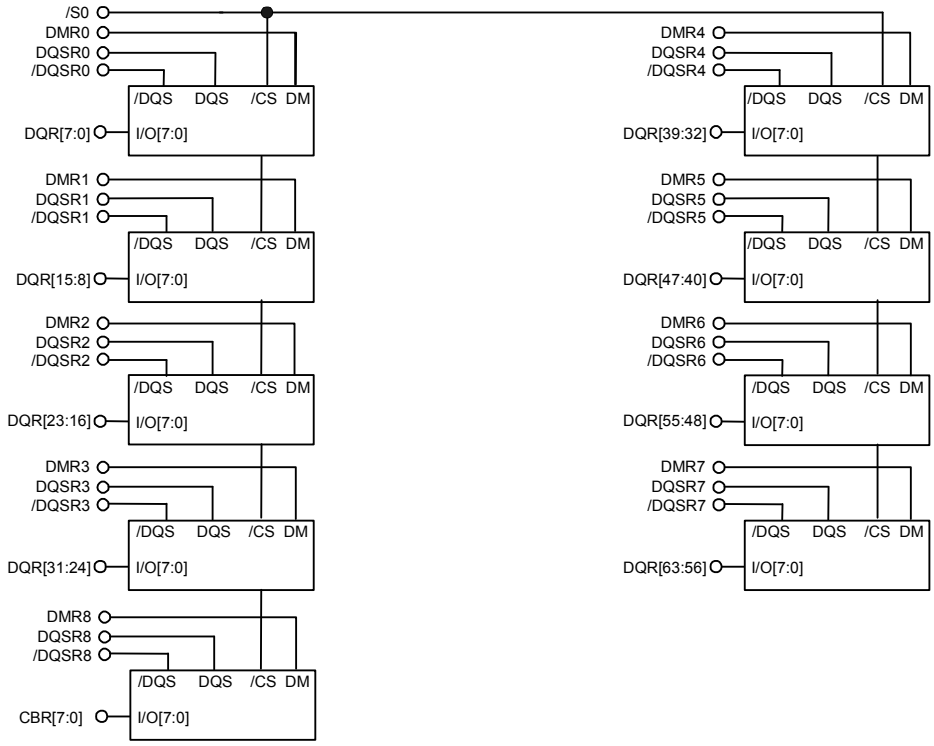
Side view

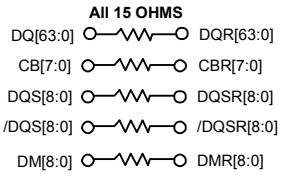


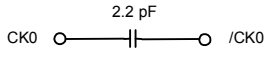
Notes

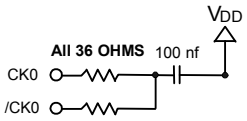
Tolerances on all dimensions except where otherwise indicated are ±.13 (.005).

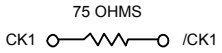
All dimensions are expressed: millimeters [inches]



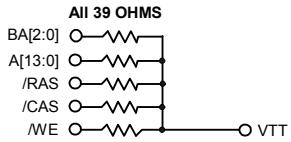


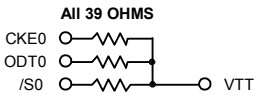


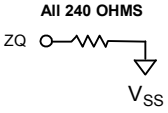


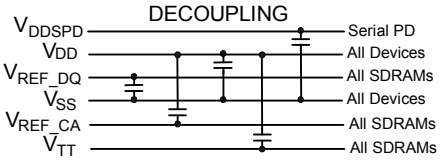


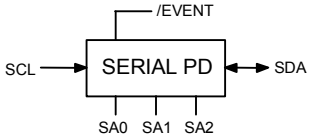
GLOBAL SDRAM CONNECTS











Absolute Maximum Ratings

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	$T_{STORAGE}$	-55	100	C
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.4	1.975	V
Voltage on Any Pin relative to V_{SS}	V_{IN},V_{OUT}	-0.4	1.975	V

Notes:

1. Operation at or above Absolute Maximum Ratings can adversely affect module reliability.

SDRAM Component Operating Temperature Range

PARAMETER	Symbol	Minimum	Maximum	Unit	Notes
Normal Operating Temperature Range	T_{OPER}	0	85	C	1, 2, 3
Extended Temperature Range		85	95	C	1, 3, 4

Notes:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the SDRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all SDRAM specification will be supported.
3. During operation, the SDRAM operating temperature must be maintained above 0 C under all operating conditions. Either the device operating temperature rating may be used to set an appropriate refresh rate and/or to monitor the maximum operating temperature.
4. Some applications require operation of the DRAM in the Extended Temperature Range between 85 C and 95 C operating temperature.
5. Full specifications are provided in this range, but the following additional conditions apply:

   a) Refresh commands have to be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs.

   b) If Self-Refresh operation is required in the Extended Temperature Range, than it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0B and MR2 A7 = 1B) or enable the Auto Self-Refresh mode (ASR) (MR2 A6 = 1B and MR2 A7= 0B). For SDRAM operations on DIMM module refer to DIMM module data sheets and SPD bytes for Extended Temperature and Auto Self-Refresh option availability.

Recommended DC Operating Conditions (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V_{DD}	1.425	1.5	1.575	V	
I/O Reference Voltage	V_{REFDQ}	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1
I/O Reference Voltage	V_{REFCA}	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1

Notes:

1. The value of V_{REF} is expected to equal one-half V_{DD} and to track variations in the V_{DD} DC level. Peak-to-peak noise on V_{REF} may not exceed ±1% V_{DD} (approx ±15 mV).

DC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(DC)}$	V_{REF} + 0.1	V_{DD}	V
Logical Low (Logic 0)	$V_{IL(DC)}$	V_{SS}	V_{REF} - 0.1	V

AC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(AC)}$	V_{REF} + 0.175	-	V
Logical Low (Logic 0)	$V_{IL(AC)}$	-	V_{REF} - 0.175	V

Differential Input Logic Levels (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Differential Input Logic High	$V_{IH.DIFF}$	+0.200		V	
Differential Input Logic Low	$V_{IL.DIFF}$		-0.200	V	
Differential Input Cross Point Voltage relative to VDD/2 for CK - /CK	V_{IX}	- 0.150	+ 0.150	V	1
		- 0.175	+ 0.175		
Differential Input Cross Point Voltage relative to VDD/2 for DQS - /DQS	V_{IX}	- 0.150	+ 0.150	V	

Notes:

1. Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and /CK are monotonic, have a single-ended swing of at least VDD/2 ±250 mV and if the differential slew rate of CK - CK is larger than 3 V/ns.

Capacitance (T_A = 25 C, f = 100 MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK0, /CK0	C_{CK}	7.2	12.6	pF
Input Capacitance, Address	BA[2:0], A[14:0], /RAS, /CAS, /WE	C_I	6.75	11.7	pF
Input Capacitance, Control	/S0, CKE0, ODT0	C_I	6.75	11.7	pF
Input/Output Capacitance	DQ[63:0], CB[7:0] DQS[8:0], /DQS[8:0], DM[8:0]	C_{IO}	1.5	2.5	pF

DC Characteristics (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input 0 V < V_{IN} < VDD)	I_{IL}	-18	+18	µA	1,2
Output Leakage Current (0V < V_{OUT} < VDDQ)	I_{OL}	-5	+5	µA	2,3

Notes:
1) All other pins not under test = 0 V
2) Values are shown per pin
3) DQ, DQS, /DQS and ODT are disabled

I_{DD} Specifications and Conditions (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Test Condition	Max Value	Unit
Operating One Bank Active-Precharge Current	$I_{DD}0$	Operating current : One bank ACTIVATE-to-PRECHARGE	360	mA
Operating One Bank Active-Read-Precharge Current	$I_{DD}1$	Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE	450	mA
Precharge Power-Down Current	$I_{DD}2P$	Precharge power down current: (Slow exit)	108	mA
Precharge Power-Down Current	$I_{DD}2P$	Precharge power down current: (Fast exit)	135	mA
Precharge Quiet Standby Current	$I_{DD}2Q$	Precharge quiet standby current	207	mA
Precharge Standby Current	$I_{DD}2N$	Precharge standby current	225	mA
Active Power-Down Current	$I_{DD}3P$	Active power-down current	135	mA
Active Standby Current	$I_{DD}3N$	Active standby current	243	mA
Operating Burst Write Current	$I_{DD}4W$	Burst write operating current	765	mA
Operating Burst Read Current	$I_{DD}4R$	Burst read operating current	810	mA
Burst Refresh Current	$I_{DD}5B$	Refresh current	1035	mA
Self Refresh Current	$I_{DD}6ET$	Self-refresh current, Extended Temperature (0 to 95 C)	108	mA
Operating Bank Interleave Read Current	$I_{DD}7$	All bank interleaved read current	1620	mA

AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	t_{AA}	13.125	20	ns
CAS-to-CAS Command Delay	t_{CCD}	4	-	t_{CK}
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	t_{CK}
Clock Cycle Time	t_{CK}	1.5	3.3	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	t_{CK}
Data Input Hold Time after DQS Strobe	t_{DH}	65	-	ps
DQ Input Pulse Width	t_{DIPW}	400	-	ps
DQS Output Access Time from Clock	t_{DQSCK}	-255	+255	ps
Write DQS High Level Width	t_{DQSH}	0.45	0.55	$t_{CK(avg)}$
Write DQS Low Level Width	t_{DQSL}	0.45	0.55	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	t_{DQSQ}	-	125	ps
Data Input Setup Time Before DQS Strobe	t_{DS}	30	-	ps
DQS Falling Edge from Clock, Hold Time	t_{DSH}	0.2	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	t_{DSS}	0.2	-	$t_{CK(avg)}$
Address and Command Hold Time after Clock	t_{IH}	140	-	ps
Address and Command Setup Time before Clock	t_{IS}	65	-	ps
Load Mode Command Cycle Time	t_{MRD}	4	-	t_{CK}
DQ-to-DQS Hold	t_{QH}	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	t_{RAS}	36	$9*t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	t_{RC}	49.125	-	ns
RAS-to-CAS Delay	t_{RCD}	13.125	-	ns
Average Periodic Refresh Interval (0 C ≤ T_{CASE} ≤ 85 C)	t_{REFI}	-	7.8	µs
Average Periodic Refresh Interval (85 C < T_{CASE} ≤ 95 C)			3.9	
Auto Refresh Row Cycle Time	t_{RFC}	160	-	ns
Row Precharge Time	t_{RP}	13.125	-	ns
Read DQS Preamble Time	t_{RPRE}	0.9	Note-1	$t_{CK(avg)}$
Read DQS Postamble Time	t_{RPST}	0.3	Note-2	$t_{CK(avg)}$
Row Active to Row Active Delay	t_{RRD}	Max(4nCK, 7.5ns)	-	ns
Internal Read to Precharge Command Delay	t_{RTP}	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	t_{WPRE}	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	t_{WPST}	0.3	-	$t_{CK(avg)}$
Write Recovery Time	t_{WR}	15	-	ns
Internal Write to Read Command Delay	t_{WTR}	Max(4nCK, 7.5ns)	-	ns

Notes:
1. The maximum read preamble is bound by $t_{LZ(DQS)}$(min) on the left side and t_{DQSCK}(max) on the right side.
2. The maximum read postamble is bound by t_{DQSCK}(min) plus t_{QSH}(min) on the left side and $t_{HZ(DQS)}$(max) on the right side.

SERIAL PRESENCE DETECT MATRIX

Byte#	Function.	Value	Hex
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage.		0x92
	Bit 3 ~ Bit 0. SPD Bytes Used -	176	
	Bit 6 ~ Bit 4. SPD Bytes Total -	256	
	Bit 7. CRC Coverage -	Bytes 0-116	
1	SPD Revision.	Rev. 1.1	0x11
2	Key Byte / DRAM Device Type.	DDR3 SDRAM	0x0B
3	Key Byte / Module Type.		0x02
	Bit 3 ~ Bit 0. Module Type -	UDIMM	
	Bit 7 ~ Bit 4. Reserved -	0	
4	SDRAM Density and Banks.		0x03
	Bit 3 ~ Bit 0. Total SDRAM capacity, in megabits -	2Gb	
	Bit 6 ~ Bit 4. Bank Address Bits -	8 banks	
	Bit 7. Reserved -	0	
5	SDRAM Addressing.		0x19
	Bit 2 ~ Bit 0. Column Address Bits -	10	
	Bit 5 ~ Bit 3. Row Address Bits -	15	
	Bit 7, 6. Reserved	0	
6	Reserved.		0x00
7	Module Organization.		0x01
	Bit 2 ~ Bit 0. SDRAM Device Width -	8-Bits	
	Bit 5 ~ Bit 3. Number of Ranks -	1-Rank	
	Bit 7, 6. Reserved	0	
8	Module Memory Bus Width.		0x0B
	Bit 2 ~ Bit 0. Primary bus width, in bits -	64-Bits	
	Bit 4, Bit 3. Bus width extension, in bits -	8-Bits	
	Bit 7 ~ Bit 5. Reserved -	0	
9	Fine Timebase (FTB) Dividend / Divisor.		0x52
	Bit 3 ~ Bit 0. Fine Timebase (FTB) Divisor	2	
	Bit 7 ~ Bit 4. Fine Timebase (FTB) Dividend	5	
10	Medium Timebase (MTB) Dividend.	1 (MTB = 0.125ns)	0x01
11	Medium Timebase (MTB) Divisor.	8 (MTB = 0.125ns)	0x08
12	SDRAM Minimum Cycle Time (tCKmin).	1.5ns	0x0C
13	Reserved.	UNUSED	0x00
14	CAS Latencies Supported, Least Significant Byte.		0x3C
	Bit 0. CL = 4 -		
	Bit 1. CL = 5 -		

	Bit 2. CL = 6 -	X	
	Bit 3. CL = 7 -	X	
	Bit 4. CL = 8 -	X	
	Bit 5. CL = 9 -	X	
	Bit 6. CL = 10 -		
	Bit 7. CL = 11 -		
15	CAS Latencies Supported, Most Significant Byte.		0x00
	Bit 0. CL = 12 -		
	Bit 1. CL = 13 -		
	Bit 2. CL =14 -		
	Bit 3. CL = 15 -		
	Bit 4. CL = 16 -		
	Bit 5. CL = 17 -		
	Bit 6. CL = 18 -		
	Bit 7. Reserved.		
16	Minimum CAS Latency Time (tAAmin).	13.125ns	0x69
17	Minimum Write Recovery Time (tWRmin).	15.0ns	0x78
18	Minimum RAS# to CAS# Delay Time (tRCDmin).	13.125ns	0x69
19	Minimum Row Active to Row Active Delay Time (tRRDmin).	6.0ns	0x30
20	Minimum Row Precharge Delay Time (tRPmin).	13.125ns	0x69
21	Upper Nibbles for tRAS and tRC.		0x11
	Bit 3 ~ Bit 0. tRAS Most Significant Nibble -	1	
	Bit 7 ~ Bit 4. tRC Most Significant Nibble -	1	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte.	36.0ns	0x20
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte.	49.125ns	0x89
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte.	160.0ns	0x00
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte.	160.0ns	0x05
26	Minimum Internal Write to Read Command Delay Time (tWTRmin).	7.5ns	0x3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin).	7.5ns	0x3C
28	Upper Nibble for tFAW.		0x00
	Bit 3 ~ Bit 0. tFAW Most Significant Nibble -	0	
	Bit 7 ~ Bit 4. Reserved -	0	
29	Minimum Four Activate Window Delay Time (tFAWmin), Least Significant Byte.	30.0ns	0xF0
30	SDRAM Optional Features.		0x83
	Bit 0. RZQ / 6 -	X	
	Bit 1. RZQ / 7 -	X	
	Bit 6 ~ Bit 2. Reserved -		

31	Bit 7. DLL-Off Mode Support		0x05
	SDRAM Drivers Supported.		
	Extended Temperature Range -	X	
	Extended Temperature Refresh Rate -		
	Auto Self Refresh (ASR) -	X	
	On-die Thermal Sensor (ODTS) Readout -		
	Reserved -		
	Reserved -		
	Reserved -		
	Partial Array Self Refresh (PASR) -		
32	Module Thermal Sensor.		0x80
	Bit 6 ~ Bit 0. Thermal Sensor Accuracy -	0	
	Bit 7. Thermal Sensor -	With TS	
33	SDRAM Device Type.		0x00
	Bit 6 ~ Bit 0. Non-Standard Device Description -	0	
	Bit 7. SDRAM Device Type -	Std Mono	
34-59	Reserved	UNUSED	0x00
60	Module Nominal Height.		0x0F
	Bit 4 ~ Bit 0. Module Nominal Height max, in mm -	29<h<=30	
	Bit 7 ~ Bit5. Reserved -	0	
61	Module Maximum Thickness.		0x01
	Bit 3 ~ Bit 0. Front, in mm (baseline thickness = 1 mm) -	1<th<=2	
	Bit 7 ~ Bit 4. Back, in mm (baseline thickness = 1 mm) -	th<=1	
62	Reference Raw Card Used.		0x03
	Bit 4 ~ Bit 0. Reference Raw Card -	R/C D	
	Bit 6, Bit 5. Reference Raw Card Revision -	Rev.0	
	Bit 7. Reserved -	0	
63	Address Mapping from Edge Connector to DRAM.		0x00
	Bit 0. Rank 1 Mapping (Registered DIMM - Reserved) -	Standard	
	Bit 7 ~ Bit 1. Reserved -	0	
64-112	Module-Specific Section	UNUSED	0x00
113	Module-Specific Section.	UNUSED	0x00
114-116	Module-Specific Section	UNUSED	0x00
117	Module Manufacturer ID Code, Least Significant Byte		0x01
118	Module Manufacturer ID Code, Most Significant Byte		0x91
119	Module Manufacturing Location	UNUSED	0x00
120,121	Module Manufacturing Date	UNUSED	0x00
122-125	Module Serial Number	#	0x23
126	Cyclical Redundancy Code (CRC).	CRC	0x63
127	Cyclical Redundancy Code (CRC).	CRC	0xD1
128-131	Module Part Number		0x20

132	Module Part Number	D	0x44
133	Module Part Number	A	0x41
134	Module Part Number	T	0x54
135	Module Part Number	A	0x41
136	Module Part Number	R	0x52
137	Module Part Number	A	0x41
138	Module Part Number	M	0x4D
139	Module Part Number		0x20
140	Module Part Number	6	0x36
141	Module Part Number	4	0x34
142	Module Part Number	3	0x33
143	Module Part Number	6	0x36
144	Module Part Number	1	0x31
145	Module Part Number		0x20
146,147	Module Revision Code		0x20
148	DRAM Manufacturer ID Code, Least Significant Byte	UNUSED	0x00
149	DRAM Manufacturer ID Code, Most Significant Byte	UNUSED	0x00
150-175	Manufacturer's Specific Data	UNUSED	0x00
176-255	Open for customer use	UNUSED	0x00

Bytes: 122-125 change per DIMM.

DATARAM CORPORATION, USA Corporate Headquarters, P.O. Box 7528, Princeton, NJ 08543-7528;
Voice: 609-799-0071, Fax: 609-799-6734; www.dataram.com