

# DTM64400B

## 8GB - 240-Pin 2Rx4 Registered ECC LV DDR3 DIMM



### Identification

DTM64400B 1Gx72  
 8GB 2Rx4 PC3L-12800R-11-11-E2

### Performance range

Clock / Module Speed / CL-t<sub>RCD</sub> -t<sub>RP</sub>

800 MHz / PC3L-12800 / 11-11-11  
 667 MHz / PC3L-10600 / 10-10-10  
 667 MHz / PC3L-10600 / 9-9-9  
 533 MHz / PC3L-8500 / 8-8-8  
 533 MHz / PC3L-8500 / 7-7-7  
 400 MHz / PC3L-6400 / 6-6-6

### Features

240-pin JEDEC-compliant DIMM, 133.35 mm wide by 30 mm high

Operating Voltage: VDD = VDDQ = +1.35V (1.283V to 1.45V)

Backward-compatible to VDD = VDDQ = +1.5V ±0.075V

On-board I<sup>2</sup>C temperature sensor with integrated Serial Presence-Detect (SPD) EEPROM

Data Transfer Rate: 12.8 Gigabytes/sec

Data Bursts: 8 and burst chop 4 mode

ZQ Calibration for Output Driver and On-Die Termination (ODT)

Programmable ODT / Dynamic ODT during Writes

Programmable CAS Latency: 6, 7, 8, 9, 10 and 11

Bi-directional Differential Data Strobe signals

SDRAM Addressing (Row/Col/Bank): 15/11/3

Fully RoHS Compliant

### Description

DTM64400B is a registered 1Gx72 memory module, which conforms to JEDEC's DDR3, PC3L-12800 standard. The assembly is Dual-Rank. Each Rank is comprised of eighteen 512Mx4 DDR3-1600 Hynix SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect and a combination register/PLL, with Address and Command Parity, is also used.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals in a Fly-by topology. A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.

### Pin Configuration

### Pin Description

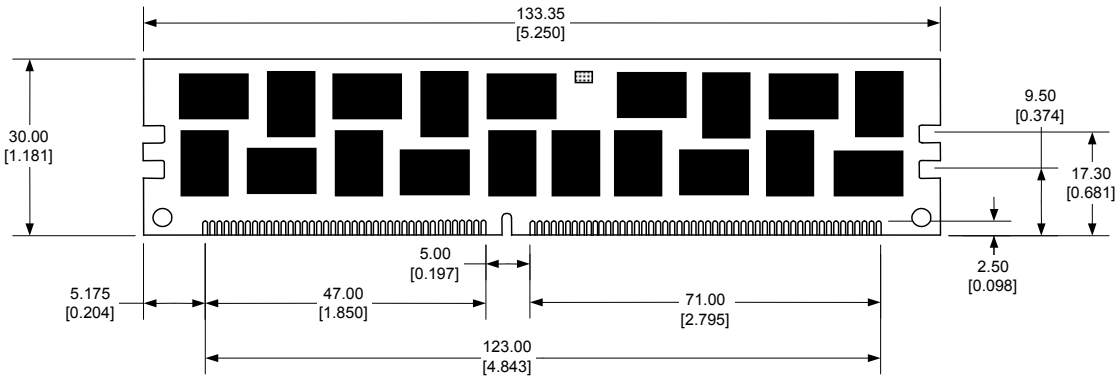
Front Side				Back Side				Name	Function
1 V <sub>REFDQ</sub>	31 DQ25	61 A2	91 DQ41	121 V <sub>SS</sub>	151 V <sub>SS</sub>	181 A1	211 V <sub>SS</sub>	CB[7:0]	Data Check Bits
2 V <sub>SS</sub>	32 V <sub>SS</sub>	62 V <sub>DD</sub>	92 V <sub>SS</sub>	122 DQ4	152 DQS12	182 V <sub>DD</sub>	212 DQS14	DQ[63:0]	Data Bits
3 DQ0	33 /DQS3	63 CK1*	93 /DQS5	123 DQ5	153 /DQS12	183 V <sub>DD</sub>	213 /DQS14	DQS[17:0], /DQS[17:0]	Differential Data Strobes
4 DQ1	34 DQS3	64 /CK1*	94 DQS5	124 V <sub>SS</sub>	154 V <sub>SS</sub>	184 CK0	214 V <sub>SS</sub>	CK[1:0], /CK[1:0]	Differential Clock Inputs
5 V <sub>SS</sub>	35 V <sub>SS</sub>	65 V <sub>DD</sub>	95 V <sub>SS</sub>	125 DQS9	155 DQ30	185 /CK0	215 DQ46	CKE[1:0]	Clock Enables
6 /DQS0	36 DQ26	66 V <sub>DD</sub>	96 DQ42	126 /DQS9	156 DQ31	186 V <sub>DD</sub>	216 DQ47	/CAS	Column Address Strobe
7 DQS0	37 DQ27	67 V <sub>REFCA</sub>	97 DQ43	127 V <sub>SS</sub>	157 V <sub>SS</sub>	187 /EVENT	217 V <sub>SS</sub>	/RAS	Row Address Strobe
8 V <sub>SS</sub>	38 V <sub>SS</sub>	68 PAR <sub>IN</sub>	98 V <sub>SS</sub>	128 DQ6	158 CB4	188 A0	218 DQ52	/S[3:0]	Chip Selects
9 DQ2	39 CB0	69 VDD	99 DQ48	129 DQ7	159 CB5	189 V <sub>DD</sub>	219 DQ53	/WE	Write Enable
10 DQ3	40 CB1	70 A10/AP	100 DQ49	130 V <sub>SS</sub>	160 V <sub>SS</sub>	190 BA1	220 V <sub>SS</sub>	A[15:0]	Address Inputs
11 V <sub>SS</sub>	41 V <sub>SS</sub>	71 BA0	101 V <sub>SS</sub>	131 DQ12	161 DQS17	191 V <sub>DD</sub>	221 DQS15	BA[2:0]	Bank Addresses
12 DQ8	42 /DQS8	72 V <sub>DD</sub>	102 /DQS6	132 DQ13	162 /DQS17	192 /RAS	222 /DQS15	ODT[1:0]	On Die Termination Inputs
13 DQ9	43 DQS8	73 /WE	103 DQS6	133 V <sub>SS</sub>	163 V <sub>SS</sub>	193 /S0	223 V <sub>SS</sub>	SA[2:0]	SPD Address
14 V <sub>SS</sub>	44 V <sub>SS</sub>	74 /CAS	104 V <sub>SS</sub>	134 DQS10	164 CB6	194 V <sub>DD</sub>	224 DQ54	SCL	SPD Clock Input
15 /DQS1	45 CB2	75 V <sub>DD</sub>	105 DQ50	135 /DQS10	165 CB7	195 ODT0	225 DQ55	SDA	SPD Data Input/Output
16 DQS1	46 CB3	76 /S1	106 DQ51	136 V <sub>SS</sub>	166 V <sub>SS</sub>	196 A13	226 V <sub>SS</sub>	/EVENT	Temperature Sensing
17 V <sub>SS</sub>	47 V <sub>SS</sub>	77 ODT1	107 V <sub>SS</sub>	137 DQ14	167 NC (TEST)	197 V <sub>DD</sub>	227 DQ60	/RESET	Reset for register and DRAMs
18 DQ10	48 V <sub>TT</sub>	78 V <sub>DD</sub>	108 DQ56	138 DQ15	168 /RESET	198 /S3, NC	228 DQ61	PAR <sub>IN</sub>	Parity bit for Addr/Ctrl
19 DQ11	49 V <sub>TT</sub>	79 /S2, NC	109 DQ57	139 V <sub>SS</sub>	169 CKE1	199 V <sub>SS</sub>	229 V <sub>SS</sub>	/ERR <sub>OUT</sub>	Error bit for Parity Error
20 V <sub>SS</sub>	50 CKE0	80 V <sub>SS</sub>	110 V <sub>SS</sub>	140 DQ20	170 V <sub>DD</sub>	200 DQ36	230 DQS16	A12/BC	Combination input: Addr12/Burst Chop
21 DQ16	51 V <sub>DD</sub>	81 DQ32	111 /DQS7	141 DQ21	171 A15	201 DQ37	231 /DQS16	A10/AP	Combination input: Addr10/Auto-precharge
22 DQ17	52 BA2	82 DQ33	112 DQS7	142 V <sub>SS</sub>	172 A14	202 V <sub>SS</sub>	232 V <sub>SS</sub>	V <sub>SS</sub>	Ground
23 V <sub>SS</sub>	53 /ERR <sub>OUT</sub>	83 V <sub>SS</sub>	113 V <sub>SS</sub>	143 DQS11	173 V <sub>DD</sub>	203 DQS13	233 DQ62	V <sub>DD</sub>	Power
24 /DQS2	54 V <sub>DD</sub>	84 /DQS4	114 DQ58	144 /DQS11	174 A12/BC	204 /DQS13	234 DQ63	V <sub>DDSPD</sub>	SPD EEPROM Power
25 DQS2	55 A11	85 DQS4	115 DQ59	145 V <sub>SS</sub>	175 A9	205 V <sub>SS</sub>	235 V <sub>SS</sub>	V <sub>REFDQ</sub>	Reference Voltage for DQ's
26 V <sub>SS</sub>	56 A7	86 V <sub>SS</sub>	116 V <sub>SS</sub>	146 DQ22	176 V <sub>DD</sub>	206 DQ38	236 V <sub>DDSPD</sub>	V <sub>REFCA</sub>	Reference Voltage for CA
27 DQ18	57 V <sub>DD</sub>	87 DQ34	117 SA0	147 DQ23	177 A8	207 DQ39	237 SA1	V <sub>TT</sub>	Termination Voltage
28 DQ19	58 A5	88 DQ35	118 SCL	148 V <sub>SS</sub>	178 A6	208 V <sub>SS</sub>	238 SDA	NC	No Connection
29 V <sub>SS</sub>	59 A4	89 V <sub>SS</sub>	119 SA2	149 DQ28	179 V <sub>DD</sub>	209 DQ44	239 V <sub>SS</sub>		
30 DQ24	60 V <sub>DD</sub>	90 DQ40	120 V <sub>TT</sub>	150 DQ29	180 A3	210 DQ45	240 V <sub>TT</sub>		

\*Not used

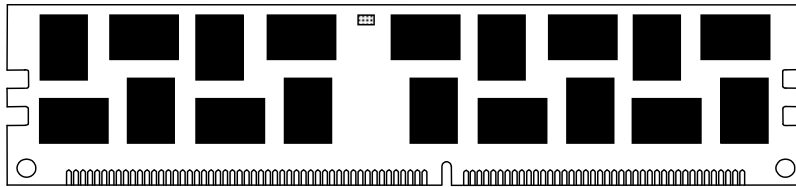
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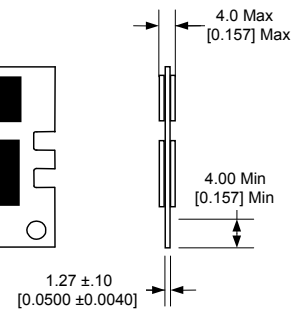
## Front view



## Back view



## Side view



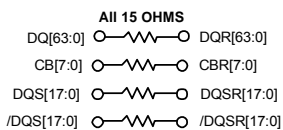
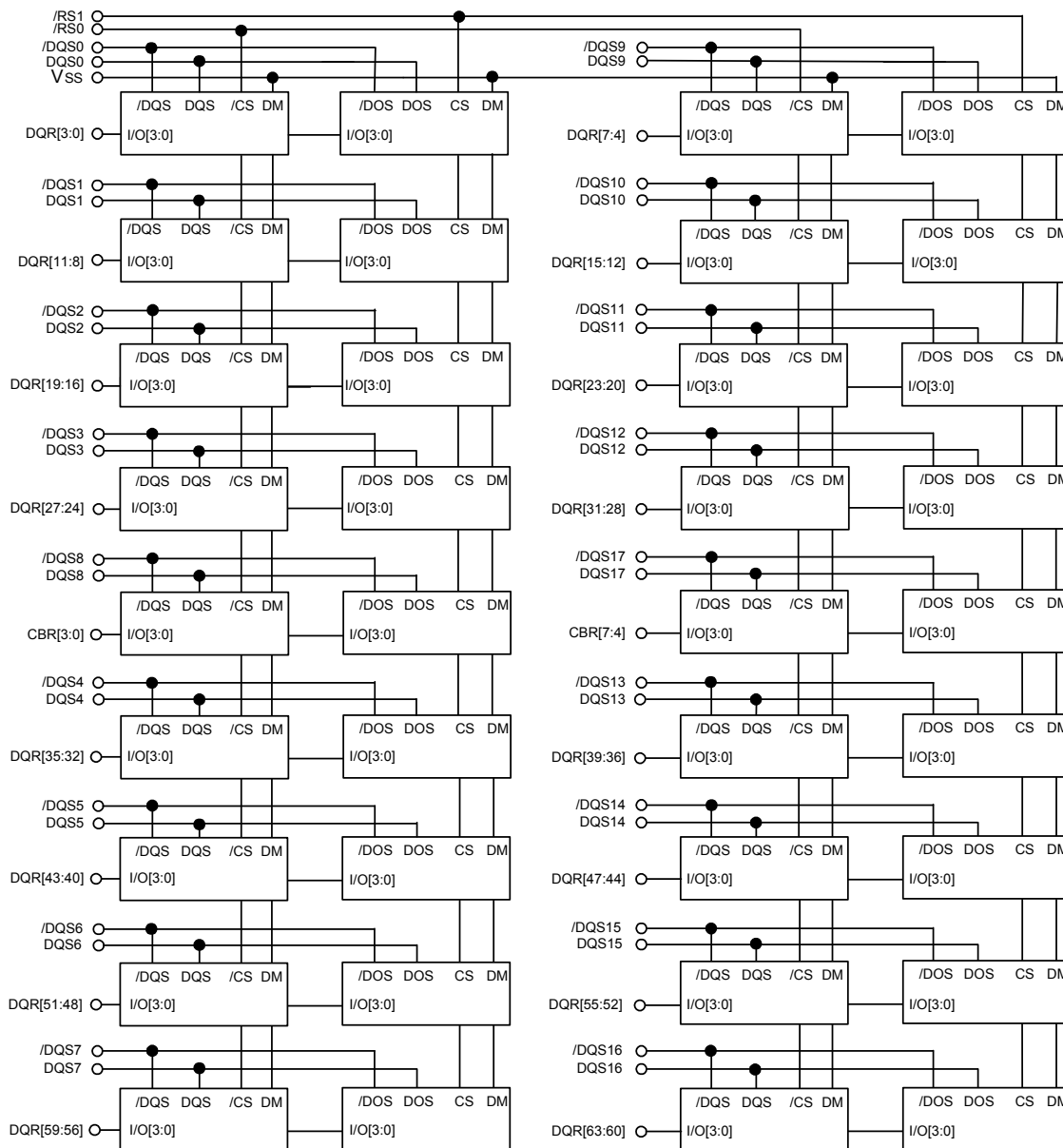
## Notes

Tolerances on all dimensions except where otherwise indicated are  $\pm .13$  (.005).

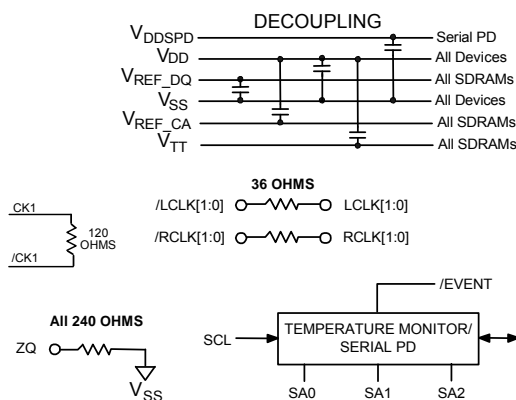
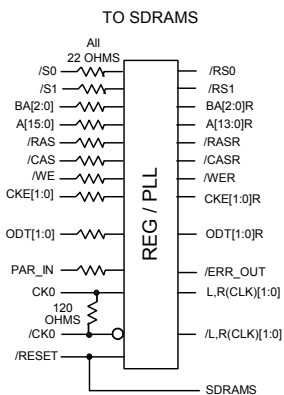
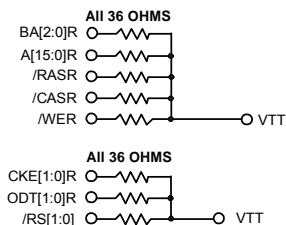
All dimensions are expressed: millimeters [inches]

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**GLOBAL SDRAM CONNECTS**



### Absolute Maximum Ratings

(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	$T_{STORAGE}$	-55	100	C
Ambient Temperature, Operating	$T_A$	0	70	C
DRAM Case Temperature, Operating	$T_{CASE}$	0	95	C
Voltage on $V_{DD}$ relative to $V_{SS}$	$V_{DD}$	-0.4	1.975	V
Voltage on Any Pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.4	1.975	V

Notes:

DRAM Operating Case Temperature above 85C requires 2X refresh.

### Recommended DC Operating Conditions ( $T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Operation Voltage	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	$V_{DD}$	1.35V	1.283	1.35	1.4500	V	
		1.5V	1.425	1.5	1.575		
I/O Reference Voltage	$V_{REFDQ}$	1.35V	0.49 $V_{DD}$	0.50 $V_{DD}$	0.51 $V_{DD}$	V	1
		1.5V					
I/O Reference Voltage	$V_{REFCA}$	1.35V	0.49 $V_{DD}$	0.50 $V_{DD}$	0.51 $V_{DD}$	V	1
		1.5V					

Notes:

1) The value of  $V_{REF}$  is expected to equal one-half  $V_{DD}$  and to track variations in the  $V_{DD}$  DC level. Peak-to-peak noise on  $V_{REF}$  may not exceed  $\pm 1\%$  of its DC value.

### DC Input Logic Levels, Single-Ended ( $T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Operation Voltage	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(DC)}$	1.35V	$V_{REF} + 0.09$	$V_{DD}$	V
		1.5V	$V_{REF} + 0.1$	$V_{DD}$	
Logical Low (Logic 0)	$V_{IL(DC)}$	1.35V	$V_{SS}$	$V_{REF} - 0.09$	V
		1.5V	$V_{SS}$	$V_{REF} - 0.1$	

### AC Input Logic Levels, Single-Ended ( $T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Operation Voltage	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(AC)}$	1.35V	$V_{REF} + 0.160$	-	V
		1.5V	$V_{REF} + 0.175$	-	
Logical Low (Logic 0)	$V_{IL(AC)}$	1.35V	-	$V_{REF} - 0.160$	V
		1.5V	-	$V_{REF} - 0.175$	

### Differential Input Logic Levels ( $T_A = 0$ to $70$ C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Differential Input Logic High	$V_{IH,DIFF}$	+0.200	DC: $V_{DD}$ AC: $V_{DD}+0.4$	V
Differential Input Logic Low	$V_{IL,DIFF}$	DC: $V_{SS}$ AC: $V_{SS}-0.4$	-0.200	V
Differential Input Cross Point Voltage relative to $V_{DD}/2$	$V_{IX}$	- 0.150	+ 0.150	V

### Capacitance ( $T_A = 25$ C, $f = 100$ MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK0, /CK0	$C_{CK}$	2	3	pF
Input Capacitance, Address	BA[2:0], A[15:0], /RAS, /CAS, /WE	$C_i$	1.5	2.5	pF
Input Capacitance Control	/S[1:0], CKE[1:0], ODT[1:0]	$C_i$	1.5	2.5	pF
Input/Output Capacitance	DQ[63:0], CB[7:0] DQS[17:0], /DQS[17:0].	$C_{IO}$	3	5	pF

### DC Characteristics ( $T_A = 0$ to $70$ C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input $0$ V < $V_{IN}$ < $V_{DD}$ )	$I_{IL}$	-18	+18	$\mu$ A	1,2
Output Leakage Current ( $0$ V < $V_{OUT}$ < $V_{DDQ}$ )	$I_{OL}$	-10	+10	$\mu$ A	2,3

Notes:

- 1) All other pins not under test = 0 V
- 2) Values are shown per pin
- 3) DQ, DQS, DQS and ODT are disabled

**I<sub>DD</sub> Specifications and Conditions** (T<sub>A</sub> = 0 to 70 C, Voltage referenced to V<sub>ss</sub> = 0 V)

PARAMETER	Symbol	Test Condition	Max Value		Unit
			1.35V	1.5V	
<b>Operating One Bank Active-Precharge Current</b>	I <sub>DD0</sub> *	Operating current : One bank ACTIVATE-to-PRECHARGE	828	954	mA
<b>Operating One Bank Active-Read-Precharge Current</b>	I <sub>DD1</sub> *	Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE	918	1044	mA
<b>Precharge Power-Down Current</b>	I <sub>DD2P</sub> **	Precharge power down current: (Slow exit)	360	432	mA
<b>Precharge Power-Down Current</b>	I <sub>DD2P</sub> **	Precharge power down current: (Fast exit)	468	540	mA
<b>Precharge Quiet Standby Current</b>	I <sub>DD2Q</sub> **	Precharge quiet standby current	612	648	mA
<b>Precharge Standby Current</b>	I <sub>DD2N</sub> **	Precharge standby current	576	648	mA
<b>Active Power-Down Current</b>	I <sub>DD3P</sub> **	Active power-down current	432	540	mA
<b>Active Standby Current</b>	I <sub>DD3N</sub> **	Active standby current	720	828	mA
<b>Operating Burst Write Current</b>	I <sub>DD4W</sub> *	Burst write operating current	1728	1854	mA
<b>Operating Burst Read Current</b>	I <sub>DD4R</sub> *	Burst read operating current	1638	1854	mA
<b>Burst Refresh Current</b>	I <sub>DD5</sub> *	Refresh current	3168	3204	mA
<b>Self Refresh Current</b>	I <sub>DD6</sub> **	Self-refresh temperature current: MAX T <sub>c</sub> = 85°C	360	432	mA
<b>Operating Bank Interleave Read Current</b>	I <sub>DD7</sub> *	All bank interleaved read current	2448	2664	mA

\* One module rank in this operation the rest in IDD2N.

\*\* Both ranks in this operation.

### AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	$t_{AA}$	13.125	20	ns
CAS-to-CAS Command Delay	$t_{CCD}$	4	-	$t_{CK}$
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	$t_{CK}$
Clock Cycle Time	$t_{CK}$	1.25	1.875	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	$t_{CK}$
Data Input Hold Time after DQS Strobe	$t_{DH}$	45	-	ps
DQ Input Pulse Width	$t_{DIPW}$	360	-	ps
DQS Output Access Time from Clock	$t_{DQSCK}$	-225	+225	ps
Write DQS High Level Width	$t_{DQSH}$	0.45	0.55	$t_{CK(avg)}$
Write DQS Low Level Width	$t_{DQSL}$	0.45	0.55	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	$t_{DQSQ}$	-	125	ps
Data Input Setup Time Before DQS Strobe	$t_{DS}$	10	-	ps
DQS Falling Edge from Clock, Hold Time	$t_{DSH}$	0.2	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	$t_{DSS}$	0.2	-	$t_{CK(avg)}$
Clock Half Period	$t_{HP}$	minimum of $t_{CH}$ or $t_{CL}$	-	ns
Address and Command Hold Time after Clock	$t_{IH}$	120	-	ps
Address and Command Setup Time before Clock	$t_{IS}$	45	-	ps
Load Mode Command Cycle Time	$t_{MRD}$	4	-	$t_{CK}$
DQ-to-DQS Hold	$t_{QH}$	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	$t_{RAS}$	35	$9 \cdot t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	$t_{RC}$	49.125	-	ns
RAS-to-CAS Delay	$t_{RCD}$	13.125	-	ns
Average Periodic Refresh Interval $0^{\circ}C \leq T_{CASE} < 85^{\circ}C$	$t_{REFI}$	-	7.8	$\mu s$
Average Periodic Refresh Interval $0^{\circ}C \leq T_{CASE} < 95^{\circ}C$	$t_{REFI}$	-	3.9	$\mu s$
Auto Refresh Row Cycle Time	$t_{RFC}$	160	-	ns
Row Precharge Time	$t_{RP}$	13.125	-	ns
Read DQS Preamble Time	$t_{RPRE}$	0.9	Note-1	$t_{CK(avg)}$
Read DQS Postamble Time	$t_{RPST}$	0.3	Note-2	$t_{CK(avg)}$
Row Active to Row Active Delay	$t_{RRD}$	Max(4nCK, 6ns)	-	ns
Internal Read to Precharge Command Delay	$t_{RTP}$	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	$t_{WPRE}$	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	$t_{WPST}$	0.3	-	$t_{CK(avg)}$
Write Recovery Time	$t_{WR}$	15	-	ns
Internal Write to Read Command Delay	$t_{WTR}$	Max(4nCK, 7.5ns)	-	ns

Notes:

1. The maximum preamble is bound by  $t_{LZDQS}(\min)$
2. The maximum postamble is bound by  $t_{HZDQS}(\max)$



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