

# DTM64370D

## 4GB - 240-Pin 2Rx8 Registered ECC DDR3 DIMM



### Identification

DTM64370D 512Mx72  
 4GB 2Rx8 PC3-12800R-11-11-B1

### Performance range

Clock / Module Speed / CL-t<sub>RCD</sub> -t<sub>RP</sub>

800 MHz / PC3-12800 / 11-11-11  
 667 MHz / PC3-10600 / 10-10-10  
 667 MHz / PC3-10600 / 9-9-9  
 533 MHz / PC3-8500 / 8-8-8  
 533 MHz / PC3-8500 / 7-7-7  
 400 MHz / PC3-6400 / 6-6-6

### Features

240-pin JEDEC-compliant DIMM, 133.35 mm wide by 30 mm high

Operating Voltage: 1.5V ± 0.075

I/O Type: SSTL\_15

On-board I2C temperature sensor with integrated serial presence-detect (SPD) EEPROM

Data Transfer Rate: 12.8 Gigabytes/sec

Data Bursts: 8 and burst chop 4 mode

ZQ Calibration for Output Driver and On-Die Termination (ODT)

Programmable ODT / Dynamic ODT during Writes

Programmable CAS Latency: 6, 7, 8, 9, 10 and 11

Bi-Directional Differential Data Strobe signals

SDRAM Addressing (Row/Col/Bank): 15/10/3

Fully RoHS Compliant

### Description

DTM64370D is a registered 512Mx72 memory module, which conforms to JEDEC's DDR3, PC3-12800 standard. The assembly is Dual-Rank. Each Rank is comprised of nine 256Mx8 DDR3 Hynix SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect and a combination register/PLL, with Address and Command Parity, is also used.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals in a Fly-by topology.

A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.

### Pin Configuration

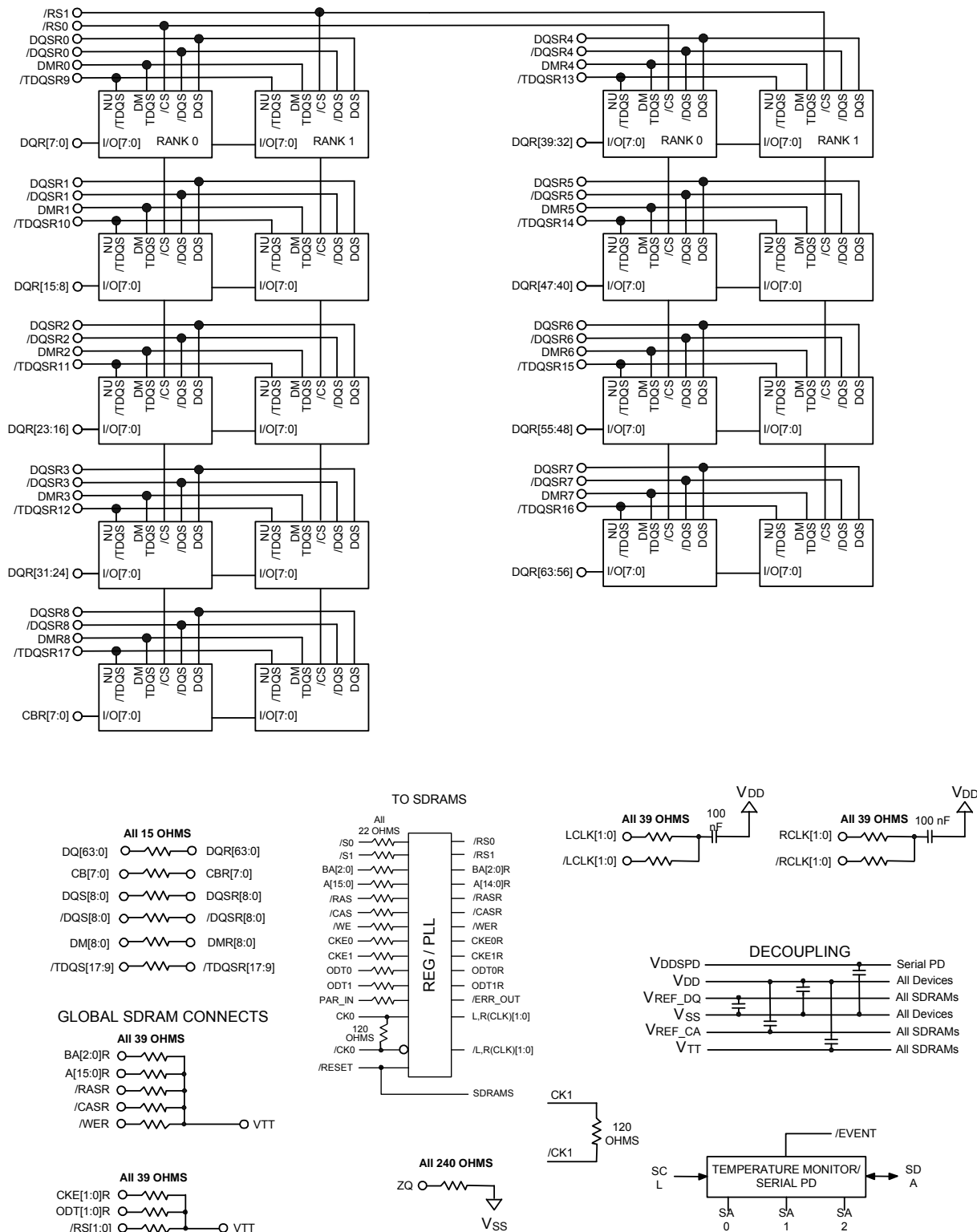
Front Side			Back Side		
1 V <sub>REFDQ</sub>	31 DQ25	61 A2	91 DQ41	121 V <sub>SS</sub>	151 V <sub>SS</sub>
2 V <sub>SS</sub>	32 V <sub>SS</sub>	62 V <sub>DD</sub>	92 V <sub>SS</sub>	122 DQ4	152 DM3
3 DQ0	33 /DQS3	63 CK1*	93 /DQS5	123 DQ5	153 NC
4 DQ1	34 DQS3	64 /CK1*	94 DQS5	124 V <sub>SS</sub>	154 V <sub>SS</sub>
5 V <sub>SS</sub>	35 V <sub>SS</sub>	65 V <sub>DD</sub>	95 V <sub>SS</sub>	125 DM0	155 DQ30
6 /DQS0	36 DQ26	66 V <sub>DD</sub>	96 DQ42	126 NC	156 DQ31
7 DQS0	37 DQ27	67 V <sub>REFCA</sub>	97 DQ43	127 V <sub>SS</sub>	157 V <sub>SS</sub>
8 V <sub>SS</sub>	38 V <sub>SS</sub>	68 P <sub>AR_IN</sub>	98 V <sub>SS</sub>	128 DQ6	158 CB4
9 DQ2	39 CB0	69 VDD	99 DQ48	129 DQ7	159 CB5
10 DQ3	40 CB1	70 A10/AP	100 DQ49	130 V <sub>SS</sub>	160 V <sub>SS</sub>
11 V <sub>SS</sub>	41 V <sub>SS</sub>	71 BA0	101 V <sub>SS</sub>	131 DQ12	161 DM8
12 DQ8	42 /DQS8	72 V <sub>DD</sub>	102 /DQS6	132 DQ13	162 NC
13 DQ9	43 DQS8	73 /WE	103 DQS6	133 V <sub>SS</sub>	163 V <sub>SS</sub>
14 V <sub>SS</sub>	44 V <sub>SS</sub>	74 /CAS	104 V <sub>SS</sub>	134 DM1	164 CB6
15 /DQS1	45 CB2	75 V <sub>DD</sub>	105 DQ50	135 NC	165 CB7
16 DQS1	46 CB3	76 /S1	106 DQ51	136 V <sub>SS</sub>	166 V <sub>SS</sub>
17 V <sub>SS</sub>	47 V <sub>SS</sub>	77 ODT1	107 V <sub>SS</sub>	137 DQ14	167 NC (TEST)
18 DQ10	48 V <sub>TT</sub>	78 V <sub>DD</sub>	108 DQ56	138 DQ15	168 /RESET
19 DQ11	49 V <sub>TT</sub>	79 /S2, NC*	109 DQ57	139 V <sub>SS</sub>	169 CKE1
20 V <sub>SS</sub>	50 CKE0	80 V <sub>SS</sub>	110 V <sub>SS</sub>	140 DQ20	170 V <sub>DD</sub>
21 DQ16	51 V <sub>DD</sub>	81 DQ32	111 /DQS7	141 DQ21	171 A15
22 DQ17	52 BA2	82 DQ33	112 DQS7	142 V <sub>SS</sub>	172 A14
23 V <sub>SS</sub>	53 /ERR_OUT	83 V <sub>SS</sub>	113 V <sub>SS</sub>	143 DM2	173 V <sub>DD</sub>
24 /DQS2	54 V <sub>DD</sub>	84 /DQS4	114 DQ58	144 NC	174 A12/BC
25 DQS2	55 A11	85 DQS4	115 DQ59	145 V <sub>SS</sub>	175 A9
26 V <sub>SS</sub>	56 A7	86 V <sub>SS</sub>	116 V <sub>SS</sub>	146 DQ22	176 V <sub>DD</sub>
27 DQ18	57 V <sub>DD</sub>	87 DQ34	117 SA0	147 DQ23	177 A8
28 DQ19	58 A5	88 DQ35	118 SCL	148 V <sub>SS</sub>	178 A6
29 V <sub>SS</sub>	59 A4	89 V <sub>SS</sub>	119 SA2	149 DQ28	179 V <sub>DD</sub>
30 DQ24	60 V <sub>DD</sub>	90 DQ40	120 V <sub>T</sub>	150 DQ29	180 A3

\*Not used

### Pin Description

Name	Function
CB[7:0]	Data Check Bits
DQ[63:0]	Data Bits
DQS[8:0], /DQS[8:0]	Differential Data Strobes
DM[8:0]	Data Mask
/TDQS[17:9]	Termination strobes
CK[1:0], /CK[1:0]	Differential Clock Inputs
CKE[1:0]	Clock Enables
/CAS	Column Address Strobe
/RAS	Row Address Strobe
/S[3:0]	Chip Selects
/WE	Write Enable
A[15:0]	Address Inputs
BA[2:0]	Bank Addresses
ODT[1:0]	On Die Termination Inputs
SA[2:0]	SPD Address
SCL	SPD Clock Input
SDA	SPD Data Input/Output
/EVENT	Temperature Sensing
/RESET	Reset for register and DRAMs
PAR_IN	Parity bit for Addr/Ctrl
/ERR_OUT	Error bit for Parity Error
A12/BC	Combination input: Addr12/Burst Chop
A10/AP	Combination input: Addr10/Auto-precharge
V <sub>SS</sub>	Ground
V <sub>DD</sub>	Power
V <sub>DDSPD</sub>	SPD EEPROM Power
V <sub>REFDQ</sub>	Reference Voltage for DQ's
V <sub>REFCA</sub>	Reference Voltage for CA
V <sub>TT</sub>	Termination Voltage
NC	No Connection





### Absolute Maximum Ratings

(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	T <sub>STORAGE</sub>	-55	100	C
Ambient Temperature, Operating	T <sub>A</sub>	0	70	C
DRAM Case Temperature, Operating	T <sub>CASE</sub>	0	95	C
Voltage on V <sub>DD</sub> relative to V <sub>SS</sub>	V <sub>DD</sub>	-0.4	1.975	V
Voltage on Any Pin relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.4	1.975	V

Notes:

DRAM Operating Case Temperature above 85C requires 2X refresh.

### Recommended DC Operating Conditions (T<sub>A</sub> = 0 to 70 C, Voltage referenced to V<sub>SS</sub> = 0 V)

PARAMETER	Symbol	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V <sub>DD</sub>	1.425	1.5	1.575	V	
I/O Reference Voltage	V <sub>REFDQ</sub>	0.49 V <sub>DD</sub>	0.50 V <sub>DD</sub>	0.51 V <sub>DD</sub>	V	1
I/O Reference Voltage	V <sub>REFCA</sub>	0.49 V <sub>DD</sub>	0.50 V <sub>DD</sub>	0.51 V <sub>DD</sub>	V	1

Notes:

1) The value of V<sub>REF</sub> is expected to equal one-half V<sub>DD</sub> and to track variations in the V<sub>DD</sub> DC level. Peak-to-peak noise on V<sub>REF</sub> may not exceed ±1% of its DC value. For Reference V<sub>DD</sub>/2 ± 15 mV.

### DC Input Logic Levels, Single-Ended (T<sub>A</sub> = 0 to 70 C, Voltage referenced to V<sub>SS</sub> = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	V <sub>IH(DC)</sub>	V <sub>REF</sub> + 0.1	V <sub>DD</sub>	V
Logical Low (Logic 0)	V <sub>IL(DC)</sub>	V <sub>SS</sub>	V <sub>REF</sub> - 0.1	V

### AC Input Logic Levels, Single-Ended (T<sub>A</sub> = 0 to 70 C, Voltage referenced to V<sub>SS</sub> = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	V <sub>IH(AC)</sub>	V <sub>REF</sub> + 0.175	-	V
Logical Low (Logic 0)	V <sub>IL(AC)</sub>	-	V <sub>REF</sub> - 0.175	V

### Differential Input Logic Levels ( $T_A = 0$ to $70$ C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Differential Input Logic High	$V_{IH,DIFF}$	+0.200	DC: $V_{DD}$ AC: $V_{DD}+0.4$	V
Differential Input Logic Low	$V_{IL,DIFF}$	DC: $V_{SS}$ AC: $V_{SS}-0.4$	-0.200	V
Differential Input Cross Point Voltage relative to $V_{DD}/2$	$V_{IX}$	- 0.150	+ 0.150	V

### Capacitance ( $T_A = 25$ C, $f = 100$ MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK0, /CK0	$C_{CK}$	1.5	2.5	pF
Input Capacitance, Address	BA[2:0], A[15:0], /RAS, /CAS, /WE	$C_I$	1.5	2.5	pF
Input Capacitance Control	/S[1:0], CKE[1:0], ODT[1:0]	$C_I$	1.5	2.5	pF
Input/Output Capacitance	DQ[63:0], CB[7:0] DQS[8:0], /DQS[8:0], DM[8:0], TDQS[17:9]	$C_{IO}$	3	5	pF

### DC Characteristics ( $T_A = 0$ to $70$ C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input $0$ V < $V_{IN}$ < $V_{DD}$ )	$I_{IL}$	-18	+18	$\mu$ A	1,2
Output Leakage Current ( $0$ V < $V_{OUT}$ < $V_{DDQ}$ )	$I_{OL}$	-10	+10	$\mu$ A	2,3

Notes:

- 1) All other pins not under test = 0 V
- 2) Values are shown per pin
- 3) DQ, DQS, DQS and ODT are disabled

**I<sub>DD</sub> Specifications and Conditions** (T<sub>A</sub> = 0 to 70 C, Voltage referenced to V<sub>SS</sub> = 0 V)

PARAMETER	Symbol	Test Condition	Max Value	Unit
Operating One Bank Active-Precharge Current	I <sub>DD0</sub> *	Operating current : One bank ACTIVATE-to-PRECHARGE	423	mA
Operating One Bank Active-Read-Precharge Current	I <sub>DD1</sub> *	Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE	468	mA
Precharge Power-Down Current	I <sub>DD2P</sub> **	Precharge power down current: (Slow exit)	216	mA
Precharge Power-Down Current	I <sub>DD2P</sub> **	Precharge power down current: (Fast exit)	270	mA
Precharge Quiet Standby Current	I <sub>DD2Q</sub> **	Precharge quiet standby current	324	mA
Precharge Standby Current	I <sub>DD2N</sub> **	Precharge standby current	324	mA
Active Power-Down Current	I <sub>DD3P</sub> **	Active power-down current	270	mA
Active Standby Current	I <sub>DD3N</sub> **	Active standby current	414	mA
Operating Burst Write Current	I <sub>DD4W</sub> *	Burst write operating current	873	mA
Operating Burst Read Current	I <sub>DD4R</sub> *	Burst read operating current	873	mA
Burst Refresh Current	I <sub>DD5</sub> **	Refresh current	2880	mA
Self Refresh Current	I <sub>DD6</sub> **	Self-refresh temperature current: MAX T <sub>C</sub> = 85°C	216	mA
Operating Bank Interleave Read Current	I <sub>DD7</sub> *	All bank interleaved read current	1278	mA

\* One module rank in this operation the rest in IDD2P slow exit.

\*\* All module ranks in this operation.

### AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	$t_{AA}$	13.75(13.125)	20	ns
CAS-to-CAS Command Delay	$t_{CCD}$	4	-	$t_{CK}$
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	$t_{CK}$
Clock Cycle Time	$t_{CK}$	1.25	2.5	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	$t_{CK}$
Data Input Hold Time after DQS Strobe	$t_{DH}$	45	-	ps
DQ Input Pulse Width	$t_{DIPW}$	360	-	ps
DQS Output Access Time from Clock	$t_{DQSCK}$	-225	+225	ps
Write DQS High Level Width	$t_{DQSH}$	0.45	0.55	$t_{CK(avg)}$
Write DQS Low Level Width	$t_{DQSL}$	0.45	0.55	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	$t_{DQSQ}$	-	100	ps
Data Input Setup Time Before DQS Strobe	$t_{DS}$	10	-	ps
DQS Falling Edge from Clock, Hold Time	$t_{DSH}$	0.18	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	$t_{DSS}$	0.18	-	$t_{CK(avg)}$
Clock Half Period	$t_{HP}$	minimum of $t_{CH}$ or $t_{CL}$	-	ns
Address and Command Hold Time after Clock	$t_{IH}$	120	-	ps
Address and Command Setup Time before Clock	$t_{IS(AC150)}$	45	-	ps
Load Mode Command Cycle Time	$t_{MRD}$	4	-	$t_{CK}$
DQ-to-DQS Hold	$t_{QH}$	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	$t_{RAS}$	35	$9 \cdot t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	$t_{RC}$	48.75(48.125)	-	ns
RAS-to-CAS Delay	$t_{RCD}$	13.75(13.125)	-	ns
Average Periodic Refresh Interval $0^{\circ}C \leq T_{CASE} < 85^{\circ}C$	$t_{REFI}$	-	7.8	$\mu s$
Average Periodic Refresh Interval $0^{\circ}C \leq T_{CASE} < 95^{\circ}C$	$t_{REFI}$	-	3.9	$\mu s$
Auto Refresh Row Cycle Time	$t_{RFC}$	160	-	ns
Row Precharge Time	$t_{RP}$	13.75(13.125)	-	ns
Read DQS Preamble Time	$t_{RPRE}$	0.9	Note-1	$t_{CK(avg)}$
Read DQS Postamble Time	$t_{RPST}$	0.3	Note-2	$t_{CK(avg)}$
Row Active to Row Active Delay	$t_{RRD}$	Max(4nCK, 6ns)	-	ns
Internal Read to Precharge Command Delay	$t_{RTP}$	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	$t_{WPRE}$	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	$t_{WPST}$	0.3	-	$t_{CK(avg)}$
Write Recovery Time	$t_{WR}$	15	-	ns
Internal Write to Read Command Delay	$t_{WTR}$	Max(4nCK, 7.5ns)	-	ns

Notes:

1. The maximum preamble is bound by  $t_{LZDQS}(\min)$
2. The maximum postamble is bound by  $t_{HZDQS}(\max)$

### SERIAL PRESENCE DETECT MATRIX

Byte#	Function.	Value	Hex
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage.		0x92
	Bit 3 ~ Bit 0. SPD Bytes Used -	176	
	Bit 6 ~ Bit 4. SPD Bytes Total -	256	
	Bit 7. CRC Coverage -	Bytes 0-116	
1	SPD Revision.	Rev. 1.1	0x11
2	Key Byte / DRAM Device Type.	DDR3 SDRAM	0x0B
3	Key Byte / Module Type.		0x01
	Bit 3 ~ Bit 0. Module Type -	RDIMM	
	Bit 7 ~ Bit 4. Reserved -	0	
4	SDRAM Density and Banks.		0x03
	Bit 3 ~ Bit 0. Total SDRAM capacity, in megabits -	2Gb	
	Bit 6 ~ Bit 4. Bank Address Bits -	8 banks	
	Bit 7. Reserved -	0	
5	SDRAM Addressing.		0x19
	Bit 2 ~ Bit 0. Column Address Bits -	10	
	Bit 5 ~ Bit 3. Row Address Bits -	15	
	Bit 7, 6. Reserved	0	
6	Module Nominal Voltage, VDD.		0x00
	Bit 0. NOT 1.5 V operable -		
	Bit 1. 1.35 V operable -		
	Bit 2. 1.2X V operable -		
	Bit 3. Reserved -		
	Bit 4. Reserved -		
	Bit 5. Reserved -		
	Bit 6. Reserved -		
Bit 7. Reserved -			
7	Module Organization.		0x09
	Bit 2 ~ Bit 0. SDRAM Device Width -	8-Bits	
	Bit 5 ~ Bit 3. Number of Ranks -	2-Rank	
	Bit 7, 6. Reserved	0	
8	Module Memory Bus Width.		0x0B
	Bit 2 ~ Bit 0. Primary bus width, in bits -	64-Bits	
	Bit 4, Bit 3. Bus width extension, in bits -	8-Bits	
	Bit 7 ~ Bit 5. Reserved -	0	
9	Fine Timebase (FTB) Dividend / Divisor.		0x52
	Bit 3 ~ Bit 0. Fine Timebase (FTB) Divisor	2	
	Bit 7 ~ Bit 4. Fine Timebase (FTB) Dividend	5	
10	Medium Timebase (MTB) Dividend.	1 (MTB = 0.125ns)	0x01

11	Medium Timebase (MTB) Divisor.	8 (MTB = 0.125ns)	0x08
12	SDRAM Minimum Cycle Time (tCKmin).	1.25ns	0x0A
13	Reserved.	UNUSED	0x00
14	CAS Latencies Supported, Least Significant Byte.		0xFC
	Bit 0. CL = 4 -		
	Bit 1. CL = 5 -		
	Bit 2. CL = 6 -	X	
	Bit 3. CL = 7 -	X	
	Bit 4. CL = 8 -	X	
	Bit 5. CL = 9 -	X	
	Bit 6. CL = 10 -	X	
Bit 7. CL = 11 -	X		
15	CAS Latencies Supported, Most Significant Byte.		0x00
	Bit 0. CL = 12 -		
	Bit 1. CL = 13 -		
	Bit 2. CL = 14 -		
	Bit 3. CL = 15 -		
	Bit 4. CL = 16 -		
	Bit 5. CL = 17 -		
	Bit 6. CL = 18 -		
Bit 7. Reserved.			
16	Minimum CAS Latency Time (tAamin).	13.125ns	0x69
17	Minimum Write Recovery Time (tWRmin).	15.0ns	0x78
18	Minimum RAS# to CAS# Delay Time (tRCDmin).	13.125ns	0x69
19	Minimum Row Active to Row Active Delay Time (tRRDmin).	6.0ns	0x30
20	Minimum Row Precharge Delay Time (tRPmin).	13.125ns	0x69
21	Upper Nibbles for tRAS and tRC.		0x11
	Bit 3 ~ Bit 0. tRAS Most Significant Nibble -	1	
	Bit 7 ~ Bit 4. tRC Most Significant Nibble -	1	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte.	35.0ns	0x18
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte.	48.125ns	0x81
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte.	160.0ns	0x00
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte.	160.0ns	0x05
26	Minimum Internal Write to Read Command Delay Time (tWTRmin).	7.5ns	0x3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin).	7.5ns	0x3C
28	Upper Nibble for tFAW.		0x00
	Bit 3 ~ Bit 0. tFAW Most Significant Nibble -	0	

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		Bit 7 ~ Bit 4. Reserved -	0	
29	Minimum Four Activate Window Delay Time (tFAWmin), Least Significant Byte.		30.0ns	0xF0
30	SDRAM Optional Features.			0x83
		Bit 0. RZQ / 6 -	X	
		Bit 1. RZQ / 7 -	X	
		Bit 2. Reserved -		
		Bit 3. Reserved -		
		Bit 4. Reserved -		
		Bit 5. Reserved -		
		Bit 6. Reserved -		
		Bit 7. DLL-Off Mode Support -	X	
31	SDRAM Drivers Supported.			0x01
		Extended Temperature Range -	X	
		Extended Temperature Refresh Rate -		
		Auto Self Refresh (ASR) -		
		On-die Thermal Sensor (ODTS) Readout -		
		Reserved -		
		Reserved -		
		Reserved -		
		Partial Array Self Refresh (PASR) -		
32	Module Thermal Sensor.			0x80
		Bit 6 ~ Bit 0. Thermal Sensor Accuracy -	0	
		Bit 7. Thermal Sensor -	With TS	
33	SDRAM Device Type.			0x00
		Bit 1 ~ Bit 0. Signal Loading -	Not specified	
		Bit 3 ~ Bit 2. Reserved. 0-Undefined -	0	
		Bit 6 ~ Bit 4. Die Count. -	Not specified	
		Bit 7. SDRAM Device Type -	Std Mono	
34	Fine Offset for SDRAM Minimum Cycle Time (tCKmin) -		UNUSED	0x00
35	Fine Offset for Minimum CAS Latency Time (tAamin) -		UNUSED	0x00
36,37	Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin) -		UNUSED	0x00
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin) -		UNUSED	0x00
39-59	Reserved		UNUSED	0x00
60	Module Nominal Height.			0x0F
		Bit 4 ~ Bit 0. Module Nominal Height max, in mm -	29<h<=30	
		Bit 7 ~ Bit5. Reserved -	0	
61	Module Maximum Thickness.			0x11
		Bit 3 ~ Bit 0. Front, in mm (baseline thickness = 1 mm) -	1<th<=2	
		Bit 7 ~ Bit 4. Back, in mm (baseline thickness = 1 mm) -	1<th<=2	
62	Reference Raw Card Used.			0x01

	Bit 4 ~ Bit 0. Reference Raw Card -	R/C B	
	Bit 6, Bit 5. Reference Raw Card Revision -	Rev.0	
	Bit 7. Reserved -	A-AL	
63	(Registered) DIMM Module Attributes.		0x05
	Bit 1 ~ Bit 0. # of Registers used on RDIMM -	1 Register	
	Bit 3 ~ Bit 2. # of Rows of DRAMs on RDIMM -	1 Row	
	Bit 7 ~ Bit 4. Reserved -	0	
64	RDIMM Thermal Heat Spreader Solution.		0x00
	Bit 6 ~ Bit 0. Heat Spreader Thermal Characteristics -	0	
	Bit 7. Heat Spreader Solution -	No HS	
65	Register Manufacturer ID Code, Least Significant Byte (Optional).		0x00
66	Register Manufacturer ID Code, Most Significant Byte (Optional).		0x00
67	Register Revision Number (Optional).		0xFF
68	Register Type.		0x00
	Bit[2-0] Support Device -	SSTE32882	
	Bit[7-3] Reserved -	0	
69	[SSTE32882]: RC1 (MS Nibble) / RC0 (LS Nibble)	UNUSED	0x00
70	[SSTE32882]: RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address.		0x50
	Bit 1, Bit 0. RC2/DA3,4 Value.-	RESERVED	
	Bit 3, Bit 2. RC2/DBA0,1 Value -	RESERVED	
	Bit 5, Bit 4. RC3/DA4,3 value, Command/Address A Outputs -	Moderate	
	Bit 7, Bit 6. RC3/DBA0,1 value, Command/Address B Outputs -	Moderate	
71	[SSTE32882]: RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock.		0x00
	Bit 1, Bit 0. RC4/DA3,4 Control Signals, A Outputs.-	Light	
	Bit 3, Bit 2. RC4/DBA0,1 Control Signals, B Outputs -	Light	
	Bit 5, Bit 4. RC5/DA4,3 value, Y1/Y1# and Y3/Y3# Clock Outputs -	Light	
	Bit 7, Bit 6. RC5/DBA0,1 value, Y0/Y0# and Y2/Y2# Clock Outputs -	Light	
72	[SSTE32882]: RC7 (MS Nibble) / RC6 (LS Nibble).	UNUSED	0x00
73	[SSTE32882]: RC9 (MS Nibble) / RC8 (LS Nibble).	UNUSED	0x00
74	[SSTE32882]: RC11 (MS Nibble) / RC10 (LS Nibble).	UNUSED	0x00
75	[SSTE32882]: RC13 (MS Nibble) / RC12 (LS Nibble).	UNUSED	0x00
76	[SSTE32882]: RC15 (MS Nibble) / RC14 (LS Nibble).	UNUSED	0x00
77-116	Module-Specific Section		UNUSED
117	Module Manufacturer ID Code, Least Significant Byte	DATARAM	0x01
118	Module Manufacturer ID Code, Most Significant Byte	DATARAM	0x91
119	Module Manufacturing Location		0x00
120,121	Module Manufacturing Date		0x20
122-125	Module Serial Number		0x20

# DTM64370D

## 4GB - 240-Pin 2Rx8 Registered ECC DDR3 DIMM

126	Cyclical Redundancy Code (CRC).	CRC	0x95
127	Cyclical Redundancy Code (CRC).	CRC	0x50
128-131	Module Part Number		0x20
132	Module Part Number	D	0x44
133	Module Part Number	A	0x41
134	Module Part Number	T	0x54
135	Module Part Number	A	0x41
136	Module Part Number	R	0x52
137	Module Part Number	A	0x41
138	Module Part Number	M	0x4D
139	Module Part Number		0x20
140	Module Part Number	6	0x36
141	Module Part Number	4	0x34
142	Module Part Number	3	0x33
143	Module Part Number	7	0x37
144	Module Part Number	0	0x30
145	Module Part Number		0x20
146,147	Module Revision Code		0x20
148	DRAM Manufacturer ID Code, Least Significant Byte		0x00
149	DRAM Manufacturer ID Code, Most Significant Byte		0x00
150-175	Manufacturer's Specific Data	UNUSED	0x00
176-255	Open for customer use	UNUSED	0x00

Bytes 122 – 125 change per DIMM.



# DTM64370D

4GB - 240-Pin 2Rx8 Registered ECC DDR3 DIMM

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