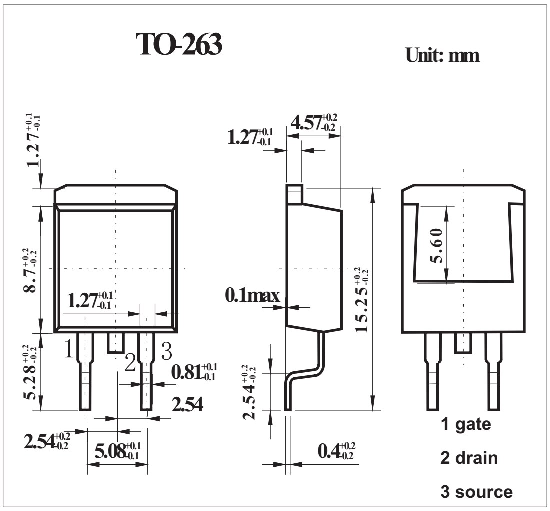
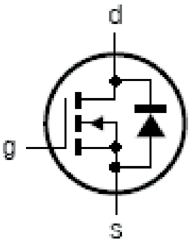
TrenchMOS™ standard level FET

KUK7604-40A



■ Features

- TrenchMOS™ technology
- Q101 compliant
- 175℃ rated
- Standard level compatible.



■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
drain-source voltage (DC)	V_{DS}	40	V
drain-gate voltage (DC) R_{GS} = 20 kΩ	V_{DGR}	40	V
gate-source voltage (DC)	V_{GS}	±20	V
drain current (DC) T_{mb} = 25℃; V_{GS} = 10 V	I_D	198	A
drain current (DC) T_{mb} = 100℃; V_{GS} = 10 V		75	A
peak drain current *1	I_{DM}	794	A
total power dissipation T_{mb} = 25 ℃	P_{tot}	300	W
storage temperature	T_{stg}	-55 to 175	℃
operating junction temperature	T_j	-55 to 175	℃
reverse drain current (DC) T_{mb} = 25℃	I_{DR}	198	A
		75	A
pulsed reverse drain current *2	I_{DRM}	794	A
non-repetitive avalanche energy	W_{DSS}	1.6	J
thermal resistance from junction to ambient	$R_{th(j-a)}$	50	K/W
thermal resistance from junction to mounting base	$R_{th(j-mb)}$	0.5	K/W

*1 T_{mb} = 25℃; pulsed; $t_p \leqslant$ 10 μs;

*2 unclamped inductive load; I_D =75 A;$V_{DS} \leqslant$ 40 V; V_{GS} = 10 V; R_{GS} = 50Ω,starting T_{mb}= 25℃

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
drain-source breakdown voltage	$V_{(BR)DSS}$	I_D = 0.25 mA; V_{GS} = 0 V;T_j = 25℃	40			V
		I_D = 0.25 mA; V_{GS} = 0 V;T_j = -55℃	36			V
gate-source threshold voltage	$V_{GS(th)}$	I_D = 1 mA; V_{DS} = V_{GS};T_j = 25℃	2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS};T_j = 175℃	1			V
		I_D = 1 mA; V_{DS} = V_{GS};T_j = -55℃			4.4	V
drain-source leakage current	I_{DSS}	V_{DS} = 40 V; V_{GS} = 0 V;T_j = 25℃		0.05	10	mA
		V_{DS} = 40 V; V_{GS} = 0 V;T_j = 175℃			500	mA
gate-source leakage current	I_{GSS}	V_{GS} = ±20 V; V_{DS} = 0 V		2	100	nA
drain-source on-state resistance	R_{DSon}	V_{GS} = 10 V; I_D = 25 A;T_j = 25℃		3.9	4.5	mΩ
		V_{GS} = 10 V; I_D = 25 A;T_j = 175℃			8.5	mΩ
total gate charge	$Q_{g(tot)}$	V_{GS} = 10 V; V_{DD} = 32 V;I_D = 25 A		117		nC
gate-to-source charge	Q_{gs}			19		nC
gate-to-drain (Miller) charge	Q_{gd}			50		nC
input capacitance	C_{iss}	V_{GS} = 0 V; V_{DS} = 25 V;f = 1 MHz		4300	5730	pF
output capacitance	C_{oss}			1400	1680	pF
reverse transfer capacitance	C_{rss}			800	1100	pF
turn-on delay time	$t_{d(on)}$	V_{DD} = 30 V; R_L = 1.2Ω;V_{GS} = 10 V; R_G = 10Ω		33		ns
rise time	t_r			110		ns
turn-off delay time	$t_{d(off)}$			151		ns
fall time	t_f			76		ns
internal drain inductance	L_d	from drain lead 6 mm from package to centre of die		4.5		nH
				2.5		nH
internal source inductance	L_s	from source lead to source bond pad		7.5		nH
source-drain (diode forward) voltage	V_{SD}	I_S = 40 A; V_{GS} = 0 V;		0.85	1.2	V
reverse recovery time	t_{rr}	I_S = 20 A;dI_S/dt = -100 A/µs		96		ns
recovered charge	Q_r	V_{GS} = -10 V; V_{DS} = 30 V		224		nC