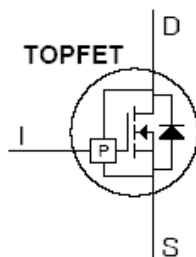
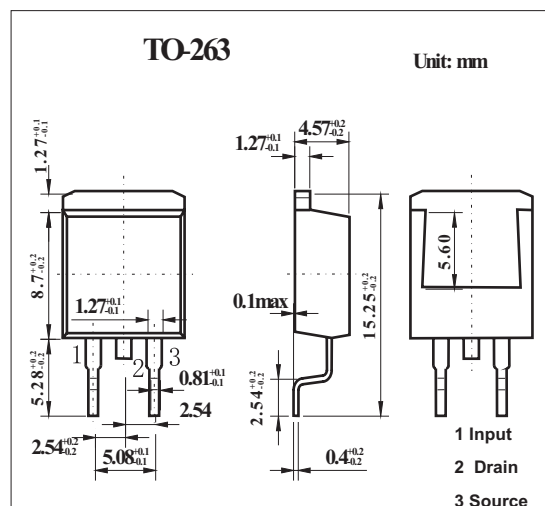


Logic level TOPFET

KUK130-50DL

■ Features

- TrenchMOS output stage
- Current limiting
- Overload protection
- Overtemperature protection
- Protection latched reset by input
- 5 V logic compatible input level
- Control of output stage and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Continuous drain source voltage	V_{DS}	50	V
Continuous drain current $V_{IS} = 5\text{ V}$; $T_{mb} = 25^\circ\text{C}$	I_D	selflimited	A
Continuous drain current $V_{IS} = 5\text{ V}$; $T_{mb} \leq 121^\circ\text{C}$	I_D	20	A
Continuous input current	I_I	-5 to 5	mA
Repetitive peak input current *1	I_{IRM}	-50 to 50	mA
Total power dissipation $T_{mb} \leq 25^\circ\text{C}$	P_D	90	W
Storage temperature	T_{stg}	-55 To 175	$^\circ\text{C}$
Continuous junction temperature2 normal operation	T_j	150	$^\circ\text{C}$
Case temperature during soldering	T_{sold}	260	$^\circ\text{C}$
Electrostatic discharge capacitor voltage *2	V_C	2	kV

*1 $\delta \leq 0.1$, $t_p = 300\text{ }\mu\text{s}$

*2 $C = 250\text{ pF}$; $R = 1.5\text{ k}\Omega$

KUK130-50DL

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Non-repetitive clamping energy	EDSM	$I_{DM} = 20\text{ A}$; $V_{DD} \leq 20\text{ V}$; $T_{mb} \leq 25^\circ\text{C}$			350	mJ
Repetitive clamping energy	EDRM	$I_{DM} = 20\text{ A}$; $V_{DD} \leq 20\text{ V}$; $T_{mb} \leq 95^\circ\text{C}$; $f = 250\text{ Hz}$			45	mJ
Drain source voltage	V_{DS}	$4\text{ V} \leq V_{IS} \leq 5.5\text{ V}$	0		35	V
Drain-source clamping voltage	$V_{(CL)DSS}$	$V_{IS} = 0\text{ V}$; $I_D = 10\text{ mA}$	50			V
		$V_{IS} = 0\text{ V}$; $I_{DM} = 4\text{ A}$; $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.01$	50	60	70	V
Drain source leakage current	I_{DSS}	$V_{DS} = 40\text{ V}$			100	μA
		$V_{DS} = 40\text{ V}$; $T_{mb} = 25^\circ\text{C}$		0.1	10	μA
Drain-source resistance	$R_{DS(ON)}$	$V_{IS} \geq 4.4\text{ V}$; $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.01$; $I_{DM} = 10\text{ A}$			52	m Ω
		$V_{IS} \geq 4.4\text{ V}$; $t_p \leq 300\text{ }\mu\text{s}$; $T_{mb} = 25^\circ\text{C}$		22	28	m Ω
Drain current limiting	I_D	$V_{DS} = 13\text{ V}$	28.5	43	57	A
		$4.4\text{ V} \leq V_{IS} \leq 5.5\text{ V}$; $-40^\circ\text{C} \leq T_{mb} \leq 150^\circ\text{C}$	21		65	A
Overload power threshold	$P_{D(TO)}$	device trips if $P_D > P_{D(TO)}$	75	185	250	W
Characteristic time	T_{DSC}		200	380	600	μs
Threshold junction temperature	$T_{J(TO)}$		150	170		$^\circ\text{C}$
Input threshold voltage	$V_{IS(TO)}$	$V_{DS} = 5\text{ V}$; $I_D = 1\text{ mA}$	0.6		2.4	V
		$V_{DS} = 5\text{ V}$; $I_D = 1\text{ mA}$; $T_{mb} = 25^\circ\text{C}$	1.1	1.6	2.1	V
Input supply current	I_{IS}	normal operation; $V_{IS} = 5\text{ V}$	100	220	400	μA
		normal operation; $V_{IS} = 4\text{ V}$	80	195	330	
Input supply current	I_{ISL}	protection latched; $V_{IS} = 5\text{ V}$	200	400	650	
		protection latched; $V_{IS} = 3\text{ V}$	130	250	430	
Protection reset voltage	V_{ISR}	reset time $t_r \geq 100\text{ }\mu\text{s}$	1.5	2	2.9	V
Latch reset time	t_{lr}	$V_{IS1} = 5\text{ V}$, $V_{IS2} < 1\text{ V}$	10	40	100	μs
Input clamping voltage	$V_{(CL)IS}$	$I_I = 1.5\text{ mA}$	5.5		8.5	V
Input series resistance to gate of power MOSFET	R_{IG}	$I_I = 1.5\text{ mA}$; $T_{mb} = 25^\circ\text{C}$		33		k Ω
Turn-on delay time	$t_{d\text{ on}}$	$V_{IS} = 5\text{ V}$		25	50	μs
Rise time	t_r			50	100	
Turn-off delay time	$t_{d\text{ off}}$	$V_{IS} = 0\text{ V}$		60	120	
Fall time	t_f			50	100	
Junction to mounting base	$R_{th\text{ j-mb}}$			1.25	1.39	K/W
Junction to ambient	$R_{th\text{ j-a}}$	minimum footprint FR4 PCB		50		K/W