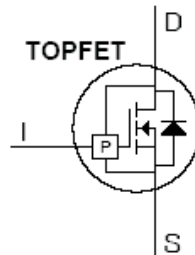
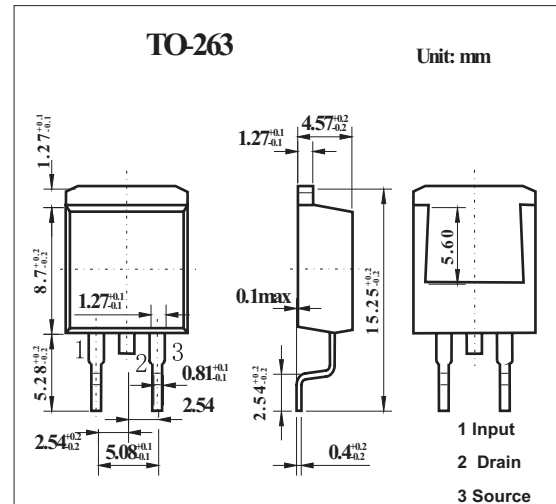


Logic level TOPFET

KUK129-50DL

■ Features

- TrenchMOS output stage
- Current limiting
- Overload protection
- Overtemperature protection
- Protection latched reset by input
- 5 V logic compatible input level
- Control of output stage and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Continuous drain source voltage ¹	V_{DS}	50	V
Continuous drain current $V_{IS} = 5\text{ V}$; $T_{mb} = 25^\circ\text{C}$	I_D	selflimited	A
Continuous drain current $V_{IS} = 5\text{ V}$; $T_{mb} \leq 125^\circ\text{C}$	I_D	16	A
Continuous input current	I_i	-5 to 5	mA
Repetitive peak input current $t_p \leq 1\text{ ms}$	I_{IRM}	-10 to 10	mA
Total power dissipation $T_{mb} \leq 25^\circ\text{C}$	P_D	65	W
Storage temperature	T_{stg}	-55 To 175	$^\circ\text{C}$
Continuous junction temperature ² normal operation	T_j	150	$^\circ\text{C}$
Case temperature during soldering	T_{sold}	260	$^\circ\text{C}$
Electrostatic discharge capacitor voltage *2	V_C	2	kV

*1 $\delta \leq 0.1$, $t_p = 300\ \mu\text{s}$

*2 $C = 250\ \text{pF}$; $R = 1.5\ \text{k}\Omega$

KUK129-50DL

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Non-repetitive clamping energy	E _{DSM}	I _{DM} = 16 A; V _{DD} ≤ 20 V; T _{mb} ≤ 25°C			200	mJ
Repetitive clamping energy	E _{DRM}	I _{DM} = 16 A; V _{DD} ≤ 20 V; T _{mb} ≤ 95°C; f = 250 Hz			32	mJ
Drain source voltage	V _{DS}	4 V ≤ V _{IS} ≤ 5.5 V	0		35	V
Drain-source clamping voltage	V _{(CL)DSS}	V _{IS} = 0 V; I _D = 10 mA	50			V
		V _{IS} = 0 V; I _{DM} = 2 A; t _p ≤ 300 μs; δ ≤ 0.01	50	60	70	V
Drain source leakage current	I _{DSS}	V _{DS} = 40 V			100	μA
		V _{DS} = 40 V; T _{mb} = 25°C		0.1	10	μA
Drain-source resistance	R _{DS(ON)}	V _{IS} ≥ 4.4 V; t _p ≤ 300 μs; δ ≤ 0.01; I _{DM} = 6 A			95	mΩ
		V _{IS} ≥ 4.4V; t _p ≤ 300μs; δ ≤ 0.01; I _{DM} = 6A; T _{mb} = 25°C		36	50	mΩ
		V _{IS} ≥ 4 V; t _p ≤ 300 μs; δ ≤ 0.01; I _{DM} = 6 A			100	mΩ
		V _{IS} ≥ 4V; t _p ≤ 300μs; δ ≤ 0.01; I _{DM} = 6A; T _{mb} = 25°C		39	55	mΩ
Drain current limiting	I _D	V _{DS} = 13 V; V _{IS} = 5 V; T _{mb} = 25°C	16	24	32	A
		V _{DS} = 13 V; 4.4 V ≤ V _{IS} ≤ 5.5 V	12		36	A
		V _{DS} = 13 V; 4 V ≤ V _{IS} ≤ 5.5 V	8		36	A
Overload power threshold	P _{D(TO)}	device trips if P _D > P _{D(TO)} ; V _{IS} = 5 V; T _{mb} = 25°C	40	120	160	W
Characteristic time	T _{DSC}		200	350	600	μs
Threshold junction temperature	T _{j(TO)}		150	170		°C
Input threshold voltage	V _{IS(TO)}	V _{DS} = 5 V; I _D = 1 mA	0.6		2.4	V
		V _{DS} = 5 V; I _D = 1 mA; T _{mb} = 25°C	1.1	1.6	2.1	V
Input supply current	I _{IS}	normal operation; V _{IS} = 5 V	100	220	400	μA
		normal operation; V _{IS} = 4 V	80	195	330	
Input supply current	I _{ISL}	protection latched; V _{IS} = 5 V	200	400	650	μA
		protection latched; V _{IS} = 3 V	130	250	430	
Protection reset voltage	V _{ISR}	reset time t _r ≥ 100 μs	1.5	2	2.9	V
Latch reset time	t _{tr}	V _{IS1} = 5 V, V _{IS2} < 1 V	10	40	100	μs
Input clamping voltage	V _{(CL)IS}	I _I = 1.5 mA	5.5		8.5	V
Input series resistance to gate of power MOSFET	R _{IG}	I _I = 1.5 mA; T _{mb} = 25°C		33		kΩ
Turn-on delay time	t _{d on}	V _{IS} = 5 V		15	30	μs
Rise time	t _r			30	60	
Turn-off delay time	t _{d off}	V _{IS} = 0 V		70	140	
Fall time	t _f			35	70	
Junction to mounting base	R _{th j-mb}			1.75	1.92	K/W
Junction to ambient	R _{th j-a}	minimum footprint FR4 PCB		50		K/W