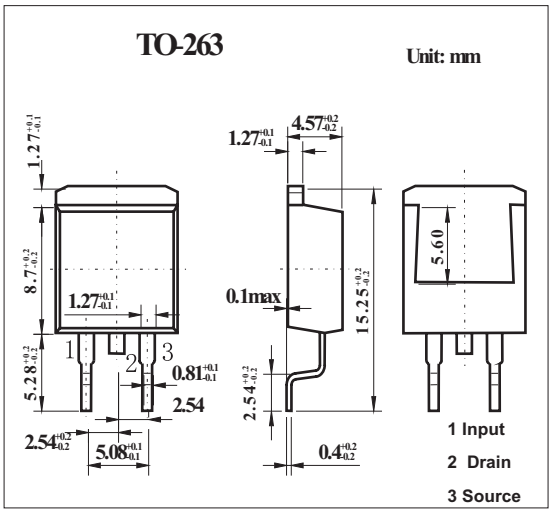
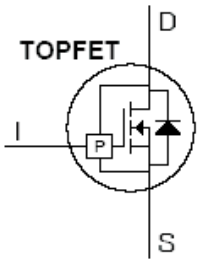
Logic level TOPFET

KUK128-50DL



Features

- TrenchMOS output stage
- Current limiting
- Overload protection
- Overtemperature protection
- Protection latched reset by input
- 5 V logic compatible input level
- Control of output stage and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads



Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Continuous drain source voltage	V_{DS}	50	V
Continuous drain current V_{IS} = 5 V; T_{mb} = 25℃	I_D	selflimited	A
Continuous drain current V_{IS} = 5 V; T_{mb} ⩽ 125℃	I_D	8	A
Continuous input current	I_I	-5 to 5	mA
Repetitive peak input current tp ⩽ 1 ms	I_{IRM}	-10 to 10	mA
Total power dissipation T_{mb} ⩽ 25℃	P_D	40	W
Storage temperature	T_{stg}	-55 To 175	℃
Continuous junction temperature normal operation	T_j	150	℃
Case temperature during soldering	T_{sold}	260	℃
Electrostatic discharge capacitor voltage *	V_C	2	kV

* C = 250 pF; R = 1.5 kΩ

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Non-repetitive clamping energy	E_{DSM}	I_{DM} = 8 A; $V_{DD} \leqslant$ 20 V;$T_{mb} \leqslant$ 25℃			100	mJ
Repetitive clamping energy	E_{DRM}	I_{DM} = 8 A; $V_{DD} \leqslant$ 20 V;$T_{mb} \leqslant$ 95℃; f = 250 Hz			20	mJ
Drain source voltage	V_{DS}	4 V $\leqslant V_{IS} \leqslant$ 5.5 V	0		35	V
Drain-source clamping voltage	$V_{(CL)DSS}$	V_{IS} = 0 V;I_D = 10 mA	50			V
		V_{IS} = 0 V;I_{DM} = 2 A; $t_p \leqslant$ 300 μs; δ ⩽ 0.01	50	60	70	V
Drain source leakage current	I_{DSS}	V_{DS} = 40 V			100	μA
		V_{DS} = 40 V;T_{mb} = 25℃		0.1	10	μA
Drain-source resistance	$R_{DS(ON)}$	$V_{IS} \geqslant$ 4.4 V; $t_p \leqslant$ 300 μs; δ ⩽ 0.01;I_{DM} = 3 A			190	mΩ
		$V_{IS} \geqslant$4.4V; $t_p \leqslant$300μs;δ⩽0.01;I_{DM}=3A;T_{mb} = 25℃		68	100	mΩ
		$V_{IS} \geqslant$ 4 V; $t_p \leqslant$ 300 μs; δ ⩽ 0.01;I_{DM} = 3 A			200	mΩ
		$V_{IS} \geqslant$4V;$t_p \leqslant$300μs;δ⩽0.01;I_{DM}=3A;T_{mb}=25℃		72	105	mΩ
Drain current limiting	I_D	V_{DS} = 13 V;V_{IS} = 5 V; T_{mb} = 25℃	8	12	16	A
		V_{DS} = 13 V;4.4 V $\leqslant V_{IS} \leqslant$ 5.5 V	6		18	A
		V_{DS} = 13 V;4 V $\leqslant V_{IS} \leqslant$ 5.5 V	5		18	A
Overload power threshold	$P_{D(TO)}$	device trips if $P_D > P_{D(TO)}$; V_{IS} = 5 V;T_{mb} = 25℃	20	55	80	W
Characteristic time	T_{DSC}		200	350	600	μs
Threshold junction temperature	$T_{j(TO)}$		150	170		℃
Input threshold voltage	$V_{IS(TO)}$	V_{DS} = 5 V; I_D = 1 mA	0.6		2.4	V
		V_{DS} = 5 V; I_D = 1 mA;T_{mb} = 25℃	1.1	1.6	2.1	V
Input supply current	I_{IS}	normal operation;V_{IS} = 5 V	100	220	400	μA
		normal operation;V_{IS} = 4 V	80	195	330	
Input supply current	I_{ISL}	protection latched;V_{IS} = 5 V	200	400	650	
		protection latched;V_{IS} = 3 V	130	250	430	
Protection reset voltage	V_{ISR}	reset time tr $\geqslant$ 100 μs	1.5	2	2.9	V
Latch reset time	t_{lr}	V_{IS1} = 5 V, V_{IS2} < 1 V	10	40	100	μs
Input clamping voltage	$V_{(CL)IS}$	I_I = 1.5 mA	5.5		8.5	V
Input series resistance to gate of power MOSFET	R_{IG}	I_I = 1.5 mA;T_{mb} = 25℃		33		kΩ
Turn-on delay time	$t_{d\ on}$	V_{IS} = 5 V		8	20	μs
Rise time	t_r			20	50	
Turn-off delay time	$t_{d\ off}$	V_{IS} = 0 V		25	70	
Fall time	t_f			16	40	
Junction to mounting base	$R_{th\ j\text{-}mb}$			2.5	3.1	K/W
Junction to ambient	$R_{th\ j\text{-}a}$	minimum footprint FR4 PCB		50		K/W