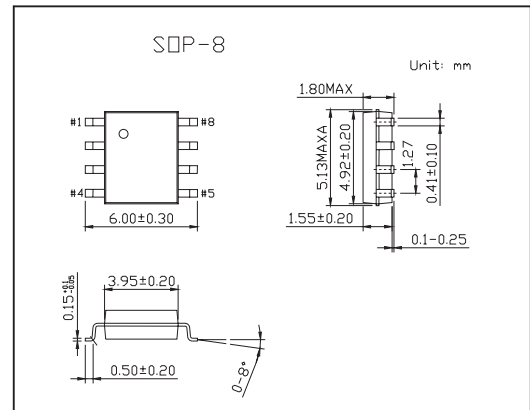
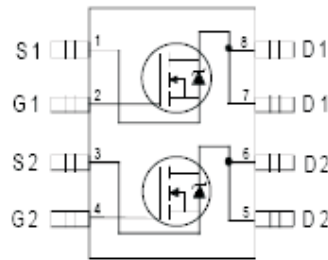


HEXFET[®] Power MOSFET

KRF7105

■ Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Dual N and P Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P-Channel	Unit
Continuous Drain Current $V_{GS} @ 10V$ $T_a = 25^\circ\text{C}$	I_D	3.5	-2.3	A
Continuous Drain Current $V_{GS} @ 10V$ $T_a = 70^\circ\text{C}$	I_D	2.8	-1.8	
Pulsed Drain Current *1	I_{DM}	14	-10	
Power Dissipation @ $T_c = 25^\circ\text{C}$	P_D	2.0		W
Linear Derating Factor		0.016		W/ $^\circ\text{C}$
Peak Diode Recovery dv/dt *2	dv/dt	3.0	-3.0	V/ns
Gate-to-Source Voltage	V_{GS}	± 20		V
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150		$^\circ\text{C}$
Maximum Junction-to-Ambient*3	$R_{\theta JA}$	62.5		$^\circ\text{C/W}$

*1 Repetitive rating; pulse width limited by max. junction temperature.

*2 N-Channel $I_{SD} \leq 3.5A$, $di/dt \leq 90A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

P-Channel $I_{SD} \leq -2.3A$, $di/dt \leq 90A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

*3 Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

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■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250 μ A	N-Ch	25		V
		V _{GS} = 0V, I _D = -250 μ A	P-Ch	-20		
Breakdown Voltage Temp. Coefficient	ΔV _{(BR)DSS} /ΔT _J	I _D = 1mA, Reference to 25°C	N-Ch	0.030		V/°C
		I _D = -1mA, Reference to 25°C	P-Ch	-0.015		
Static Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 1.0A*1	N-Ch	0.083	0.10	Ω
		V _{GS} = 4.5V, I _D = 0.5A*1		0.14	0.16	
		V _{GS} = -10V, I _D = -1.0A*1	P-Ch	0.16	0.25	
		V _{GS} = -4.5V, I _D = -0.50A*1		0.30	0.40	
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μ A	N-Ch	1.0	3.0	V
		V _{DS} = V _{GS} , I _D = -250 μ A	P-Ch	-1.0	-3.0	
Forward Transconductance	g _{fs}	V _{DS} = 15V, I _D = 3.5A*1	N-Ch	4.3		S
		V _{DS} = -15V, I _D = -3.5A*1	P-Ch	3.1		
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} = 20V, V _{GS} = 0V	N-Ch		2.0	μ A
		V _{DS} = -20V, V _{GS} = 0V	P-Ch		-2.0	
		V _{DS} = 20V, V _{GS} = 0V, T _J = 55°C	N-Ch		25	
		V _{DS} = -20V, V _{GS} = 0V, T _J = 55°C	P-Ch		-25	
Gate-to-Source Forward Leakage	I _{GSS}	V _{GS} = ±20V	N-Ch		±100	nA
			P-Ch		±100	
Total Gate Charge	Q _g	N-Channel I _D = 2.3A, V _{DS} = 12.5V, V _{GS} = 10V *1	N-Ch	9.4	27	nC
Gate-to-Source Charge	Q _{gs}	P-Channel	N-Ch	1.7		
			P-Ch	1.9		
Gate-to-Drain ("Miller") Charge	Q _{gd}	I _D = -2.3A, V _{DS} = -12.5V, V _{GS} = -10V *1	N-Ch	3.1		
			P-Ch	2.8		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 25V, I _D = 1.0A, R _G = 6.0 Ω	N-Ch	7.0		ns
Rise Time	t _r	P-Channel R _D = 25 Ω *1	N-Ch	9.0		
			P-Ch	13		
Turn-Off Delay Time	t _{d(off)}	V _{DD} = -25V, I _D = -1.0A, R _G = 6.0 Ω R _D = 25 Ω 1*1	N-Ch	45		
			P-Ch	45		
Fall Time	t _f		N-Ch	25		
			P-Ch	37		
Internal Drain Inductace	L _D	Between lead, 6mm(0.25in.) from packing and center of die contact	N-Ch	4.0		
Internal Source Inductance	L _S		P-Ch	4.0		
			N-Ch	6.0		
P-Ch	6.0					
Input Capacitance	C _{iss}	N-Channel V _{GS} = 0V, V _{DS} = 15V, f = 1.0MHz *1	N-Ch	330		pF
			P-Ch	290		
Output Capacitance	C _{oss}	P-Channel	N-Ch	250		
			P-Ch	210		
Reverse Transfer Capacitance	C _{rss}	V _{GS} = 0V, V _{DS} = -15V, f = 1.0MHz *1	N-Ch	61		
			P-Ch	67		

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■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit	
Continuous Source Current (Body Diode)	Is		N-Ch		2.0	A	
			P-Ch		-2.0		
Pulsed Source Current (Body Diode) *2	ISM		N-Ch		14		
			P-Ch		-9.2		
Diode Forward Voltage	VSD	TJ = 25°C, Is = 1.3A, VGS = 0V*1	N-Ch		1.2	V	
		TJ = 25°C, Is = -1.3A, VGS = 0V*1	P-Ch		-1.2		
Reverse Recovery Time	trr	N-Channel TJ = 25°C, IF = 1.3A, di/dt = 100A/μs*1	N-Ch	36	54	ns	
			P-Ch	69	100		
Reverse RecoveryCharge	Qrr		P-Channel TJ = 25°C, IF = -1.3A, di/dt = -100A/μs*1	N-Ch	41	75	nC
				P-Ch	90	180	
Forward Turn-On Time	ton	Intrinsic turn-on time is negligible (turn-on is dominated by Ls+Ld)		N-Ch			
				P-Ch			

*1 Pulse width $\leq 300 \mu s$; duty cycle $\leq 2\%$.

*2 Repetitive rating; pulse width limited by max. junction temperature.