Dual N & P-Channel, Logic Level MOSFET

KQS4900

■ Features

- N-Channel

  1.3 A, 60 V $R_{DS(ON)}$ = 0.55Ω @ V_{GS} = 10 V

  $R_{DS(ON)}$ = 0.65Ω @ V_{GS} =5V

- P-Channel

  -0.3 A, -300V $R_{DS(ON)}$ = 15.5Ω @ V_{GS} =- 10V

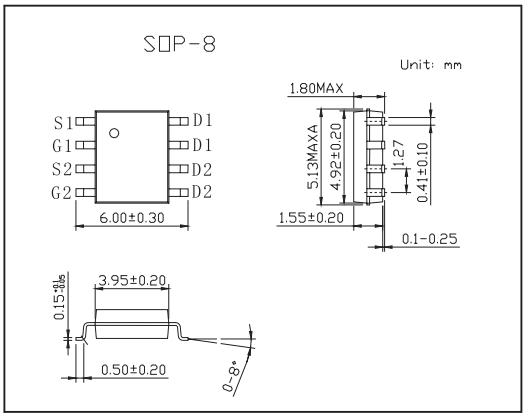
  $R_{DS(ON)}$ = 16Ω @ V_{GS} =-5V

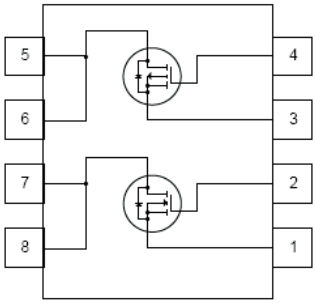
- Low gate charge (typical N-Channel 1.6 nC)

  (typical P-Channel 3.6 nC)

- Fast switching

- Improved dv/dt capability





■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage	V_{DSS}	60	-300	V
Gate to Source Voltage	V_{GS}	±20		V
Drain Current Continuous Ta = 25℃	I_D	1.3	-0.3	A
Ta = 70℃		0.82	-0.19	
Drain Current Pulsed *1	I_{DM}	5.2	-1.2	A
Peak Diode Recovery dv/dt	dv/dt	7	4.5	V/ns
Power Dissipation for Single Operation Ta = 25℃	P_D	2		W
Ta = 70℃		1.3		
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150		℃
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	62.5		℃/W

*1Repetitive Rating : Pulse width limited by maximum junction temperature

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	N-Ch	60			V
		V_{GS} = 0 V, I_D = -250 μA	P-Ch	-300			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0 V	N-Ch			1	μA
		V_{DS} = 48 V, T_C = 55℃				10	
		V_{DS} = -300 V, V_{GS} = 0 V	P-Ch			-1	μA
		V_{DS} = -240 V, T_C = 55℃				-10	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0 V	N-Ch			±100	nA
		V_{GS} = ±20 V, V_{DS} = 0 V	P-Ch			±100	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 4V, I_D = 20mA	N-Ch	1.0		1.95	V
		V_{DS} = 4V, I_D = -20mA	P-Ch	-1.0		-1.95	
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D =0.65A	N-Ch		0.39	0.55	Ω
		V_{GS} = 5 V, I_D = 0.65A			0.46	0.65	
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10 V, I_D =-0.15 A	P-Ch		11.2	15.5	
		V_{GS} = -5 V, I_D =-0.15 A			11.4	16	
Forward Transconductance	g_{FS}	V_{DS} = 10V, I_D = 0.65A	N-Ch		1.7		S
		V_{DS} = -10V, I_D = -0.15A	P-Ch		0.6		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 30 V, I_D = 1.3 A,R_G=25Ω *	N-Ch		5.7	21	ns
			P-Ch		10	30	
Turn-On Rise Time	t_r		N-Ch		21	50	ns
			P-Ch		25	60	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel V_{DD} = -150 V, I_D = -0.3 A,R_G=25Ω *	N-Ch		11	32	ns
			P-Ch		35	80	
Turn-Off Fall Time	t_f		N-Ch		17	45	ns
			P-Ch		47	105	
Total Gate Charge	Q_g	N-Channel V_{DS} =48V,I_D=1.3A,V_{GS}=5V *	N-Ch		1.6	2.1	nC
			P-Ch		3.6	4.7	
Gate-Source Charge	Q_{gs}		N-Ch		0.28		nC
		P-Channel V_{DS}=-240V,I_D=-30.3A,V_{GS}=-5V *	P-Ch		0.42		
Gate-Drain Charge	Q_{gd}		N-Ch		0.82		nC
			P-Ch		2.1		
Maximum Continuous Drain-Source Diode Forward Current	I_S		N-Ch			1.3	A
			P-Ch			-0.3	
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1.3A	N-Ch			1.5	V
		V_{GS} = 0 V, I_S = -0.3A	P-Ch			-4.0	

* Pulse Test : Pulse width ≤ 300 μs, Duty cycle ≤ 2%