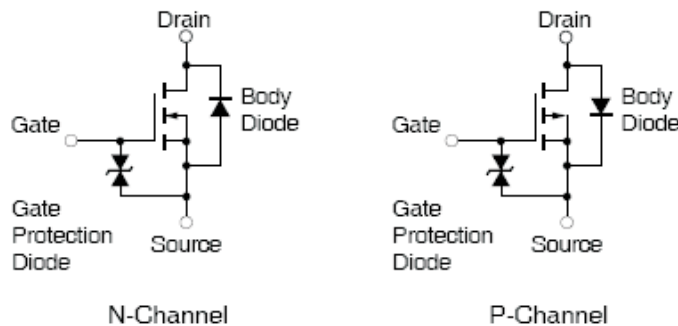
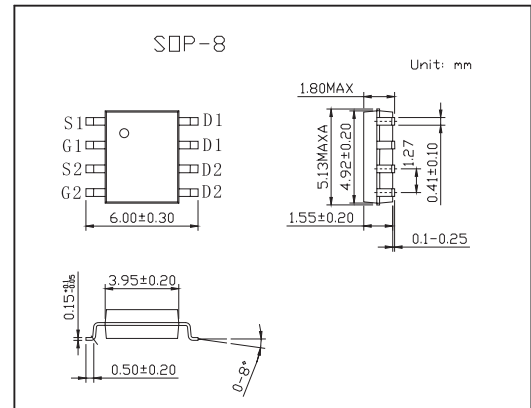


MOS Field Effect Transistor

KPA1790

■ Features

- Dual chip type
- Low on-state resistance
 - N-channel $R_{DS(on)1} = 0.12 \Omega$ TYP. ($V_{GS} = 10 \text{ V}$, $I_D = 0.5 \text{ A}$)
 - $R_{DS(on)2} = 1.19 \Omega$ TYP. ($V_{GS} = 4 \text{ V}$, $I_D = 0.5 \text{ A}$)
- P-channel $R_{DS(on)1} = 0.45 \Omega$ TYP. ($V_{GS} = -10 \text{ V}$, $I_D = -0.35 \text{ A}$)
- $R_{DS(on)2} = 0.74 \Omega$ TYP. ($V_{GS} = -4 \text{ V}$, $I_D = -0.35 \text{ A}$)
- Low input capacitance
 - N-channel $C_{iss} = 180 \text{ pF}$ TYP.
 - P-channel $C_{iss} = 230 \text{ pF}$ TYP.
- Built-in G-S protection diode
- Small and surface mount package



N-Channel

P-Channel

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	60	-60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 1.0	± 0.7	A
Drain Current (pulse) *1	$I_{D(pulse)}$	± 4.0	± 2.8	A
Total Power Dissipation (1 unit) *2	P_T	1.7		W
Total Power Dissipation (2 units) *2	P_T	2		W
Channel Temperature	T_{ch}	150		$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150		$^\circ\text{C}$
Single Avalanche Current *3	I_{AS}	0.5	-0.35	A
Single Avalanche Energy *3	E_{AS}	0.02	0.01	mJ

*1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

*2. Mounted on ceramic substrate of $2000 \text{ mm}^2 \times 2.25 \text{ mm}$

*3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 30 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

KPA1790

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Zero Gate Voltage Drain Current	IDSS	VDS = 60 V, VGS = 0 V			10	μA
		VDS = -60V, VGS = 0 V			-10	
Gate Leakage Current	IGSS	VGS = ±16 V, VDS = 0 V			±10	μA
		VGS = ±16 V, VDS = 0 V			±10	
Gate Cut-off Voltage	VGS(off)	VDS = 10 V, ID = 1 mA	1.0	1.7	2.5	V
		VDS = -10 V, ID = -1 mA	-1.0	-1.7	-2.5	
Forward Transfer Admittance	yfs	VDS = 10 V, ID = 0.5 A	1.0	1.7		S
		VDS = -10 V, ID = -0.35A	5.0			
Drain to Source On-state Resistance	RDS(on)1	VGS = 10 V, ID = 0.5 A		0.12	0.26	Ω
	RDS(on)2	VGS = 4 V, ID = 0.5 A		0.19	0.34	
	RDS(on)1	VGS = -10 V, ID = -0.35 A		0.45	0.6	Ω
	RDS(on)2	VGS = -4 V, ID = -0.35 A		0.74	1.1	
Input Capacitance	Ciss	N-Channel VDS = 10 V, VGS = 0 V, f = 1 MHz	N-Ch	180		pF
			P-Ch	230		
Output Capacitance	Coss	P- Channel	N-Ch	100		pF
			P-Ch	100		
Reverse Transfer Capacitance	Crss	VDS = -10 V, VGS = 0 V, f = 1 MHz	N-Ch	35		pF
			P-Ch	25		
Turn-on Delay Time	td(on)	N-Channel VDD = 30 V, ID = 0.5 A, VGS = 10 V	N-Ch	1		ns
			P-Ch	1.9		
Rise Time	tr	RG = 10 Ω	N-Ch	1.4		ns
			P-Ch	1.7		
Turn-off Delay Time	td(off)	P- Channel VDD = -30 V, ID = -0.35 A, VGS = -10 V	N-Ch	23		ns
			P-Ch	30		
Fall Time	tf	RG = 10 Ω	N-Ch	17		ns
			P-Ch	15		
Total Gate Charge	QG	N-Channel ID = 1.0 A, VDD = 48 V, VGS = 10 V	N-Ch	8		nC
			P-Ch	7.6		
Gate to Source Charge	QGS	P- Channel ID = -0.7 A, VDD = -48 V, VGS = -10 V	N-Ch	1		nC
			P-Ch	1		
Gate to Drain Charge	QGD		N-Ch	3.5		nC
			P-Ch	2		
Body Diode Forward Voltage Note	VF(S-D)	IF = 1.0 A, VGS = 0 V	N-Ch	0.75		V
			P-Ch	0.85		
Reverse Recovery Time	trr	N-Channel IF = 1.0A, VGS = 0 V, di/dt = 100 A/μs	N-Ch	30		ns
			P-Ch	58		
Reverse Recovery Charge	Qrr	P-Channel IF = 0.7A, VGS = 0 V, di/dt = 100 A/μs	N-Ch	33		nC
			P-Ch	130		