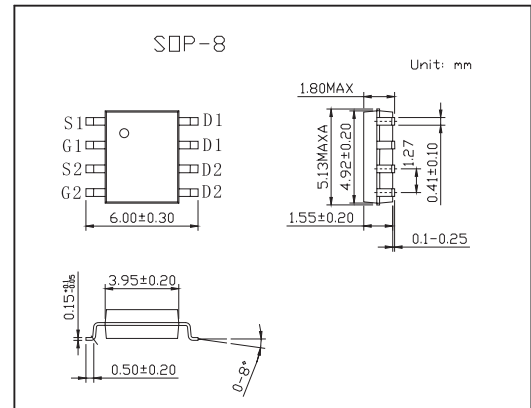
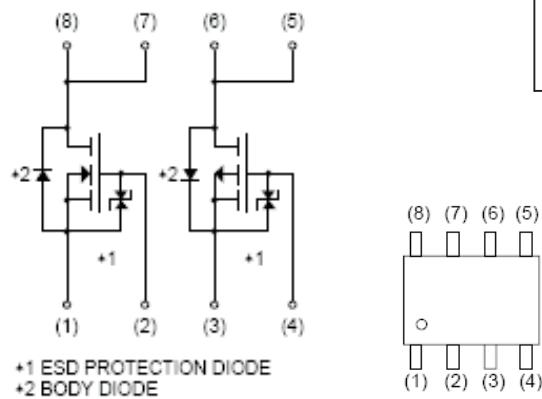


Switching KP8M7

■ Features

- Low on-resistance.
- Built-in G-S Protection Diode.
- Small and Surface Mount Package.
- Power switching, DC / DC converter.



■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-source voltage	V_{DSS}	30	-30	V
Gate-source voltage	V_{GSS}	± 20	± 20	V
Drain current Continuous	I_D	± 5.0	± 7.0	A
Drain current Pulsed *	I_{DP}	± 20	± 28	A
Source current (Body diode) Continuous	I_S	1.6	-1.6	A
Source current (Body diode) Pulsed *	I_{SP}	6.4	-28	A
Total power dissipation	P_D	2		W
Channel temperature	T_{ch}	150		$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150		$^\circ\text{C}$
Channel to ambient	$R_{th(ch-a)}$	62.5		$^\circ\text{C/W}$

* $P_w \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

KP8M7

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit	
Gate-source leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	N-Ch		±10	μ A	
		V _{GS} =±20V, V _{DS} =0V	P-Ch		±10		
Drain-source breakdown voltage	V _{(BR) DSS}	I _D =1mA, V _{GS} =0V	N-Ch	30		V	
		I _D =-1mA, V _{GS} =0V	P-Ch	-30			
Zero gate voltage drain current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	N-Ch		1	μ A	
		V _{DS} =-30V, V _{GS} =0V	P-Ch		-1		
Gate threshold voltage	V _{GS (th)}	V _{DS} =10V, I _D =1mA	N-Ch	1.0	2.5	V	
		V _{DS} =-10V, I _D =-1mA	P-Ch	-1.0	-2.5		
Static drain-source on-state resistance	R _{DS (on)}	I _D =5.0A, V _{GS} =10A	N-Ch		36	51	m Ω
		I _D =5.0A, V _{GS} =4.5V			52	73	
		I _D =5.0A, V _{GS} =4V			58	82	
Static drain-source on-state resistance	R _{DS (on)}	I _D =-7A, V _{GS} =-10A	P-Ch		20	28	m Ω
		I _D =-7A, V _{GS} =-4.5V			25	35	
		I _D =-7A, V _{GS} =-4.0V			30	42	
Forward transfer admittance	Y _{fs}	I _D =5.0A, V _{DS} =10V	N-Ch	3.0		S	
		I _D =-7A, V _{DS} =-10V	P-Ch	6.0			
Input capacitance	C _{iss}	N-Channel V _{DS} =10V, V _{GS} =0V, f=1MHz	N-Ch		230	pF	
			P-Ch		2600		
Output capacitance	C _{oss}	P-Channel	N-Ch		80	pF	
			P-Ch		450		
Reverse transfer capacitance	C _{rss}	V _{DS} =-10V, V _{GS} =0V, f=1MHz	N-Ch		50	pF	
			P-Ch		350		
Turn-on delay time	t _{d (on)}	I _D =2.5A, V _{DD} =15V	N-Ch		6	ns	
		I _D =-3.5A, V _{DD} =-15V	P-Ch		20		
Rise time	t _r	N-Channel V _{GS} =10V, R _L =6.0 Ω, R _G =10 Ω	N-Ch		8	ns	
			P-Ch		50		
Turn-off delay time	t _{d (off)}	P-Channel	N-Ch		22	ns	
			P-Ch		110		
Fall time	t _f	V _{GS} =-10V, R _L =4.3 Ω, R _G =10 Ω	N-Ch		5	ns	
			P-Ch		70		
Total gate charge	Q _g	N-Channel V _{DD} =15V, V _{GS} =5V, I _D =5.0A	N-Ch		3.9	5.5	nC
			P-Ch		25		
Gate-source charge	Q _{gs}	P-Channel	N-Ch		1.1		nC
			P-Ch		5.5		
Gate-drain charge	Q _{gd}	V _{DD} =-15V, V _{GS} =-5V, I _D =-7.0A	N-Ch		1.4		nC
			P-Ch		10		
Forward voltage	V _{SD}	I _S =6.4A, V _{GS} =0V	N-Ch			1.2	V
		I _S =-1.6A, V _{GS} =0V	P-Ch			-1.2	