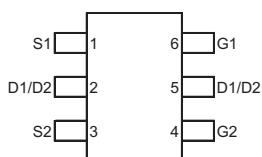
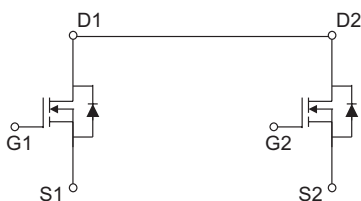
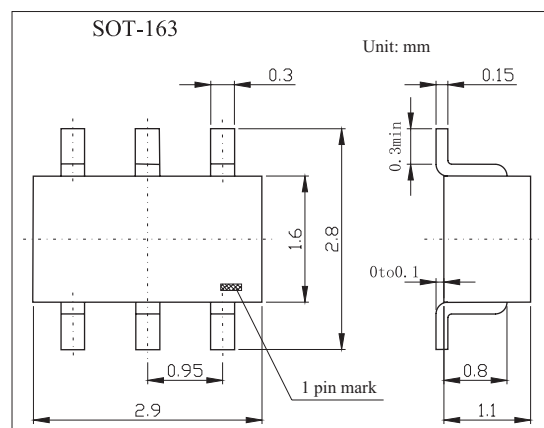


## Dual N-Channel High Density Trench MOSFET

## KI8205T

## ■ Features

- Super high dense cell trench design for low  $R_{DS(on)}$ .
- Rugged and reliable.
- Surface Mount package.

■ Absolute Maximum Ratings  $T_a = 25^\circ\text{C}$ 

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current-Continuous @ $T_A = 25^\circ\text{C}$ *1	$I_D$	4.3	A
-Pulse *2	$I_{DM}$	21.5	A
Drain-Source Diode Forward Current *1	$I_S$	1.7	A
Maximum Power Dissipation $T_A=25^\circ\text{C}$ *1	$P_D$	1.25	W
$T_A=75^\circ\text{C}$		0.75	
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to 150	$^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{thJA}$	100	$^\circ\text{C/W}$

\*1 Surface Mounted on FR4 Board ,  $t \leq 10\text{sec}$  .

\*2 Pulse width limited by maximum junction temperature.

## Dual N-Channel High Density Trench MOSFET

## KI8205T

## ■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V <sub>DSS</sub>	V <sub>GS</sub> = 0V , I <sub>D</sub> = 250 μ A	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 20V , V <sub>DS</sub> = 0V			1	μ A
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = ±12V , V <sub>GS</sub> = 0V			±100	nA
Gate Threshold Voltage *1	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	0.6	0.9	1.5	V
Drain-Source On-State Resistance *1	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4V , I <sub>D</sub> = 4.3A		25	30	mΩ
		V <sub>GS</sub> = 2.5V , I <sub>D</sub> = 3.4A		34	46	
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 8V , V <sub>GS</sub> = 0V, f = 1.0MHz		550		pF
Output Capacitance	C <sub>OSS</sub>			164		
Reverse Transfer Capacitance	C <sub>RSS</sub>			138		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10V , I <sub>D</sub> = 1A		10		ns
Turn-Off Delay Time	t <sub>r</sub>	V <sub>GEN</sub> = 4.5V		8.2		ns
Rise Time	t <sub>d(off)</sub>	R <sub>L</sub> = 10 Ω		25		ns
Fall Time	t <sub>f</sub>	R <sub>GEN</sub> = 6 Ω		6.7		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10V , I <sub>D</sub> = 3A, V <sub>GS</sub> = 4.5V		6.2		nC
Gate-Source Charge	Q <sub>gs</sub>			1.8		nC
Gate-Drain Charge	Q <sub>gd</sub>			1.5		nC
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V , I <sub>S</sub> = 1.7A *1			1.2	V

\*1 Pulse width ≤ 300 μ s , Duty Cycle ≤ 2% .