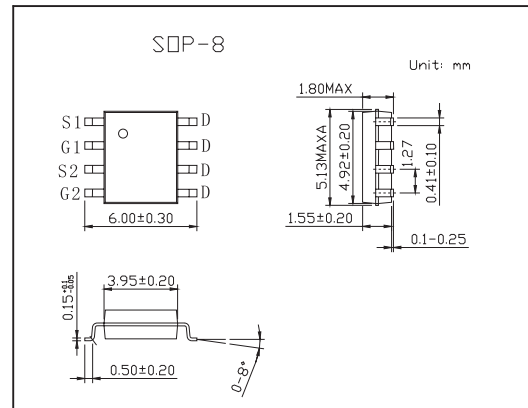
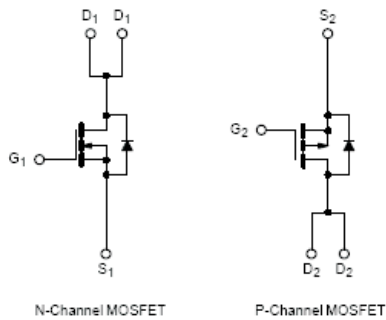


## N- and P-Channel 2.5-V (G-S) MOSFET

## KI4562DY

## ■ PIN Configuration

■ Absolute Maximum Ratings  $T_A = 25^\circ\text{C}$ 

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	$V_{DS}$	20	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	$\pm 12$	V
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )* $T_A = 25^\circ\text{C}$	$I_D$	$\pm 7.1$	$\pm 6.2$	A
		$\pm 5.7$	$\pm 4.9$	A
$T_A = 70^\circ\text{C}$				
Pulsed Drain Current	$I_{DM}$	$\pm 40$	$\pm 40$	A
Continuous Source Current (Diode Conduction)*	$I_S$	1.7	-1.7	A
Maximum Power Dissipation* $T_A = 25^\circ\text{C}$	$P_D$	2		W
		1.3		W
$T_A = 70^\circ\text{C}$				
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$
Maximum Junction-to-Ambient *	$R_{thJA}$	62.5		$^\circ\text{C/W}$

\*Surface Mounted on FR4 Board,  $t \leq 10$  sec.

## KI4562DY

■ Electrical Characteristics T<sub>J</sub> = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit	
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	0.6			V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-0.6			
Gate Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V	N-Ch			±100	nA
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V	P-Ch			±100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0 V	N-Ch			1	μA
		V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0 V	P-Ch			-1	
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C	N-Ch			5	
		V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C	P-Ch			-5	
On State Drain Currenta	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 4.5 V	N-Ch	20			A
		V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -4.5 V	P-Ch	-20			
Drain Source On State Resistance*	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 7.1A	N-Ch		0.019	0.025	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -6.2A	P-Ch		0.027	0.033	
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 6.0A	N-Ch		0.025	0.035	
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -5.0A	P-Ch		0.040	0.050	
Forward Transconductance*	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 7.1A	N-Ch		27		S
		V <sub>DS</sub> = -10 V, I <sub>D</sub> = -6.2A	P-Ch		20		
Diode Forward Voltage*	V <sub>SD</sub>	I <sub>S</sub> = 1.7A, V <sub>GS</sub> = 0 V	N-Ch			1.2	V
		I <sub>S</sub> = -1.7A, V <sub>GS</sub> = 0 V	P-Ch			-1.2	
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 7.1A	N-Ch		25	50	nC
Gate Source Charge	Q <sub>gs</sub>	P-Channel V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.52 V, I <sub>D</sub> = -6.2A	P-Ch		22	35	
			N-Ch		6.5		
Gate Drain Charge	Q <sub>gd</sub>		P-Ch		7		
Turn On Time	t <sub>d(on)</sub>	N Channel V <sub>DD</sub> = 10 V, R <sub>L</sub> = 10 Ω	N-Ch		40	60	ns
			P-Ch		27	50	
Rise Time	t <sub>r</sub>	I <sub>D</sub> = 1A, V <sub>GEN</sub> = 4.5V, R <sub>g</sub> = 6 Ω	N-Ch		40	60	
			P-Ch		32	50	
Turn Off Delay Time	t <sub>d(off)</sub>	P-Channel V <sub>DD</sub> = -10 V, R <sub>L</sub> = 10 Ω	N-Ch		90	150	
			P-Ch		95	150	
Fall Time	t <sub>f</sub>	I <sub>D</sub> = -1 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 6 Ω	N-Ch		40	60	
			P-Ch		45	70	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 1.7 A, di/dt = 100 A/μs	N-Ch		40	80	
		I <sub>F</sub> = -1.7 A, di/dt = 100 A/μs	P-Ch		40	80	

\* Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.