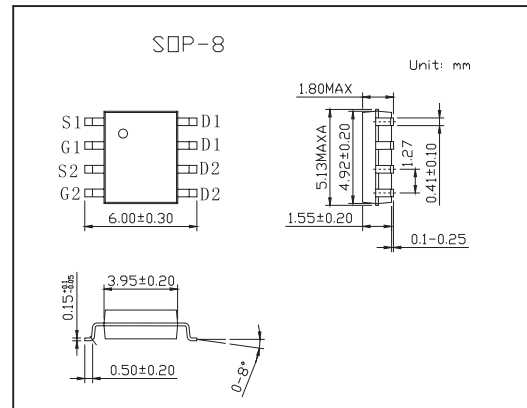
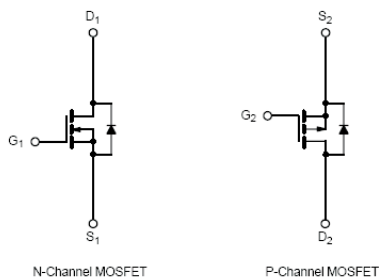


N- and P-Channel 30-V (D-S) MOSFET

KI4532DY

■ PIN Configuration

■ Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V_{DS}	30	-30	V	
Gate-Source Voltage	V_{GS}	± 20	± 20	V	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)* $T_A = 25^\circ\text{C}$	I_D	± 3.9	± 3.5	A	
		$T_A = 70^\circ\text{C}$	± 3.1	± 2.8	A
Pulsed Drain Current	I_{DM}	± 20	± 20	A	
Continuous Source Current (Diode Conduction)*	I_S	1.7	-1.7	A	
Maximum Power Dissipation*	P_D	$T_A = 25^\circ\text{C}$	2	2	W
		$T_A = 70^\circ\text{C}$	1.3	1.3	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	
Maximum Junction-to-Ambient*	R_{thJA}	62.5		$^\circ\text{C}/\text{W}$	

*Surface Mounted on FR4 Board, $t \leq 10$ sec.

KI4532DY

■ Electrical Characteristics $T_J = 25^\circ\text{C}$

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch	1		V	
		$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	P-Ch	-1			
Gate Body Leakage	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	N-Ch		± 100	nA	
		$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	P-Ch		± 100		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	N-Ch		1		
		$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}$	P-Ch		-1		
		$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$	N-Ch			25	μA
		$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$	P-Ch			-25	
On State Drain Currenta	$I_{D(on)}$	$V_{DS} \geq 5\text{V}, V_{GS} = 10\text{V}$	N-Ch	15		A	
		$V_{DS} \leq -5\text{V}, V_{GS} = -10\text{V}$	P-Ch	-15			
Drain Source On State Resistance*	$r_{DS(on)}$	$V_{GS} = 10\text{V}, I_D = 3.9\text{A}$	N-Ch		0.043	0.065	Ω
		$V_{GS} = -10\text{V}, I_D = -2.5\text{A}$	P-Ch		0.066	0.085	
		$V_{GS} = 4.5\text{V}, I_D = 3.1\text{A}$	N-Ch		0.075	0.095	
		$V_{GS} = -4.5\text{V}, I_D = -1.8\text{A}$	P-Ch		0.125	0.19	
Forward Transconductance*	g_{fs}	$V_{DS} = 15\text{V}, I_D = 3.9\text{A}$	N-Ch		7	S	
		$V_{DS} = -15\text{V}, I_D = -2.5\text{A}$	P-Ch		5		
Diode Forward Voltage*	V_{SD}	$I_S = 1.7\text{A}, V_{GS} = 0\text{V}$	N-Ch		0.8	1.2	V
		$I_S = -1.7\text{A}, V_{GS} = 0\text{V}$	P-Ch		-0.8	-1.2	
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10\text{V}, V_{GS} = 10\text{V}, I_D = 3.9\text{A}$	N-Ch		9.8	15	nC
Gate Source Charge	Q_{gs}	P-Channel $V_{DS} = -10\text{V}, V_{GS} = -10\text{V}, I_D = -2.5\text{A}$	N-Ch		2.1		
Gate Drain Charge	Q_{gd}		P-Ch		1.9		
Turn On Time	$t_{d(on)}$	N Channel $V_{DD} = 10\text{V}, R_L = 10\Omega$	N-Ch		9	15	
Rise Time	t_r	$I_D = 1\text{A}, V_{GEN} = 10\text{V}, R_g = 6\Omega$	P-Ch		7	15	
			N-Ch		6	18	
Turn Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -10\text{V}, R_L = 10\Omega$	N-Ch		18	27	ns
			P-Ch		14	27	
Fall Time	t_f	$I_D = -1\text{A}, V_{GEN} = -10\text{V}, R_g = 6\Omega$	N-Ch		6	15	
			P-Ch		8	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\text{A}, di/dt = 100\text{A}/\mu\text{s}$	N-Ch		52	80	
		$I_F = -1.7\text{A}, di/dt = 100\text{A}/\mu\text{s}$	P-Ch		50	80	

* Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.