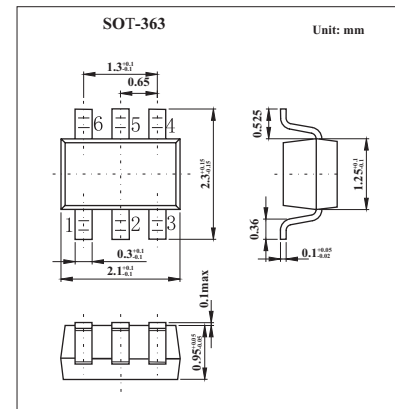
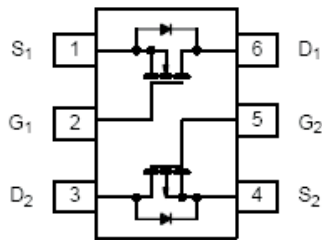


Complementary Low-Threshold MOSFET Pair

KI1555DL

■ PIN Configuration

■ Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Parameter	Symbol	N-Channel		P-Channel		Unit
		5 secs	Steady State	5 secs	Steady State	
Drain-Source Voltage	V_{DS}	20		-8		V
Gate-Source Voltage	V_{GS}	± 12		± 8		V
Continuous Drain Current ($T_J = 150^\circ\text{C}$)* $T_A = 25^\circ\text{C}$	I_D	± 0.70	± 0.66	± 0.60	± 0.57	A
		$T_A = 85^\circ\text{C}$	± 0.50	± 0.48	± 0.43	± 0.41
Pulsed Drain Current	I_{DM}	± 1				A
Continuous Source Current (Diode Conduction) ^a	I_S	0.25	0.23	-0.25	-0.23	A
Maximum Power Dissipation* $T_A = 25^\circ\text{C}$	P_D	0.3	0.27	0.3	0.27	W
		$T_A = 85^\circ\text{C}$	0.16	0.14	0.16	0.14
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ\text{C}$

*Surface Mounted on 1" X 1" FR4 Board.

■ Thermal Resistance Ratings $T_A = 25^\circ\text{C}$

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient*	$t \leq 5 \text{ sec}$	R_{thJA}	360	415	$^\circ\text{C/W}$
	Steady State		400	460	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	300	350	

*Surface Mounted on 1" X 1" FR4 Board.

KI1555DL

■ Electrical Characteristics T_J = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit	
Gate Threshold Voltage	V _{GS(th)}	V _{Ds} = V _{Gs} , I _D = 250 μA	N-Ch	0.6			V
		V _{Ds} = V _{Gs} , I _D = -250 μA	P-Ch	-0.45			
Gate Body Leakage	I _{GSS}	V _{Ds} = 0 V, V _{Gs} = ±12V	N-Ch			±100	nA
		V _{Ds} = 0 V, V _{Gs} = ±8V	P-Ch			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{Ds} = 16V, V _{Gs} = 0 V	N-Ch			1	nA
		V _{Ds} = -6.4V, V _{Gs} = 0 V	P-Ch			-1	
		V _{Ds} = 16 V, V _{Gs} = 0 V, T _J = 85°C	N-Ch			5	μA
		V _{Ds} = -6.4V, V _{Gs} = 0 V, T _J = 85°C	P-Ch			-5	
On State Drain Currenta	I _{D(on)}	V _{Ds} ≥ 5 V, V _{Gs} = 4.5 V	N-Ch	1.0			A
		V _{Ds} ≤ -5 V, V _{Gs} = -4.5 V	P-Ch	-1.0			
Drain Source On State Resistance*	r _{DS(on)}	V _{Gs} = 4.5 V, I _D = 0.66A	N-Ch		0.320	0.385	Ω
		V _{Gs} = -4.5 V, I _D = -0.57A	P-Ch		0.510	0.600	
		V _{Gs} = 2.5 V, I _D = 0.40A	N-Ch		0.560	0.630	
		V _{Gs} = -2.5 V, I _D = -0.48A	P-Ch		0.720	0.850	
		V _{Gs} = -1.8 V, I _D = -0.20A	P-Ch		1.00	1.200	
Forward Transconductance*	g _{fs}	V _{Ds} = 10 V, I _D = 0.66A	N-Ch		1.5		mS
		V _{Ds} = -4 V, I _D = -0.57A	P-Ch		1.2		
Diode Forward Voltage*	V _{SD}	I _s = 0.23A, V _{Gs} = 0 V	N-Ch		0.8	1.2	V
		I _s = -0.23A, V _{Gs} = 0 V	P-Ch		-0.8	-1.2	
Total Gate Charge	Q _g	N-Channel V _{Ds} = 10 V, V _{Gs} = 4.5V, I _D = 0.66A	N-Ch		0.8	1.2	pC
Gate Source Charge	Q _{gs}	P-Channel	N-Ch		0.06		
			P-Ch		0.17		
Gate Drain Charge	Q _{gd}	V _{Ds} = -4 V, V _{Gs} = -4.5 V, I _D = -0.57A	N-Ch		0.30		
			P-Ch		0.16		
Turn On Time	t _{d(on)}	N- Channel V _{DD} = 10 V, R _L = 20 Ω	N-Ch		10	20	ns
Rise Time	t _r	I _D = 0.5 A, V _{GEN} = 4.5V, R _g = 6 Ω	P-Ch		6	12	
			N-Ch		16	30	
Turn Off Delay Time	t _{d(off)}	P-Channel V _{DD} = -4 V, R _L = 8 Ω	N-Ch		10	20	
			P-Ch		10	20	
Fall Time	t _f	I _D = -0.5 A, V _{GEN} = -4.5 V, R _g = 6 Ω	N-Ch		10	20	
			P-Ch		10	20	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 0.23 A, di/dt = 100 A/μs	N-Ch		20	40	
		I _F = -0.23 A, di/dt = 100 A/μs	P-Ch		20	40	

* Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.