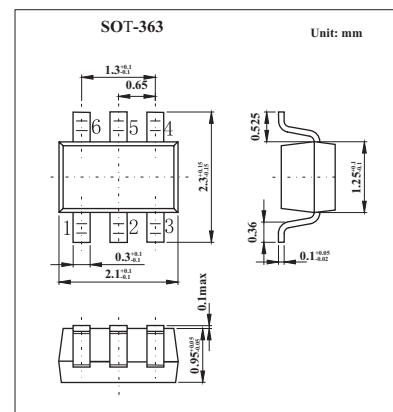
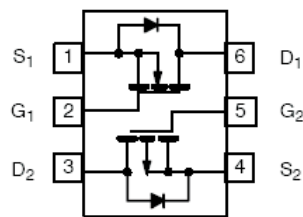


Complementary 20-V (D-S) Low-Threshold MOSFET

KI1501DL

■ PIN Configuration



■ Absolute Maximum Ratings TA = 25°C

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	20	-20	V
Gate-Source Voltage	V _{GS}	±8	±8	V
Continuous Drain Current (T _J = 150°C)* TA = 25°C	I _D	250	-180	mA
		TA = 70°C	200	-140
Pulsed Drain Current	I _{DM}	500	-500	mA
Maximum Power Dissipation*	P _D	0.2		W
		0.13		W
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C
Maximum Junction-to-Ambient*	R _{thJA}	625		°C/W

*Surface Mounted on FR4 Board, t ≤ 10 sec.

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■ Electrical Characteristics T_J = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit	
Drain Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 10 μA	N-Ch	20	24		V
		V _{GS} = 0 V, I _D = -10 μA	P-Ch	-20	-24		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 50 μA	N-Ch	0.4	0.9	1.5	
		V _{DS} = V _{GS} , I _D = -50 μA	P-Ch	-0.4	-0.9	-1.5	
Gate Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8V	N-Ch		±2	±100	nA
			P-Ch		±2	±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch		0.001	100	nA
		V _{DS} = -20 V, V _{GS} = 0 V	P-Ch		-0.001	-100	
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55°C	N-Ch			1	μA
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55°C	P-Ch			-1	
On State Drain Currenta	I _{D(on)}	V _{DS} ≥ 2.5 V, V _{GS} = 5.0 V	N-Ch	120			mA
		V _{DS} ≤ -2.5 V, V _{GS} = -5.0 V	P-Ch	-120			
		V _{DS} ≥ 4.5 V, V _{GS} = 8.0 V	N-Ch	400			
		V _{DS} ≤ -4.5 V, V _{GS} = -8.0 V	P-Ch	-400			
Drain Source On State Resistance*1	r _{DS(on)}	V _{GS} = 2.5 V, I _D = 150 mA	N-Ch		1.6	2.5	Ω
		V _{GS} = -2.5 V, I _D = -75 mA	P-Ch		4	5	
		V _{GS} = 4.5 V, I _D = 250 mA	N-Ch		1.2	2.0	
		V _{GS} = -4.5 V, I _D = -180 mA	P-Ch		2.6	3.8	
Forward Transconductance*1	g _{fs}	V _{DS} = 2.5 V, I _D = 50 mA	N-Ch		150		mS
		V _{DS} = -2.5 V, I _D = -50 mA	P-Ch		200		
Diode Forward Voltage*1	V _{SD}	I _S = 50 mA, V _{GS} = 0 V	N-Ch		0.7	1.2	V
		I _S = -50 mA, V _{GS} = 0 V	P-Ch		-0.7	-1.2	
Total Gate Charge	Q _g	N-Channel V _{DS} = 5 V, V _{GS} = 4.5 V, I _D = 100 mA	N-Ch		300	450	pC
Gate Source Charge	Q _{gs}	P-Channel V _{DS} = -5 V, V _{GS} = -4.5 V, I _D = -mA *2	N-Ch		25		
			P-Ch		25		
Gate Drain Charge	Q _{gd}		N-Ch		100		
			P-Ch		100		
Input Capacitance	C _{iss}	N-Channel V _{DS} = 5 V, V _{GS} = 0 V	N-Ch		15		pF
Output Capacitance	C _{oss}	P-Channel V _{DS} = -5 V, V _{GS} = 0 V *2	N-Ch		11		
			P-Ch		11		
Reverse Transfer Capacitance	C _{rss}		N-Ch		5		
			P-Ch		5		
Turn On Time	t _{d(on)}	N Channel V _{DD} = 3 V, R _L = 100 Ω	N-Ch		7	12	ns
Rise Time	t _r	I _D = 0.25 A, V _{GEN} = 4.5 V, R _g = 10 Ω	N-Ch		25	35	
			P-Ch		25	35	
Turn Off Delay Time	t _{d(off)}	P-Channel V _{DD} = -3 V, R _L = 100 Ω	N-Ch		19	30	
			P-Ch		19	30	
Fall Time	t _f	I _D = -0.25 A, V _{GEN} = -4.5 V, R _g = 10 Ω	N-Ch		9	15	
			P-Ch		9	15	

*1 Guaranteed by design, not subject to production testing.

*2 Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.