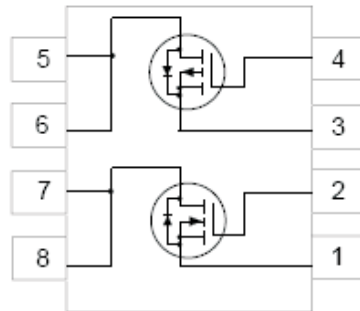
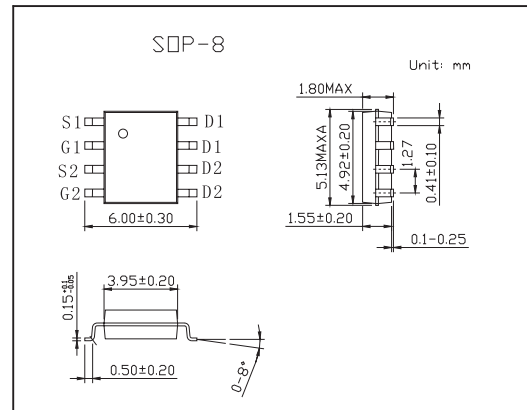


Dual N & P-Channel Enhancement Mode Field Effect Transistor KDS8928A

■ Features

- N-Channel
5.5 A, 30 V $R_{DS(ON)} = 0.030 \Omega$ @ $V_{GS} = 4.5V$
 $R_{DS(ON)} = 0.038 \Omega$ @ $V_{GS} = 2.5V$
- P-Channel
-4 A, -20 V $R_{DS(ON)} = 0.055 \Omega$ @ $V_{GS} = -4.5 V$
 $R_{DS(ON)} = 0.070 \Omega$ @ $V_{GS} = -2.5V$
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and handling capability in a widely used surface mount package
- Dual (N & P-Channel) MOSFET in surface mount package.



■ Absolute Maximum Ratings $T_a = 25^\circ C$

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage	V_{DSS}	30	30	V
Gate to Source Voltage	V_{GS}	8	-8	V
Drain Current Continuous (Note 1a)	I_D	5.5	-4	A
Drain Current Pulsed		20	-20	A
Power Dissipation for Single Operation	P_D	2		W
Power Dissipation for Single Operation (Note 1a)	P_D	1.6		W
(Note 1b)		1		
(Note 1c)		0.9		
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150		$^\circ C$
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78		$^\circ C/W$
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40		$^\circ C/W$

KDS8928A

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit	
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	30		V	
		V _{GS} = 0 V, I _D = -250 μA	P-Ch	-20			
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I _D = 250 μA, Referenced to 25°C	N-Ch		32	mV/°C	
		I _D = -250 μA, Referenced to 25°C	P-Ch		-23		
Zero Gate Voltage Drain Current	I _{DSS}	V _{Ds} = 24V, V _{GS} = 0 V	N-Ch		1	μA	
		V _{Ds} = -16 V, V _{GS} = 0 V	P-Ch		-1		
Gate-Body Leakage	I _{GSS}	V _{GS} = ±8V, V _{Ds} = 0 V	N-Ch		±100	nA	
		V _{GS} = ±8 V, V _{Ds} = 0 V	P-Ch		±100		
Gate Threshold Voltage	V _{GS(th)}	V _{Ds} = V _{GS} , I _D = 250 μA	N-Ch	0.4	0.67	V	
		V _{Ds} = V _{GS} , I _D = -250 μA	P-Ch	-0.4	-0.6		
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I _D = 250 μA, Referenced to 25°C	N-Ch		-3	mV/°C	
		I _D = -250 μA, Referenced to 25°C	P-Ch		4		
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 5.5A	N-Ch		0.025	0.03	mΩ
		V _{GS} = 2.5 V, I _D = 4.5A			0.031	0.038	
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -4 A	P-Ch		0.043	0.055	
		V _{GS} = -2.5 V, I _D = -3.4 A			.059	0.072	
On-State Drain Current	I _{D(on)}	V _{GS} = 4.5 V, V _{Ds} = 5V	N-Ch	20		A	
		V _{GS} = -4.5 V, V _{Ds} = -5V	P-Ch	-20			
Forward Transconductance	g _{FS}	V _{Ds} = 5V, I _D = 5.5A	N-Ch		20	S	
		V _{Ds} = -5V, I _D = -4A	P-Ch		13		
Input Capacitance	C _{iss}	N-Channel V _{Ds} = 10 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		900	pF	
			P-Ch		1130		
Output Capacitance	C _{oss}	P-Channel	N-Ch		410	pF	
			P-Ch		480		
Reverse Transfer Capacitance	C _{rss}	V _{Ds} = -10 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		110	pF	
			P-Ch		120		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 6 V, I _D = 1 A,	N-Ch		6	12	ns
			P-Ch		8	16	
Turn-On Rise Time	t _r	V _{GS} = 4.5 V, R _{GEN} = 6 Ω (Note 2)	N-Ch		19	31	ns
			P-Ch		23	37	
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = -10 V, I _D = -1 A,	N-Ch		42	67	ns
			P-Ch		260	360	
Turn-Off Fall Time	t _f	V _{GS} = -4.5 V, R _{GEN} = 6 Ω (Note 2)	N-Ch		13	24	ns
			P-Ch		90	125	
Total Gate Charge	Q _g	N-Channel V _{Ds} = 10V, I _D = 5.5A, V _{GS} = 4.5V (Note 2)	N-Ch		19.8	28	nC
			P-Ch		20	28	
Gate-Source Charge	Q _{gs}	P-Channel	N-Ch		2		nC
			P-Ch		2.8		
Gate-Drain Charge	Q _{gd}	V _{Ds} = -5V, I _D = -4A, V _{GS} = -5V (Note 2)	N-Ch		6.3		nC
			P-Ch		3.2		

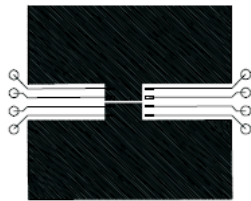
KDS8928A

■ Electrical Characteristics Ta = 25°C

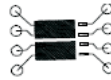
Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Maximum Continuous Drain-Source Diode Forward Current	Is	N-Ch			1.3	A
		P-Ch			-1.3	
Drain-Source Diode Forward Voltage	VSD	VGS = 0 V, Is = 1.3A (Not 2)		0.68	1.2	V
		VGS = 0 V, Is = -1.3A (Not 2)		-0.7	-1.2	

Notes:

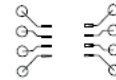
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 78°C/W on a 0.5 in² pad of 2oz copper.



b. 125°C/W on a 0.02 in² pad of 2oz copper.



c. 135°C/W on a 0.003 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.