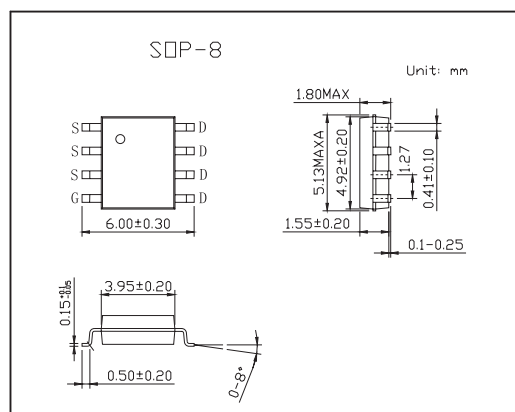
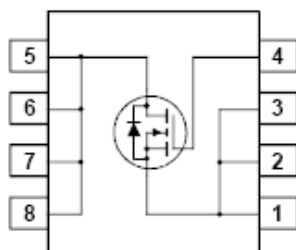


40V N-Channel PowerTrench MOSFET

KDS4470

■ Features

- 12.5 A, 40 V. $R_{DS(ON)} = 9\text{m}\Omega$ @ $V_{GS} = 10\text{ V}$
- Low gate charge (45 nC typical)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DS}	40	V
Gate to Source Voltage	V_{GS}	+30/-20	V
Drain Current Continuous (Note 1a)	I_D	12.5	A
Drain Current Pulsed		50	A
Power dissipation (Note 1a)	P_D	2.5	W
Power dissipation (Note 1b)		1.4	
Power dissipation (Note 1c)		1.2	
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient (Note 1c)	$R_{\theta JA}$	125	$^\circ\text{C/W}$
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	25	$^\circ\text{C/W}$

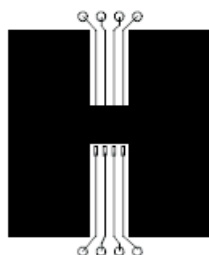
KDS4470

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Avalanche Energy	EAS	Single Pulse, V _{DD} =40V, I _D =12.5A(Not 2)			370	mJ
Drain-Source Avalanche Current	I _{AS}	(Not 2)			12.5	A
Drain-Source Breakdown Voltage	B _V DSS	V _{GS} = 0 V, I _D = 250 μA	40			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta B_{V_{DSS}}}{\Delta T_J}$	I _D = 250 μA, Referenced to 25°C		42		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 32 V, V _{GS} = 0 V			1	μA
Gate-Body Leakage, Forward	I _{GSSF}	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
Gate-Body Leakage, Reverse	I _{GSSR}	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	3.9	5	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I _D = 250 μA, Referenced to 25°C		-8		mV/°C
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 12.5 A		6	9	mΩ
		V _{GS} = 10 V, I _D = 12.5 A, T _J = 125°C		9	14	
On-State Drain Current	I _{D(on)}	V _{GS} = 10 V, V _{DS} = 5 V	25			A
Forward Transconductance	g _{FS}	V _{DS} = 10V, I _D = 12.5 A		45		S
Input Capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1.0 MHz		2659		pF
Output Capacitance	C _{oss}			605		pF
Reverse Transfer Capacitance	C _{rss}			298		pF
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω (Note 2)		14	25	ns
Turn-On Rise Time	t _r			12	22	ns
Turn-Off Delay Time	t _{d(off)}			37	59	ns
Turn-Off Fall Time	t _f			29	46	ns
Total Gate Charge	Q _g	V _{DS} = 20 V, I _D = 12.5 A, V _{GS} = 10 V (Note 2)		45	63	nC
Gate-Source Charge	Q _{gs}			27		nC
Gate-Drain Charge	Q _{gd}			5		nC
Maximum Continuous Drain-Source Diode Forward Current	I _S				2.1	A
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = 2.1 A (Not 2)		0.7	1.2	V
Diode Reverse Recovery Time	t _{rr}	I _F = 12.5 A, di _F /dt = 100 A/μs		33		nS
Diode Reverse Recovery Charge	Q _{rr}			39		nC

Notes:

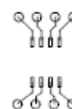
1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a) 50°C/W when mounted on a 1in² pad of 2 oz copper



b) 105°C/W when mounted on a .04 in² pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%