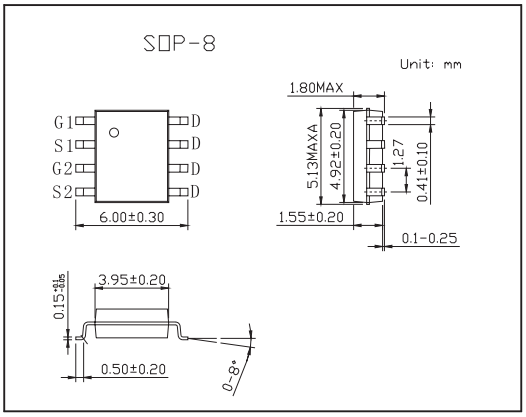
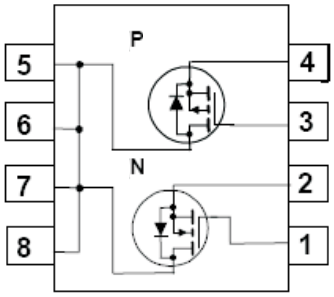
20V N & P-Channel PowerTrench MOSFET

KDR8702H

■ Features

- N-Ch $R_{DS(ON)}$ = 54mΩ @ V_{GS} = 2.5 V
  3.6 A, 20 V $R_{DS(ON)}$ = 38mΩ @ V_{GS} =4.5V
- P-Ch $R_{DS(ON)}$ = 110 mΩ @ VGS =- 2.5 V
  -2.6 A, -20 V $R_{DS(ON)}$ = 80 mΩ @ V_{GS} =-4.5V
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$





■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage	V_{DSS}	20	-20	V
Gate to Source Voltage	V_{GS}	±12	±8	V
Drain Current Continuous (Note 1a)	I_D	3.6	-2.6	A
Drain Current Pulsed		15	-10	A
Power Dissipation for Single Operation (Note 1a)	P_D	0.8		W
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150		℃
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	146		℃/W
Thermal Resistance Junction to Ambient (Note 1b)	$R_{\theta JA}$	76		℃/W
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40		℃/W

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	B_{VDSS}	V_{GS} = 0 V, I_D = 250 μA	N-Ch	20			V
		V_{GS} = 0 V, I_D = -250 μA	P-Ch	-20			
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃	N-Ch		36		mV/℃
		I_D = -250 μA, Referenced to 25℃	P-Ch		-15		
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0 V	N-Ch			1	μA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-1	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0 V	N-Ch			±100	nA
		V_{GS} = ±8 V, V_{DS} = 0 V	P-Ch			±100	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	N-Ch	0.6	0.8	1.5	V
		V_{DS} = V_{GS}, I_D = -250 μA	P-Ch	-0.4	-0.7	-1.6	
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃	N-Ch		-2		mV/℃
		I_D = -250 μA, Referenced to 25℃	P-Ch		2.5		
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D =3.6A	N-Ch		31	38	mΩ
		V_{GS} = 2.5 V, I_D = 3.1 A			42	54	
		V_{GS} = 4.5 V, I_D =3.6 A,TJ = 125℃			41	58	
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -4.5 V, I_D =-2.6 A	P-Ch		66	80	
		V_{GS} = -2.5 V, I_D =-2.2 A			85	110	
		V_{GS} = -4.5 V, I_D =-2.6 A,TJ = 125℃			83	108	
On-State Drain Current	$I_{D(on)}$	V_{GS} = 4.5 V, V_{DS} = 5V	N-Ch	10			A
		V_{GS} = -4.5 V, V_{DS} = -5V	P-Ch	-10			
Forward Transconductance	g_{FS}	V_{DS} = V_{GS}, I_D = 250 μA	N-Ch		15		S
		V_{DS} = V_{GS}, I_D = -250 μA	P-Ch		9		
Gate Resistance	R_G	V_{GS} = 15 mV, f = 1.0 MHz	N-Ch		1		Ω
			P-Ch		4.8		
Input Capacitance	C_{iss}	N-Channel	N-Ch		650		pF
		V_{DS} = 10 V, V_{GS} = 0 V,f = 1.0 MHz	P-Ch		607		
Output Capacitance	C_{oss}		N-Ch		170		pF
		P-Channel	P-Ch		165		
Reverse Transfer Capacitance	C_{rss}	V_{DS} = -10 V, V_{GS} = 0 V,f = 1.0 MHz	N-Ch		80		pF
			P-Ch		60		
Turn-On Delay Time	$t_{d(on)}$	N-Channel	N-Ch		8	16	ns
		V_{DD} = 10 V, I_D = 1 A,	P-Ch		12	22	
Turn-On Rise Time	tr	V_{GS} = 4.5 V, R_{GEN} = 6 Ω	N-Ch		9	18	ns
			P-Ch		11	20	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel	N-Ch		16	29	ns
		V_{DD} = -10 V, I_D = -1 A,	P-Ch		26	42	
Turn-Off Fall Time	tf	V_{GS} = -4.5 V, R_{GEN} = 6 Ω	N-Ch		7	14	ns
			P-Ch		8	16	

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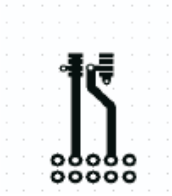
Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Total Gate Charge	Q_g	N-Channel	N-Ch		7	10	nC
		V_{DS} =10V,I_D=3.6A,V_{GS}=4.5V	P-Ch		6	8	
Gate-Source Charge	Q_{gs}	(Note 2)	N-Ch		1.3		nC
		P-Channel	P-Ch		1.2		
Gate-Drain Charge	Q_{gd}	V_{DS}=-10V,I_D=-2.6A,V_{GS}=-4.5V	N-Ch		2.2		nC
		(Note 2)	P-Ch		1.6		
Maximum Continuous Drain-Source Diode Forward Current	I_S		N-Ch			0.7	A
			P-Ch			-0.7	
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 0.7A (Not 2)	N-Ch		0.7	1.2	V
		V_{GS} = 0 V, I_S = -0.7A (Not 2)	P-Ch		-0.7	-1.2	
Diode Reverse Recovery Time	trr	N-Channel	N-Ch		16		nS
		I_F =3.6A,di_F/dt = 100 A/μs	P-Ch		22		
Maximum Reverse Recovery Current	Irm		N-Ch		0.6		A
		P-Channel	P-Ch		0.7		
Diode Reverse Recovery Charge	Qrr	I_F =-2.6A,di_F/dt = 100 A/μs	N-Ch		5		nC
			P-Ch		8		

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 76°C/W when mounted on a 1in^2 pad of 2 oz copper



b) 146°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%