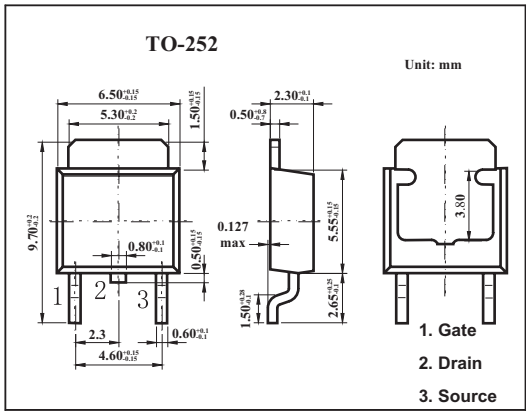
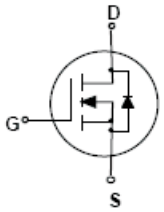
30V N-Channel Power Trench MOSFET

KDD6030L



■ Features

- 12 A, 30 V. $R_{DS(ON)}$ = 14.5mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 21mΩ @ V_{GS} = 4.5 V
- Low gate charge
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$



■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current Continuous @Tc=25℃ (Note 3)	I_D	50	A
@Ta=25℃ (Note 1a)		12	A
Drain Current Pulsed (Note 1a)		100	A
Power dissipation @ Tc=25℃ (Note 3)	P_D	56	W
Power dissipation @ Ta=25℃ (Note 1a)		3.2	
Power dissipation @ Ta=25℃ (Note 1b)		1.5	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	℃
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	2.7	℃/W
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	45	℃/W
Thermal Resistance Junction to Ambient (Note 1b)	$R_{\theta JA}$	96	℃/W

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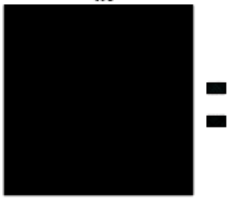
■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Avalanche Energy	E_{AS}	Single Pulse, V_{DD} = 15 V, I_D= 12A (Note 2)			100	mJ
Maximum Drain-Source Avalanche Current	I_{AR}	(Not 2)			12	A
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃		24		mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1	1.9	3	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃		-5		mV/℃
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 12A		7.7	14.5	mΩ
		V_{GS} = 4.5 V, I_D = 10A		9.9	21	
		V_{GS} = 10 V, I_D =12 A,T_J = 125℃		11.4	25	
On-State Drain Current	$I_{D(on)}$	V_{GS} = 10 V, V_{DS} = 5 V	50			A
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 12 A		47		S
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V,f = 1.0 MHz		1230		pF
Output Capacitance	C_{oss}			325		pF
Reverse Transfer Capacitance	C_{rss}			150		pF
Gate Resistance	R_G	V_{GS} = 15 mV, f = 1.0 MHz		1.5		pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 1 A,V_{GS} = 10 V, R_{GEN} = 6 Ω (Note 2)		10	19	ns
Turn-On Rise Time	t_r			7	13	ns
Turn-Off Delay Time	$t_{d(off)}$			29	46	ns
Turn-Off Fall Time	t_f			12	21	ns
Total Gate Charge	Q_g	V_{DS} = 15 V, I_D = 12 A,V_{GS} = 5 V (Note 2)		13	28	nC
Gate-Source Charge	Q_{gs}			3.5		nC
Gate-Drain Charge	Q_{gd}			5.1		nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				2.7	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, Is = 2.9 A (Not 2)		0.76	1.2	V
Diode Reverse Recovery Time	trr	I_F = 12 A, di_F/dt = 100 A/μs		24		nS
Diode Reverse Recovery Charge	Qrr			13		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA}$ = 45°C/W when mounted on a 1in² pad of 2 oz copper

b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at T_C = 25°C and $R_{DS(on)}$ is at $T_{J(max)}$ and V_{GS} = 10V. Package current limitation is 21A