

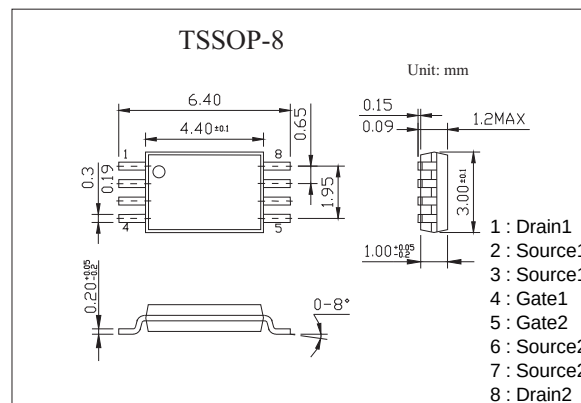
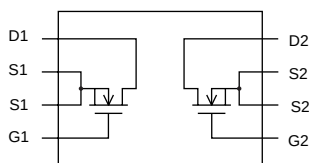
Dual N-Channel Enhancement Mode MOSFET

FTD2011

Features

$R_{DS(ON)}=30m\Omega$ Max. @ $V_{GS}=4V$

$R_{DS(ON)}=45m\Omega$ Max. @ $V_{GS}=2.5V$

Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 10	V
Drain-Current	I_D	5	A
		20	A
Power Dissipation	P_D	1.3	W
Thermal Resistance, Junction- to-Ambient	$R_{\theta JA}$	96	$^\circ\text{C/W}$
Operating Junction and Storage Temperature Range	T_j, T_{stg}	-55 to 150	$^\circ\text{C}$

Note: 1. PW 10 μs , duty cycle 1%

2. Mounted on a ceramic board (1000mm²×0.8mm)

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Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{DSS}	V _{GS} =0V, I _D =1mA	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V			1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±8V, V _{DS} =0V			±10	μA
Cutoff Voltage	V _{GS(off)}	V _{DS} =10V, I _D =1mA	0.5		1.3	V
Drain- Source on-state Resistance	R _{DS(ON)}	V _{GS} =4V, I _D =4A			30	mΩ
		V _{GS} =2.5V, I _D =2A			45	mΩ
On-State Drain Current	I _{D(ON)}	V _{DS} =5V, V _{GS} =4.5V	18			A
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =5A	5			S
Input Capacitance	C _{iss}	V _{DS} = 10V, V _{GS} = 0V, f = 1.0MHz		900		pF
Output Capacitance	C _{oss}			260		pF
Reverse Transfer Capacitance	C _{rss}			200		pF
Turn-On Delay Time	t _{D(on)}	V _{DD} =10V, I _D =4A, V _{GS} =4V, R _L =2.5Ω, R _{GEN} =50Ω		15		ns
Rise Time	t _r			150		ns
Turn-Off Delay Time	t _{D(off)}			100		ns
Fall Time	t _f			150		ns
Total Gate Charge	Q _g	V _{DS} = 10V, I _D = 4A, V _{GS} = 10V		32		nC
Gate-Source Charge	Q _{gs}			1.5		nC
Gate-Drain Charge	Q _{gd}			6		nC

Marking

Marking	2011
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