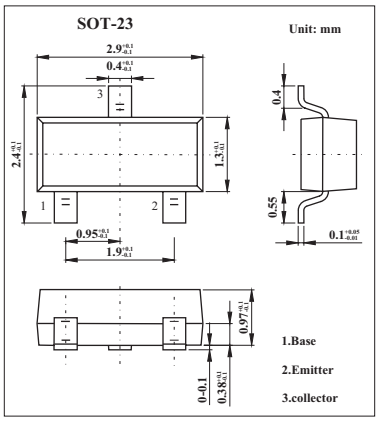
PNP Epitaxial Planar Silicon Transistors

2SA1338



■ Features

- Adoption of FBET process.
- High breakdown voltage : V_{CEO}=-50V.
- Large current capacitiy and high f_T.
- Ultrasmall-sized package permitting sets to be smallsized, slim.

■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Collector-base voltage	V_{CBO}	-60	V
Collector-emitter voltage	V_{CEO}	-50	V
Emitter-base voltage	V_{EBO}	-5	V
Collector current	I_C	-500	mA
Collector current (pulse)	I_{CP}	-800	mA
Collector dissipation	P_C	200	mW
Jumction temperature	T_j	150	℃
Storage temperature	T_{stg}	-55 to +150	℃

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Collector cutoff current	I_{CBO}	V_{CB} = -40V , I_E = 0			-0.1	μA
Emitter cutoff current	I_{EBO}	V_{EB} = -4V , I_C = 0			-0.1	μA
DC current Gain	h_{FE}	V_{CE} = -5V , I_C = -10mA	100		560	
Gain bandwidth product	f_T	V_{CE} = -10V , I_C = -50mA		200		MHz
Common base output capacitance	Cob	V_{CB} = -10V , f = 1MHz		5.6		pF
Collector-to-emitter saturation voltage	$V_{CE(sat)}$	I_C = -100mA , I_B =-10mA		0.15	0.4	V
Base-to-emitter saturation voltage	$V_{BE(sat)}$	I_C = -100mA , I_B =-10mA		0.8	1.2	V
Collector-to-base breakdown voltage	$V_{(BR)CBO}$	I_C = -10μA , I_E = 0	-60			V
Collector-to-emitter breakdown voltage	$V_{(BR)CEO}$	I_C = -100μA , R_{BE} = ∞	-50			V
Emitter-to-base breakdown voltage	$V_{(BR)EBO}$	I_E = -10μA , I_C = 0	-5			V
Turn-on time	t_{on}	V_{CC} = 20V, I_C = -10I_{B1} = -10I_{B2} = 100mA		70		ns
Storage time	t_{stg}			400		ns
Fall time	t_f			50		ns

■ h_{FE} Classification

Marking	AL			
Rank	4	5	6	7
hFE	100～200	140～280	200～400	280～560