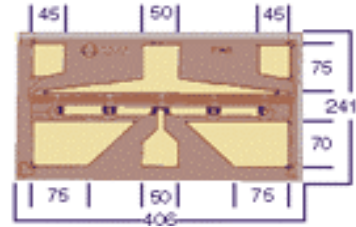


Features:

- 18.0 dB typical Small Signal Gain at 12 GHz
- +20.0 dBm typical Output Power at 12 GHz
- 2 x 0.3 x 300 Micron Refractory Metal/Gold Gate
- Sorted into 5 mA Idss Bin Ranges
- Excellent for High Gain and Medium Power Applications
- Ideal for Commercial, Military, Hi-Rel Space Applications



Chip Dimensions: 406 x 241 microns
Chip Thickness: 100 microns

Description:

The MwT-PH5 is a dual gate AlGaAs/InGaAs PHEMT (Pseudomorphic-High-Electron-Mobility-Transistor) device whose nominal 0.3 micron gate length and 300 micron gate width make it ideally suited for applications requiring high-gain and power up to 30 GHz frequency range. The device is equally effective for either wideband (e.g. 6 to 18 GHz) or narrow-band applications. The chip is produced using MwT's reliable metal systems and all devices from each wafer are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability.

Electrical Specifications:

• at $T_a = 25\text{ }^\circ\text{C}$

SYMBOL	PARAMETERS & CONDITIONS	FREQ	UNITS	MIN	TYP
P1dB	Output Power at 1dB Compression $V_{ds}=7.0\text{ V}$ $I_{ds}=0.6 \times I_{DSS}=48\text{ mA}$	12 GHz	dBm	18.0	20.0
SSG	Small Signal Gain $V_{DS}=7.0\text{ V}$ $I_{ds}=0.6 \times I_{DSS}=48\text{ mA}$	12 GHz	dB	15.0	18.0
PAE	Power Added Efficiency at P1dB $V_{DS}=7.0\text{ V}$ $I_{ds}=0.6 \times I_{DSS}=48\text{ mA}$	12 GHz	%		30
NFopt	Optimum Noise Figure $V_{ds}=3.0\text{ V}$ $I_{ds}=20\text{ mA}$	12 GHz	dB		2.0
GA	Small Signal Gain $V_{ds}=3.0\text{ V}$ $I_{ds}=20\text{ mA}$	12 GHz	dB		12.0
IDSS	Recommended IDSS Range for Optimum P1dB		mA		40-120

DC Specifications: • at $T_a = 25\text{ }^\circ\text{C}$

SYMBOL	PARAMETERS & CONDITIONS	UNITS	MIN	TYP	MAX
IDSS	Saturated Drain Current $V_{ds}=3.0\text{ V}$ $V_{gs}=0.0\text{ V}$	mA	40		120
Gm	Transconductance $V_{ds}=2.5\text{ V}$ $V_{gs}=0.0\text{ V}$	mS	40	60	
Vp	Pinch-off Voltage $V_{ds}=3.0\text{ V}$ $V_{gs2}=0\text{ V}$ $I_{ds}=0\text{ mA}$	V		-1.2	-2.5
BVGSO	Gate-to-Source Breakdown Voltage $I_{gs} = -0.4\text{ mA}$	V	-6.0	-12.0	
BVGDO	Gate-to-Drain Breakdown Voltage $I_{gd} = -0.4\text{ mA}$	V	-10.0	-13.0	
Rth	Chip Thermal Resistance	$^\circ\text{C/W}$		150*	

* Overall Rth depends on case mounting

MAXIMUM RATINGS AT $T_a = 25\text{ }^\circ\text{C}$

Symbol	Parameter	Units	Cont Max1	Absolute Max2
VDS	Drain to Source Voltage	V	6.5	7.0
Tch	Channel Temperature	$^\circ\text{C}$	+150	+175
Tst	Storage Temperature	$^\circ\text{C}$	-65 to+150	+175
Pin	RF Input Power	mW	80	120
Pt	Total Power Dissipation	mW	800	1000

Notes:

1. Exceeding any one of these limits in continuous operation may reduce the mean-time- to-failure below the design goal.
2. Exceeding any one of these limits may cause permanent damage.

ORDERING INFORMATION:

When placing order or inquiring, please specify BIN range, wafer number, if known, and visual screening level required. For details of BIN Selection and Safe Handling Procedure please see supplementary information in available PDF on our website www.mwtinc.com.

BIN SELECTION

BIN #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
IDSS	30-	35-	40-	45-	50-	55-	60-	65-	70-	75-	80-	85-	90-	95-	100-	105-
(mA)	35	40	45	50	55	60	65	70	75	80	85	90	95	100	105	110