MicroWave Technology
An IXYS Company

MwT-LN300

26 GHz Super Low Noise pHEMT Device

May 2010

FEATURES

- **0.6 dB Minimum Noise Figure at 12 GHz**
- **10.0 dB Associated Gain at 12 GHz**
- **15.0 dBm P1dB at 12 GHz**
- **0.15 Micron x 300 Micron Gate**

APPLICATIONS

- **Excellent Choice for Super Low Noise Applications**
- **Ideal for Commercial, Military, Hi-Rel Space Applications**

DESCRIPTION

The MwT-LN300 is a super low noise, quasi-enhancement-mode pHEMT whose nominal 0.15 micron gate length and 300 micron gate width makes it ideally suited for applications requiring very low noise and high associated gain up to 30 GHz. The device is equally effective for wideband (e.g. 6 to 18 GHz) and narrow-band applications. Each wafer can be screened to meet the high quality and reliability requirements for space and military applications.

RF SPECIFICATIONS AT Ta = 25 C

SYMBOL	PARAMETERS & CONDITIONS	FREQ	UNITS	MIN	TYP	MAX
NF min	Minimum Noise Figure Vds=2.5V Ids = 25 mA (Vgs=0)	4 GHz 12 GHz	dB		0.2 0.6	
SSG	Associated Gain Vds=2.5V Ids = 25 mA (Vgs=0)	4 GHz 12 GHz	dB		13.0 10.0	
P1dB	Output Power at 1dB Compression Vds=3.0V Ids = 50 mA	12 GHz	dBm		16.0	

Note: MWT-LN300 is a quasi enhancement mode device. For best noise figure, Vgs bias voltage should be set at either 0 or slightly positive voltages to achieve the target operating current.

DC SPECIFICATIONS AT Ta = 25 C

SYMBOL	PARAMETERS & CONDITIONS	FREQ	UNITS	MIN	TYP	MAX
Imax	Saturated Drain Current Vds = 2.5V Vgs = 0.6V		mA		120	
Gm	Transconductance Vds = 2.5V Vgs = 0.2V		mS	160	200	
Vp	Pinch-off Voltage Vds = 2.0V Ids = 0.5mA		V		-0.2	
BVGSO	Gate-to-Source Breakdown Voltage Igs = -0.3mA		V	-6.0	-8.0	
BVGDO	Gate-to-Drain Breakdown Voltage Igd = -0.3mA		V	-7.5	-9.0	
Rth *	Chip Thermal Resistance		ºC/W		180	

* Overall Rth depends on chip mounting

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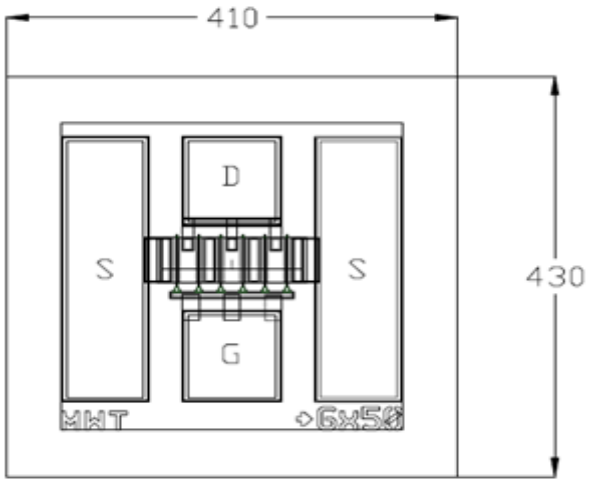
NOISE PARAMETERS Vds=2.5V, Ids=25mA

Freq (GHz)	NFmin (dB)	GA (dB)	Gamma Opt		Rn/50
			Mag	Ang	
2	0.17	16.5	0.803	-7.7	0.12
4	0.2	13.0	0.799	19.3	0.12
6	0.28	11.2	0.781	42.8	0.12
8	0.37	10.3	0.753	63.1	0.11
10	0.46	9.8	0.719	80.5	0.1
12	0.55	9.5	0.682	95.2	0.09
14	0.65	9.2	0.644	107.6	0.08
16	0.74	9.0	0.611	118.1	0.07
18	0.83	8.7	0.584	126.8	0.07
20	0.92	8.0	0.568	134.2	0.07
22	1.02	7.6	0.565	140.4	0.07
24	1.11	7.2	0.58	145.9	0.06
26	1.2	6.7	0.615	150.8	0.06

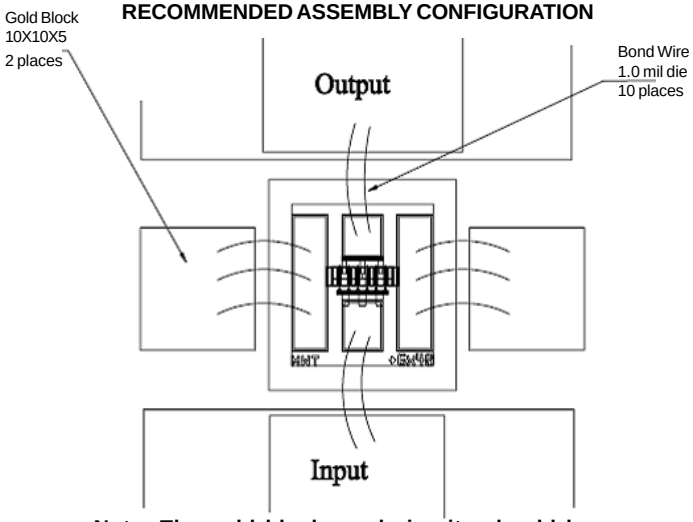


Chip Dimensions: 410 x 430 microns
Source pad: 80 x 280
Gate and Drain pad: 90 x 90
Chip Thickness: 100 microns

S-PARAMETERS V=2.5V, Ids=25mA

F	S11		S21		S12		S22		K	GMAX
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang		dB
1	0.93	-31.9	12.22	158.6	0.032	69.9	0.40	-31.2	0.20	25.9
2	0.90	-58.9	10.82	144.5	0.056	56.3	0.41	-61.2	0.15	22.8
3	0.87	-80.5	9.37	132.7	0.073	45.1	0.41	-83.7	0.14	21.1
4	0.86	-97.0	8.09	123.5	0.084	36.9	0.42	-99.8	0.15	19.8
5	0.84	-109.9	7.03	116.1	0.091	30.5	0.42	-112.0	0.15	18.9
6	0.84	-119.7	6.18	110.2	0.097	25.4	0.43	-120.7	0.16	18.0
7	0.83	-127.7	5.49	105.1	0.100	21.1	0.43	-127.7	0.17	17.4
8	0.83	-134.6	4.92	100.6	0.102	17.9	0.44	-133.4	0.18	16.8
9	0.83	-139.8	4.46	96.8	0.104	14.6	0.44	-137.8	0.18	16.3
10	0.83	-144.7	4.06	93.3	0.104	11.9	0.44	-141.8	0.21	15.9
11	0.82	-148.5	3.72	90.2	0.106	10.3	0.44	-144.9	0.24	15.5
12	0.81	-151.7	3.45	87.6	0.106	8.0	0.44	-147.2	0.26	15.1
13	0.82	-154.4	3.20	84.8	0.106	5.9	0.44	-149.2	0.27	14.8
14	0.81	-157.2	3.00	82.2	0.106	4.5	0.45	-151.2	0.30	14.5
15	0.82	-159.7	2.80	79.6	0.105	2.8	0.45	-153.0	0.30	14.3
16	0.82	-162.0	2.63	77.3	0.107	0.8	0.45	-154.2	0.29	13.9
17	0.82	-164.4	2.49	74.9	0.106	-0.6	0.45	-156.1	0.33	13.7
18	0.80	-166.3	2.35	72.9	0.106	-1.2	0.45	-157.0	0.40	13.5
19	0.80	-167.9	2.22	70.6	0.106	-3.5	0.45	-158.2	0.42	13.2
20	0.81	-169.2	2.11	68.3	0.107	-3.9	0.45	-159.4	0.43	12.9
21	0.81	-170.7	2.02	66.8	0.105	-5.5	0.46	-159.7	0.43	12.8
22	0.80	-172.1	1.93	64.4	0.105	-4.3	0.46	-161.2	0.51	12.6
23	0.80	-172.9	1.84	62.9	0.105	-7.8	0.46	-161.6	0.50	12.4
24	0.81	-173.6	1.77	61.1	0.103	-8.6	0.46	-162.7	0.52	12.3
25	0.79	-175.6	1.69	59.2	0.102	-8.5	0.47	-163.1	0.60	12.2
26	0.79	-176.9	1.62	57.4	0.107	-7.89	0.46	-163.5	0.61	11.8

RECOMMENDED ASSEMBLY CONFIGURATION



Note: The gold blocks and circuits should be placed as close to the device as possible. The bond wire should be as short as possible.

MAXIMUM RATINGS at Ta = 25 C

Symbol	Parameters	Units	Cont Max 1	Absolute Max 2
VDS	Drain to Source Voltage	V	4.0	4.5
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +160	+180
Pin	RF Input Power	mW	20	40
Pt	Total Power Dissipation	mW	300	400

Exceeding any on of these limits in continuous operation may reduce the mean-time-to-failure below the design goal and may cause permanent damage

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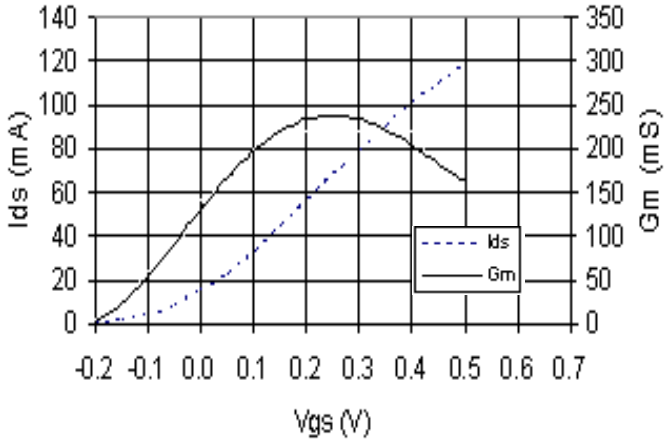
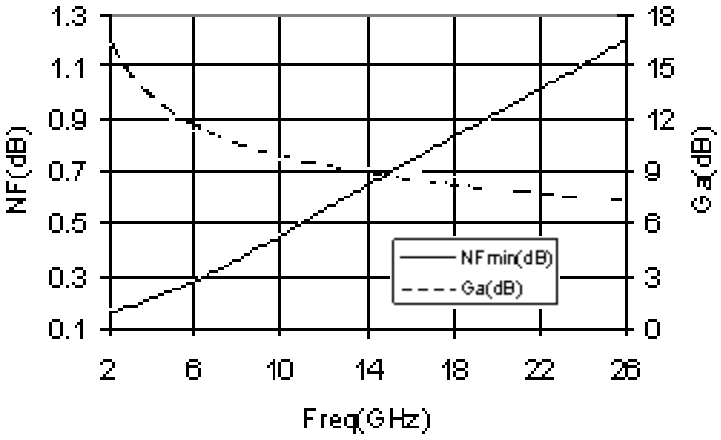
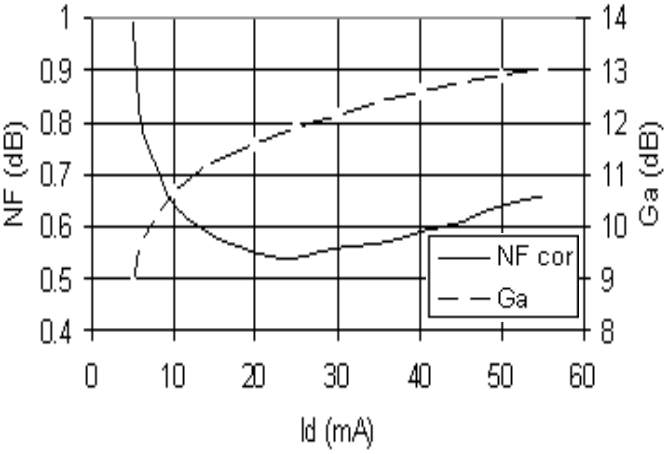
Gm & Ids vs. Vgs
Vds = 2.5V



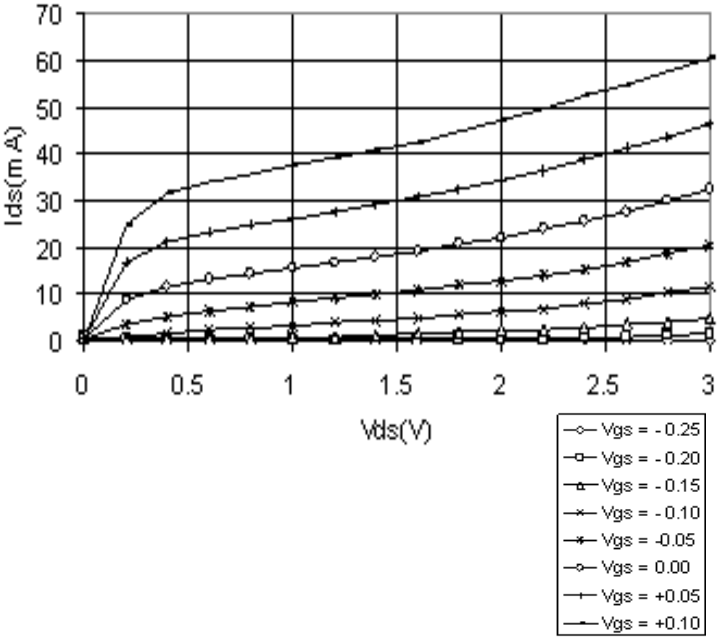
NF & Associated Gain vs. Freq
Vds = 2.5V, Ids = 20mA



NF & Ga vs. Ids
Freq = 12GHz, Vds = 2.5V



DC IV Characteristics



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