MLA-06183A-R4

5 - 18 GHz Low-Noise MMIC Amplifier
Data Sheet Rev A
May 2010

FEATURES

- **Wide Band:** **5 to 18 GHz**
- **NF (ext match):** **3.4 dB @ 6 GHz**
  3.0 dB @ 12 GHz
  3.7 dB @ 18 GHz
- **P-1dB:** **21 dBm**
- **OIP3:** **29 dBm**
- **Gain:** **19 db**
- **Bias Condition:** **VDD = 4.5V**
  IDD = 135 mA
- **50-Ohm On-chip Matching**
- **Unconditionally Stable from 50 MHz to 20 GHz**

APPLICATIONS

- **Microwave Radios**
- **Satellite Communications**
- **EW Systems**
- **Military Systems**
- **Commercial Wireless Systems**

DESCRIPTION

The MLA-06183A is a fully-matched 2-stage broadband low-noise MMIC amplifier utilizing high-reliability low-noise GaAs PHEMT technology. This MMIC is suited for microwave radios, wideband EW, military, satellite communications, instrumentation, and commercial communication systems, where low-noise figure and high-gain are desirable. It has excellent gain of 19 dB and Noise Figure of 3 dB @ 12 GHz. Typical P-1dB is 21 dBm and OIP3 is + 29 dBm @ 12 GHz. It has on-chip bias circuit, choke, and DC blocking to provide bias stability and ease of use.

ELECTRICAL SPECIFICATIONS: *VDD1, VDD2=+4.5V,VG2/VG2=-0.025 (2), IDD=135mA, Ta=25 C, ZO=50 ohm (1)*

PARAMETER	TEST CONDITIONS	TYPICAL DATA	UNITS
Frequency Range		5-18	GHz
Gain	6 - 8 GHz 8 - 14 GHz 14 - 17.5 GHz 18 GHz	20 19 18 16	dB
Gain Flatness	6 - 14 GHz 14 - 18 GHz	0.75 1.25	+/-dB
Input Return Loss	6 - 14 GHz 14 - 18 GHz	9 12	dB
Output Return Loss		12	dB
Output P1dB	6 GHz 12 GHz 18 GHz	17 21 22	dBm
Output IP3 @ 0 dBm/tone, 1 MHz separation	6 GHz 12 GHz 18 GHz	29 29 27	dBm
Noise Figure	6 GHz 12 GHz 18 GHz	3.4 3.0 3.7	dB
Operating Bias Conditions: VDD1, VDD2 IDD	VG1,VG2=-0.025V, typical	+ 4.5 135	V mA
Stability Factor K	0.05 to 20 GHz	> 1	

(1) All data is measured on 50 Ohm carrier, with Dual-Bias Supply and stub tuning shown in the datasheet assembly diagram.
(2) Since the VG bias setting has typical range of -0.1 to +0.1V, VG1, VG2 bias inputs may be directly grounded/bonded to DC ground to convert to single +ve supply operation such that VG = 0V. The bias current will then be fixed and cannot be controlled or shut down by VG input.

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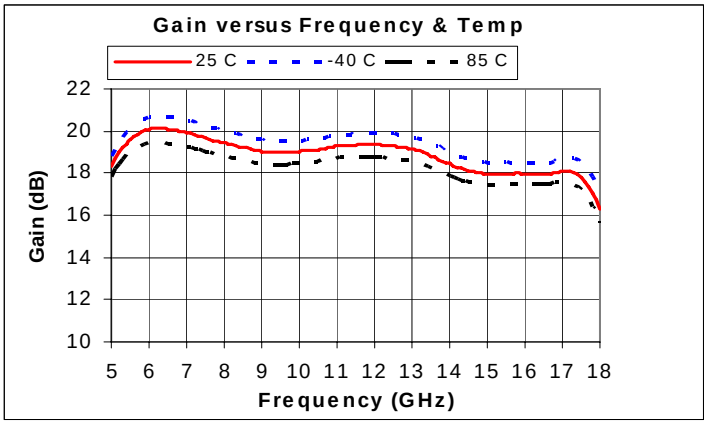
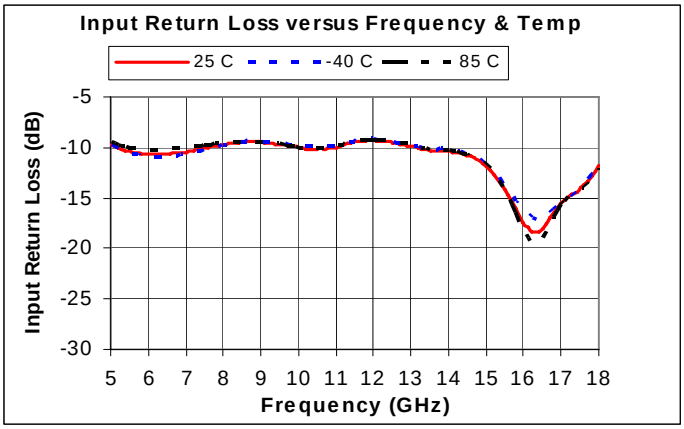
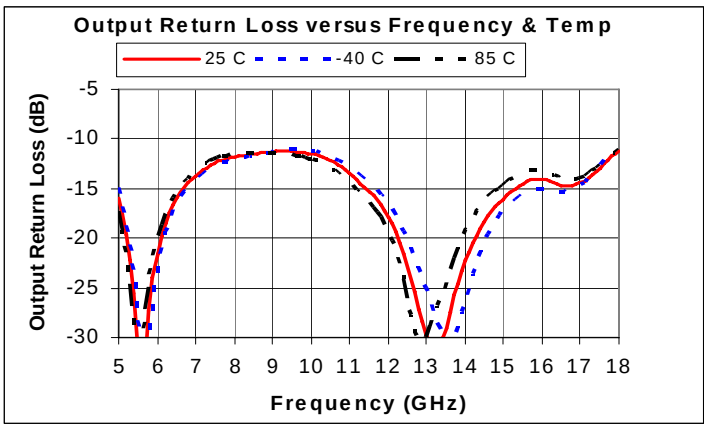
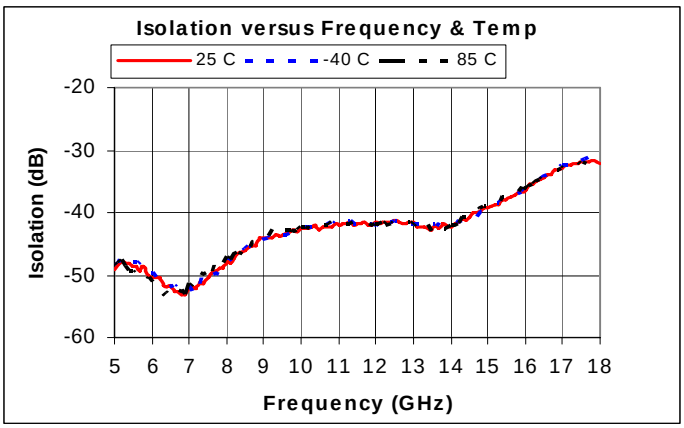
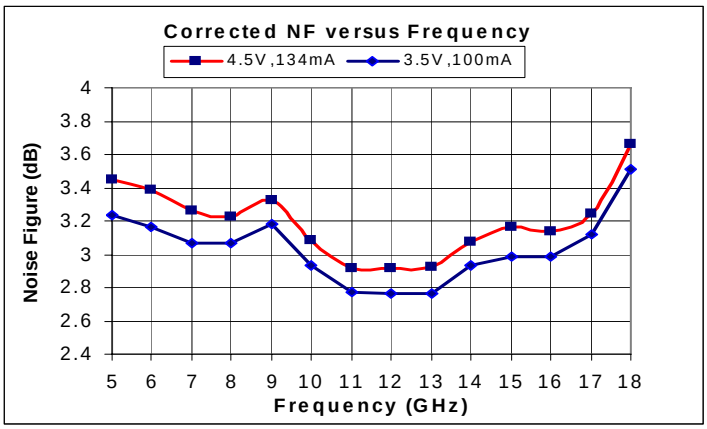
TYPICAL RF PERFORMANCE: *VDD1, VDD2=+4.5V,VG2/VG2=-0.025 (2), IDD=135mA, Ta=25 C, ZO=50 ohm (1)*

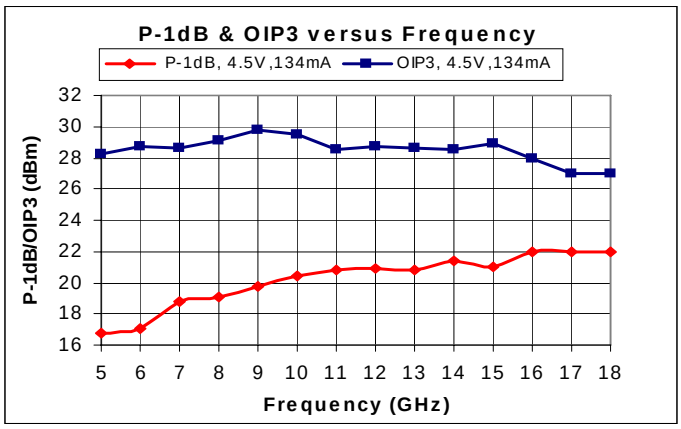












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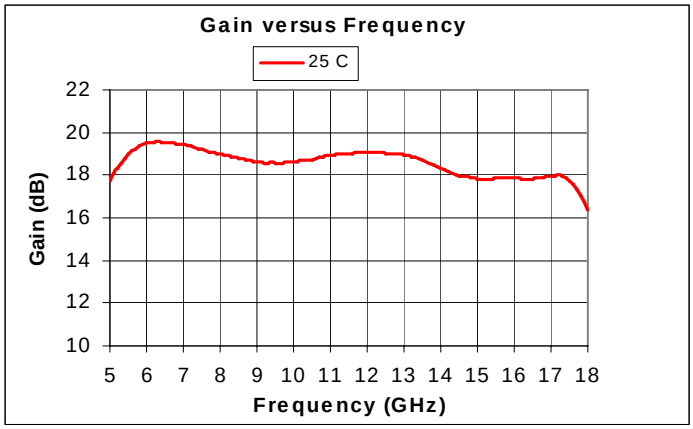

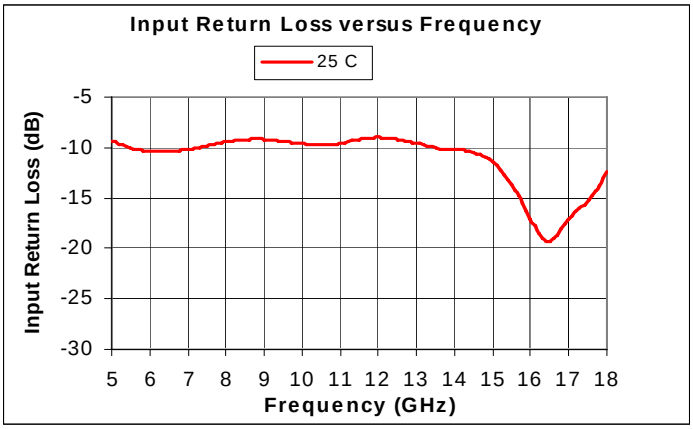

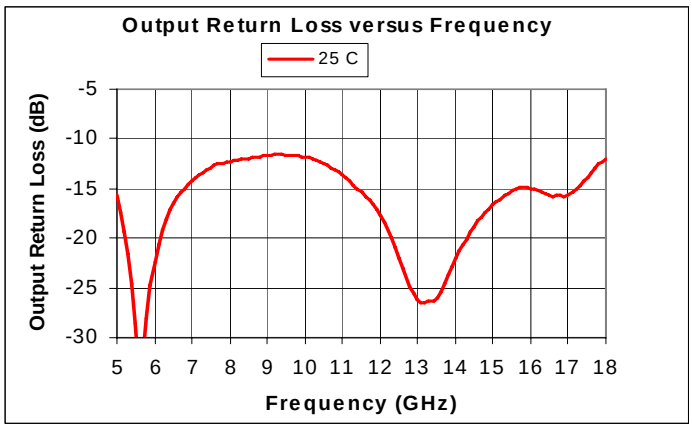

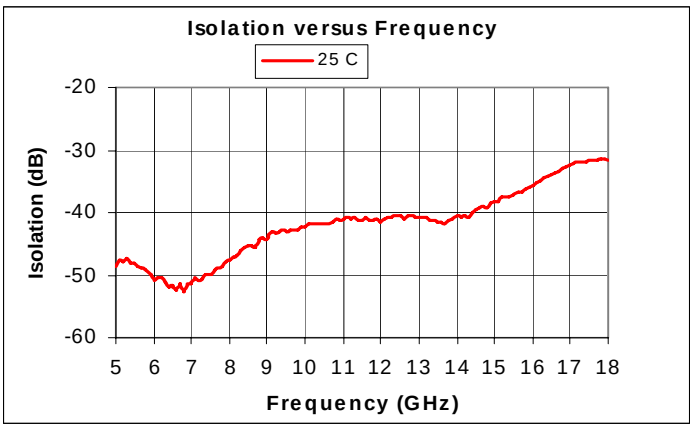

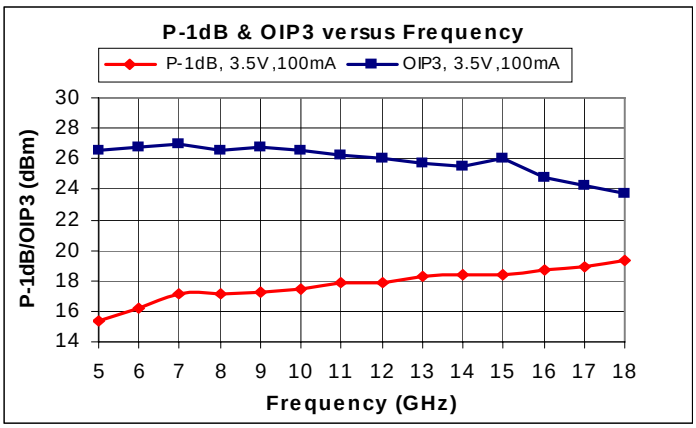

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETERS	UNITS	MAX
VDD	Drain Voltage	V	5.5
IDD	Drain Current	mA	200
Pdiss	DC Power Dissipation	W	0.7
Pin max	RF Input Power	dBm	+13
Toper	Operating Case/Lead Temp Range	°C	-40 to +85
Tch	Channel Temperature	°C	150
Tstg	Storage Temperature	°C	-60 to 150

Exceeding any on of these limits may cause permanent damage.

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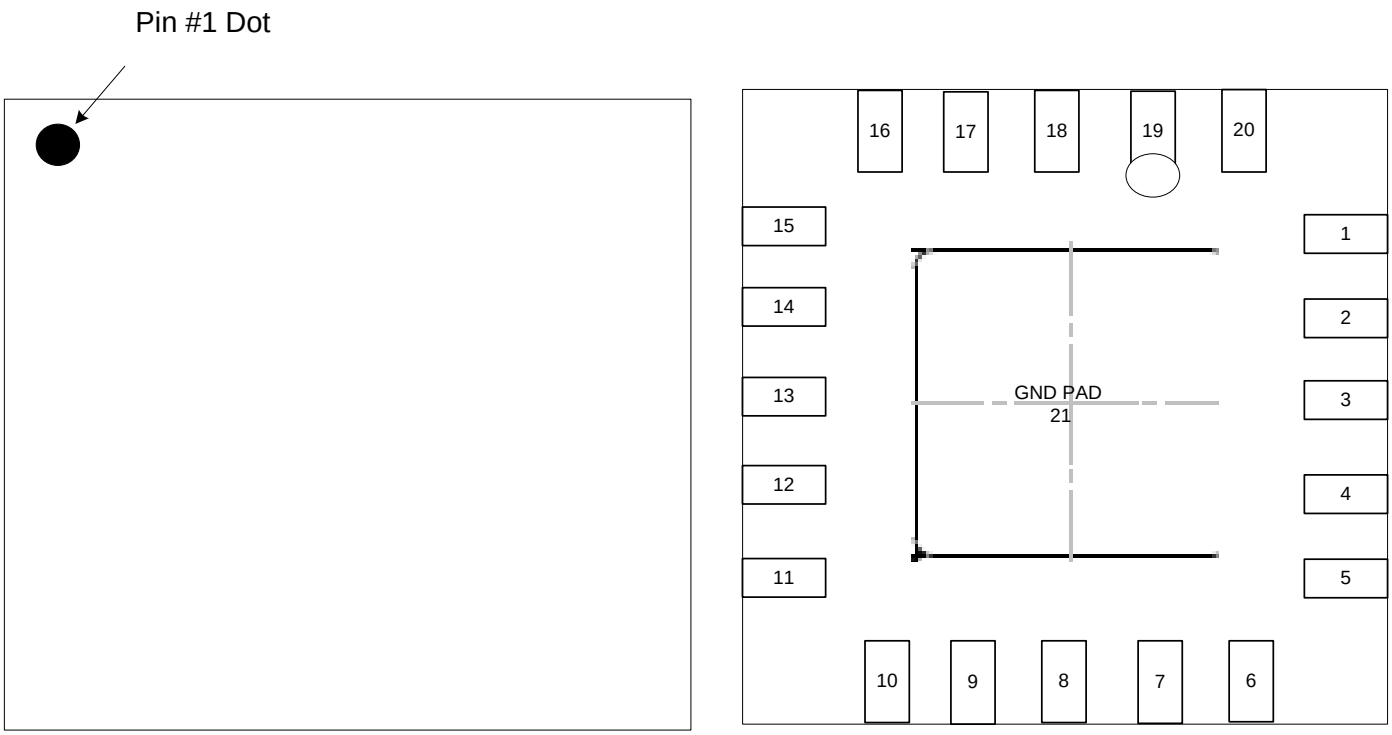
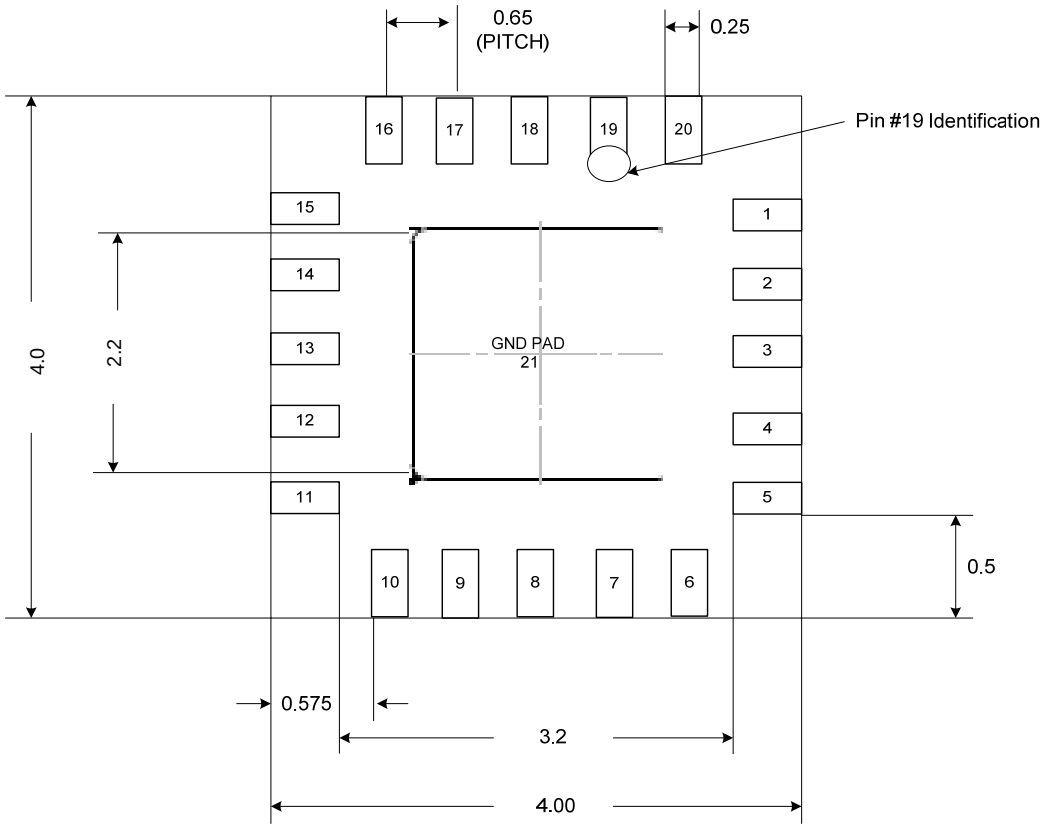
Package Pin-out:

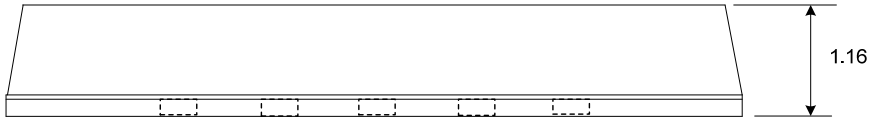


Pin	Description
3	RF Input
13	RF Output
7	Vg1
9	Vg2
19	Vd1
17	Vd2
1, 2, 4, 5 ,6, 10, 11, 12, 14, 15, 16, 20, 21	Ground
8, 18	N/C

Mechanical Information:



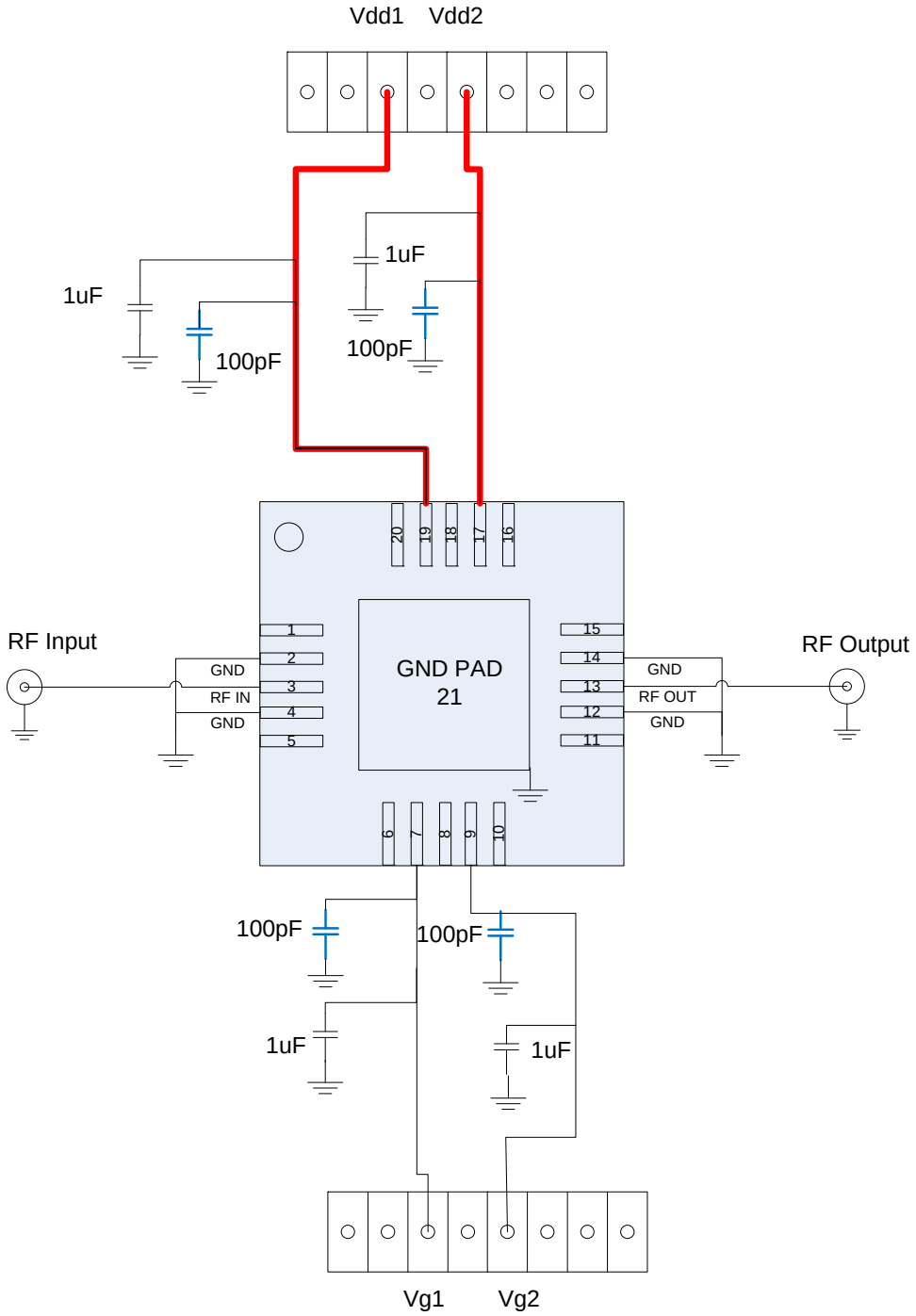
BOTTOM VIEW



SIDE VIEW

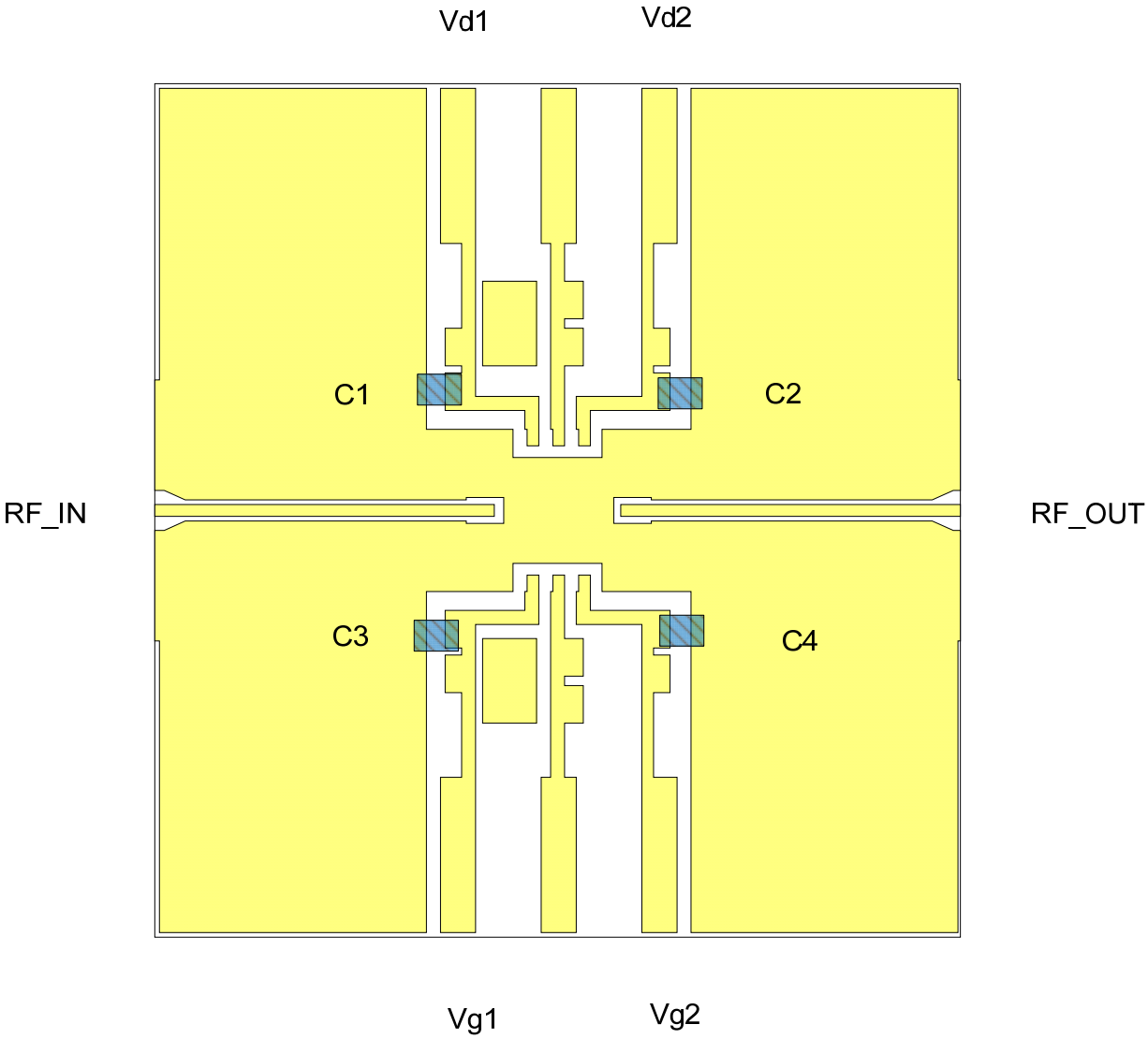
The units are in [mm].

Application Circuit:



Recommended Application Board Design:

Board Material is 10mil (Dielectric) thickness Rogers 4350B with 0.5oz cupper clads.
Board is soldered on a gold plated solid cupper block and adequate heat-sinking is required for 1.5W total maximum power dissipation.



Part	Description
C1, C2, C3, C4	0.1uF capacitor (0603)