Quad Line 12V ESD Protection Diode Array

UESD16V8S4C SOT23-6L

General Description

The UESD16V8S4C of TVS diode array is designed to protect sensitive electronics from damage or latch-up due to ESD, for high voltage applications where board space is at a premium. It is unidirectional device and may be used on lines where the signal polarities are above ground, each device will protect up to four lines.
TVS diodes are solid-state devices feature large cross-sectional area junctions for conducting high transient currents, specifically for transient suppression. It offers desirable characteristics for board level protection including fast response time, low operating, low clamping voltage, and no device degradation.
The UESD16V8S4C may be used to meet the immunity requirements of IEC 61000-4-2, level 4. The small package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

Applications

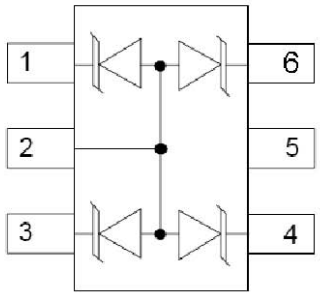
Cellular Handsets & Accessories
Telecom Equipment
Notebooks & Handhelds
Portable Instrumentation
Industrial PC
Industrial Automation

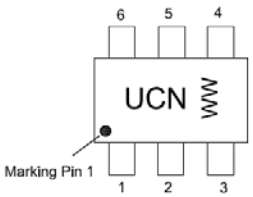
Features

Transient protection for data & power lines to
IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
Protect four I/O lines
Ultra-small SOT23-6L package
Working Voltages: 12V
Low Leakage current
Low operating and clamping voltage
Solid-state silicon avalanche technology

Pin Configurations

Top View





WW: Week Code
UESD16V8S4C
SOT23-6L

Ordering Information

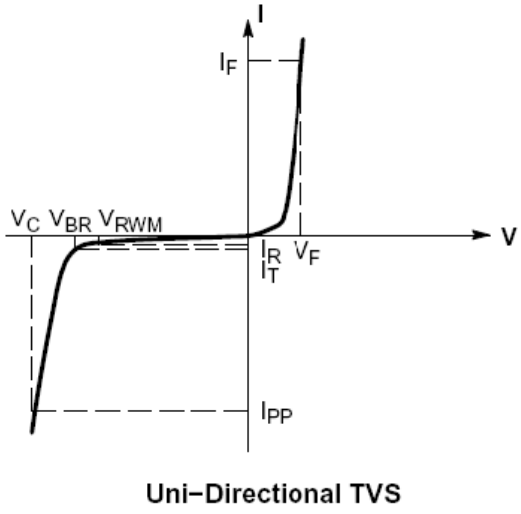
Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UESD16V8S4C	12.0V	SOT23-6L	4	UCN	3000pcs/7 Inch Tape & Reel

Absolute Maximum Ratings

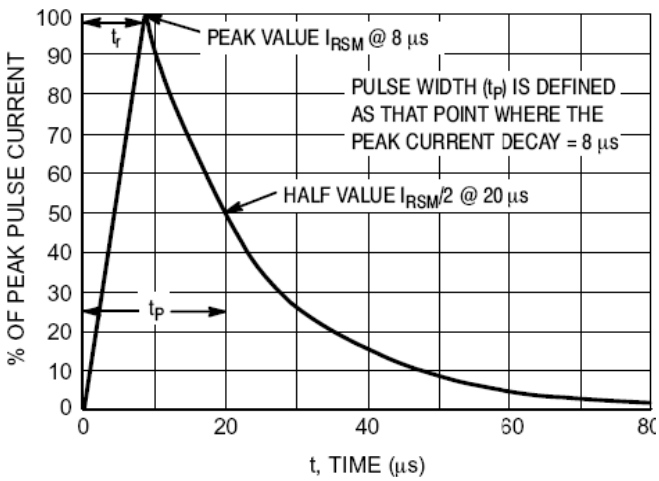
RATING	SYMBOL	VALUE	UNITS
Peak Pulse Power (tp = 8/20μs)	P_{PK}	140	Watts
Maximum Peak Pulse Current (t=8/20μs)	I_{PP}	5.9	Amps
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Symbol Definition

PARAMETER	SYMBOL
Maximum Reverse Peak Pulse Current	I_{PP}
Clamping Voltage @ I_{pp}	V_C
Working Peak Reverse Voltage	V_{RWM}
Maximum Reverse Leakage Current @ V_{RWM}	I_R
Breakdown Voltage @ I_t	V_{BR}
Test Current	I_t
Forward Current	I_F
Forward Voltage @ I_F	V_F
Peak Power Dissipation	P_{PK}
Max. Capacitance @ V_R = 0V, f = 1MHz	C



Uni−Directional TVS



Electrical Characteristics

(T=25°C, Device for 12.0V Reverse Stand-off Voltage)

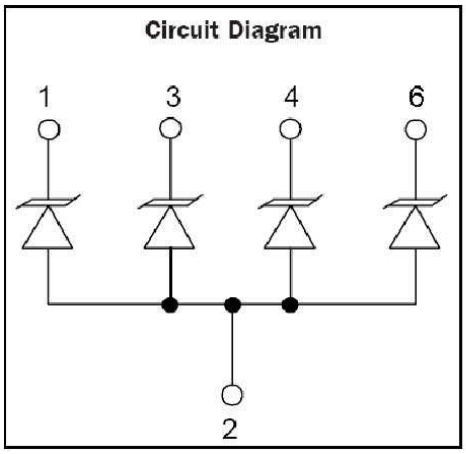
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Reverse Stand-Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	It = 1mA	16		18	V
Reverse Leakage Current	I_R	VRWM = 12V, T=25°C			0.5	μA
Clamping Voltage	V_C	I_{PP} =5.9A, t_p = 8/20μS			23	V
Junction Capacitance	C_J	V_R = 0V, f = 1MHz		20	30	pF

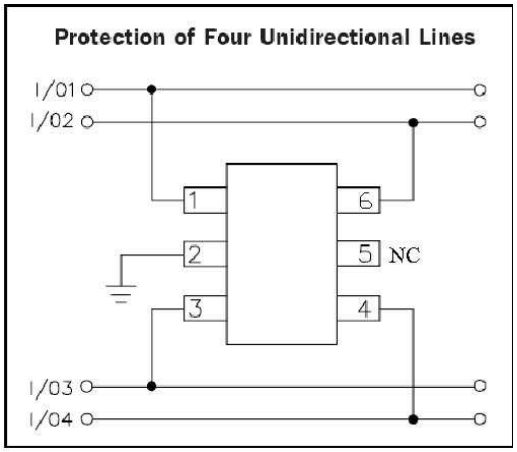
Applications Information

UESD16V8S4C ESD protection diode is designed to protect quad data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode should be placed towards the line that is to be protected.

Device Connection for Protection of Quad Data Lines

The Quad TVS Diode Array is designed to protect up to four unidirectional data lines. The device is connected as follows:
Unidirectional protection of four I/O lines is achieved by connecting pins 1,3,4, and 6 to the data lines. Pin 2 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.





Circuit Board Layout Recommendations for Suppression of ESD

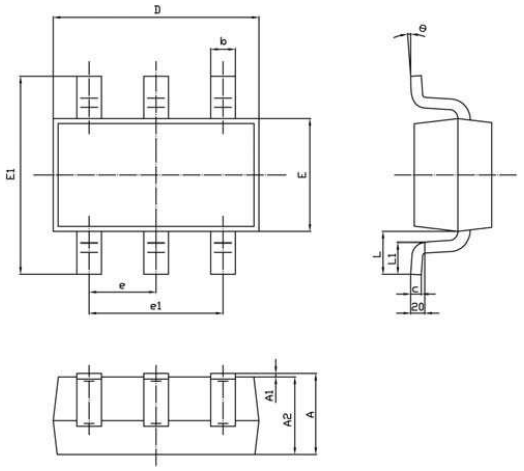
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

Place the TVS near the input terminals or connectors to restrict transient coupling.
Minimize the path length between the TVS and the protected line.
Minimize all conductive loops including power and ground loops.
The ESD transient return path to ground should be kept as short as possible.
Never run critical signals near board edges.
Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.
Keep parallel signal paths to a minimum.
Avoid running protection conductors in parallel with unprotected conductor.
Minimize all printed-circuit board conductive loops including power and ground loops.
Avoid using shared transient return paths to a common ground point.

Package Information

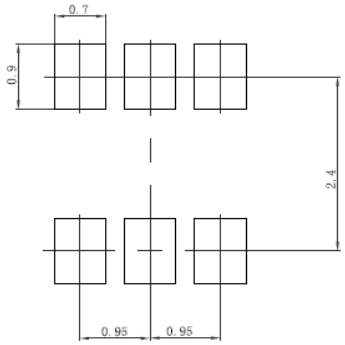
UESD16V8S4C SOT23-6L

Outline Drawing



Symbol	DIMENSIONS			
	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950REF		0.037REF	
e1	1.800	2.000	0.071	0.079
L	0.600REF		0.023REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

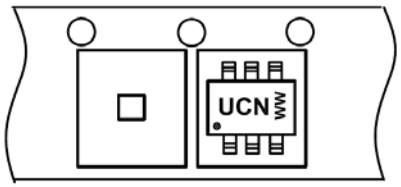
Land Pattern



NOTES:

1. Compound dimension: 2.92×1.60 ;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



IMPORTANT NOTICE

The information in this document has been carefully reviewed and is believed to be accurate. Nonetheless, this document is subject to change without notice. Union assumes no responsibility for any inaccuracies that may be contained in this document, and makes no commitment to update or to keep current the contained information, or to notify a person or organization of any update. Union reserves the right to make changes, at any time, in order to improve reliability, function or design and to attempt to supply the best product possible.

Union Semiconductor, Inc
Add: 7F, No. 5, Bibo Road, Shanghai 201203
Tel: 021-51097928
Fax: 021-51026018
Website: www.union-ic.com