



DESCRIPTION

PT6963 is an LED Controller driven on a 1/5 to 1/8 duty factor. 11 segment output lines, 4 grid output lines, 3 segment/grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to PT6963 via a four-line serial interface. Housed in a 32-pin SOP, PT6963 pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

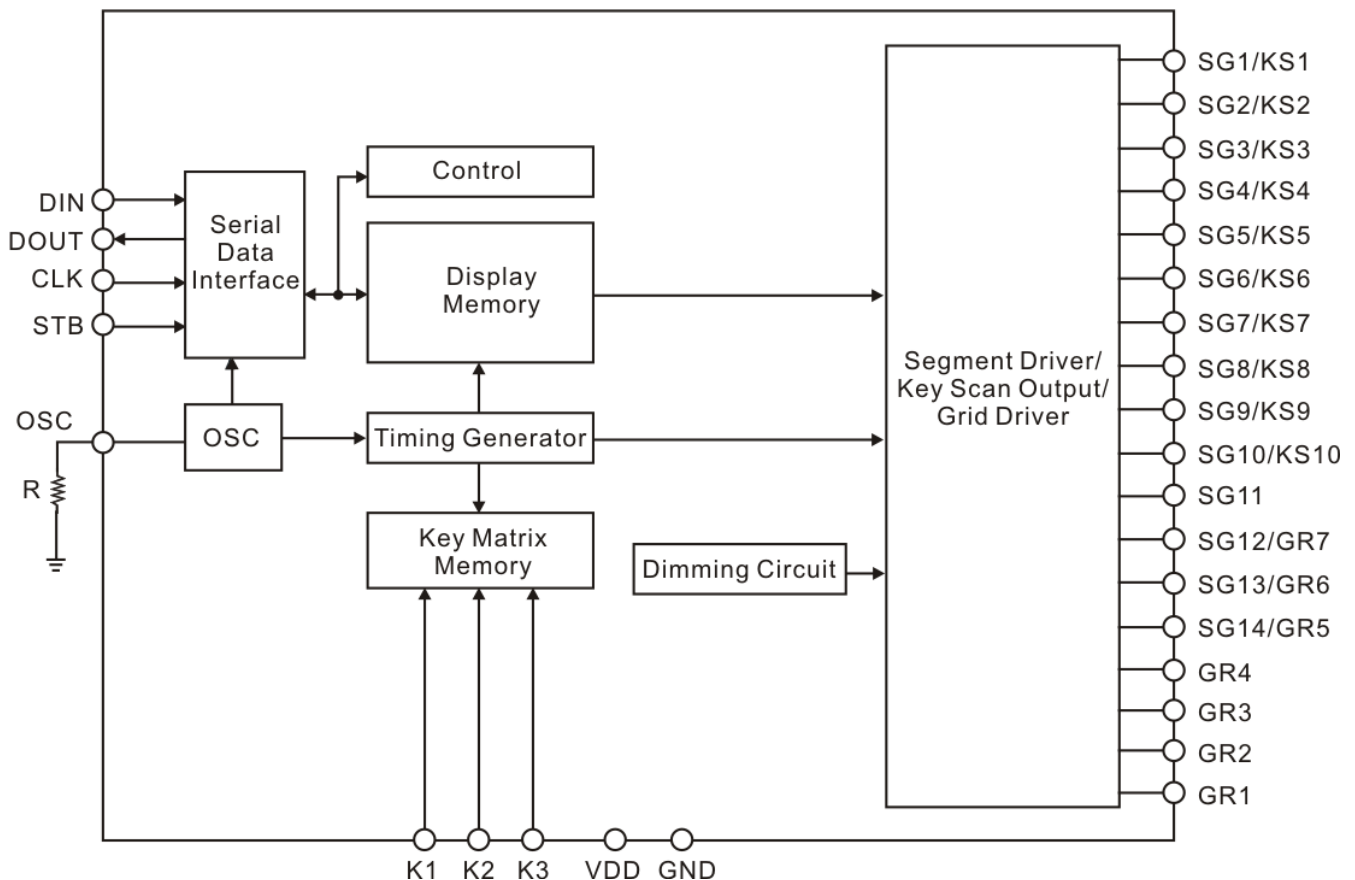
FEATURES

- CMOS technology
- Low power consumption
- Multiple display modes (14 segment, 4 Grid to 11 segment, 7 Grid)
- Key scanning (10 x 3 Matrix)
- 8-Step dimming circuitry
- Serial interface for Clock, Data Input, Data Output, Strobe Pins and low voltage operation ability when user's MCU power supply is 3.3V.
- Available in 32-pin, SOP

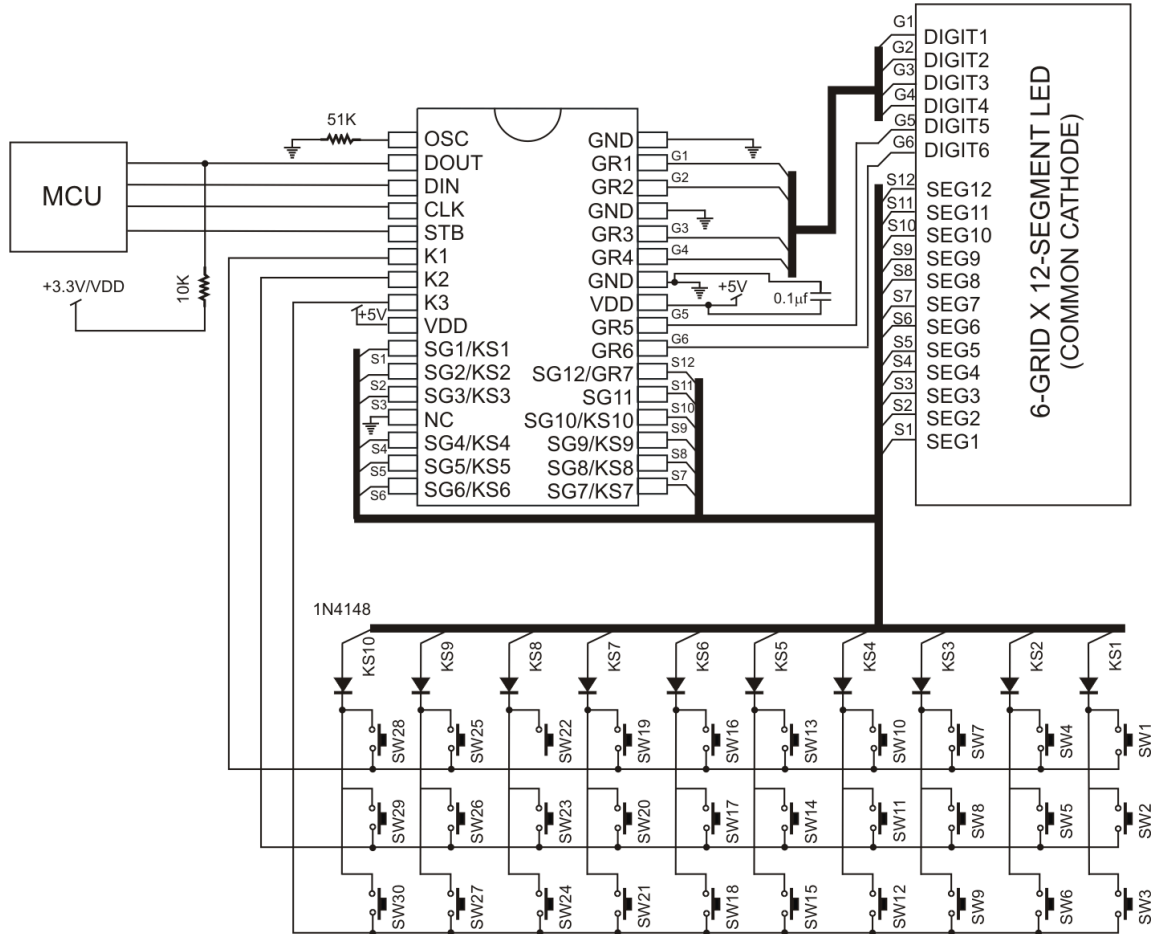
APPLICATIONS

- Micro-computer Peripheral Device
- VCR set
- Combo set

BLOCK DIAGRAM



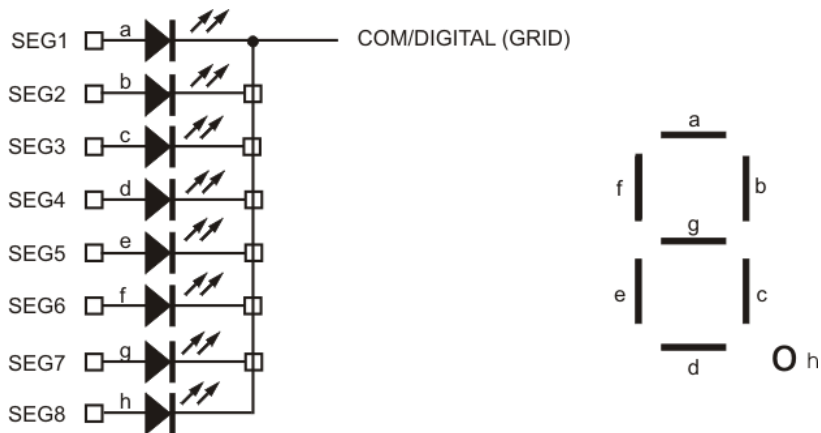
APPLICATION CIRCUIT



Notes:

1. The capacitor (0.1µF) connected between the GND and the VDD pins must be located as close as possible to the PT6963 chip.
2. It is strongly suggested that the NC pin (pins 13) be connected to the GND.
3. The PT6963 power supply is separate from the application system power supply.

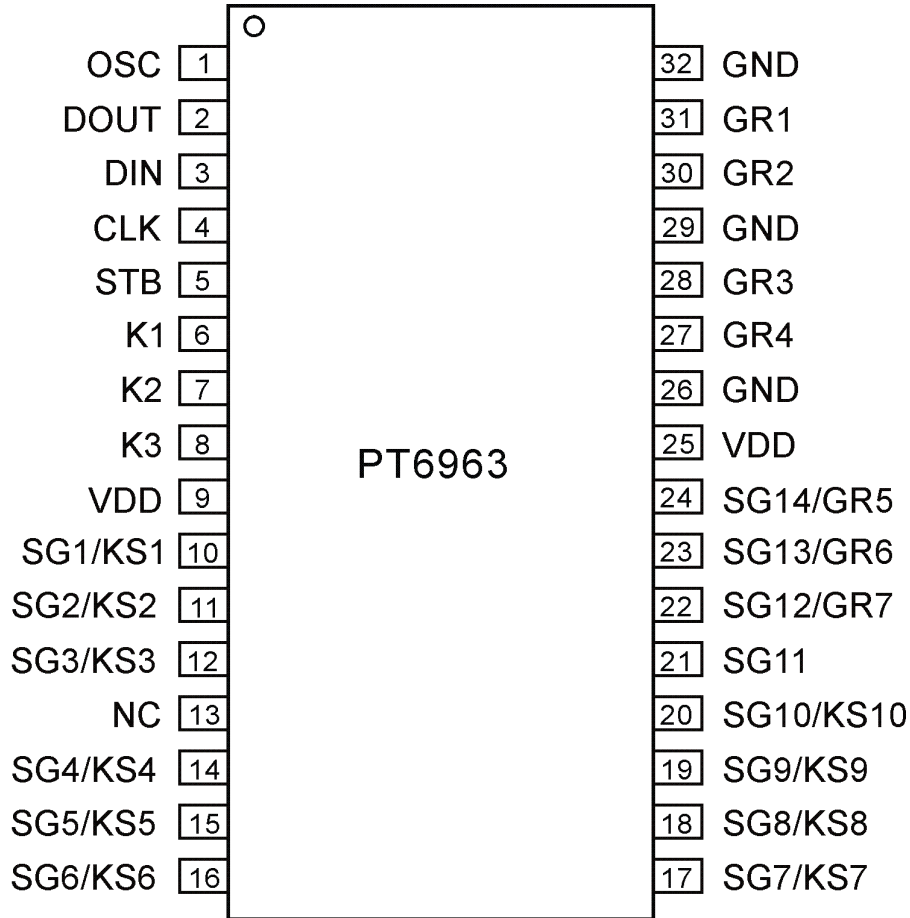
COMMON CATHODE TYPE LED PANEL



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6963-S	32pins, SOP, 300mil	PT6963-S

PIN DESCRIPTION



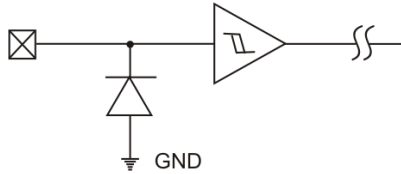
PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency	1
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock.	2
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	3
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	4
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is "HIGH", CLK is ignored.	5
K1 ~ K3	I	Key Data Input Pins The data sent to these pins are latched at the end of the display cycle. (Internal Pull-Low Resistor)	6, 7, 8
VDD	-	Power Supply	9, 25
SG1/KS1 ~ SG10/KS10	O	Segment Output Pins (p-channel, open drain) Also acts as the Key Source	10 ~ 12 14 ~ 20
NC	-	No Connection	13
SG11	O	Segment Output pins (P-Channel, open drain)	21
SG12/GR7 ~ SG14/GR5	O	Segment / Grid Output Pins	22, 23, 24
GND	-	Ground Pin	26, 29, 32
GR4 ~ GR1	O	Grid Output Pins	27, 28, 30, 31

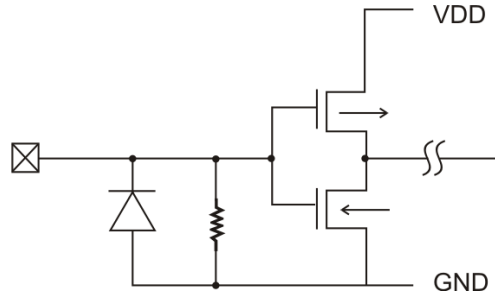
INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below.

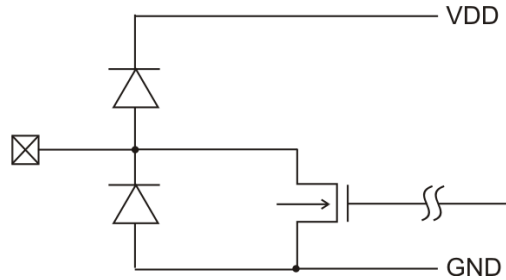
INPUT PINS: CLK, STB & DIN



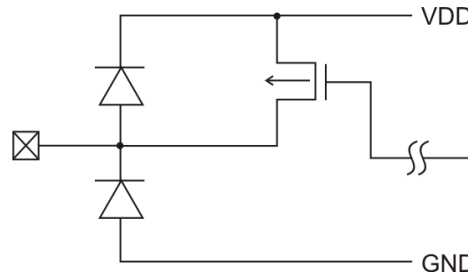
OUTPUT PINS: K1 TO K3



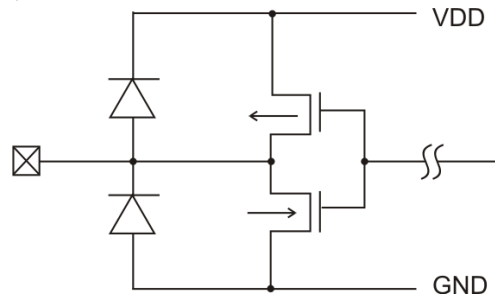
OUTPUT PINS: DOUT, GR1 TO GR4



OUTPUT PINS: SG1 TO SG11

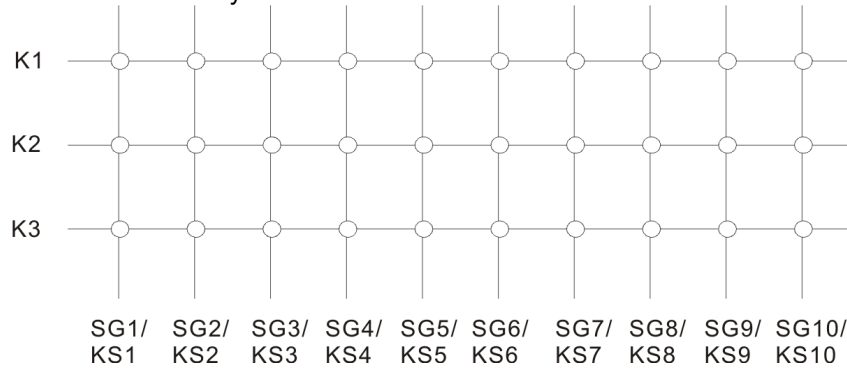


OUTPUT PINS: SG14/GR5, SG13/GR6 AND SG12/GR7

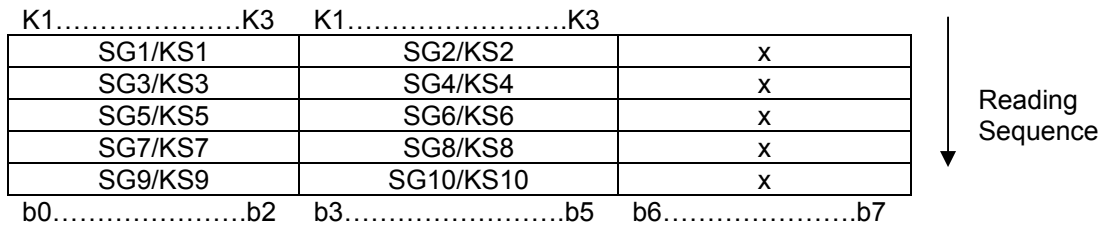


PT6963 KEY MATRIX & KEY INPUT DATA STORAGE RAM

PT6963 Key Matrix consists of 10 x 3 array as shown below:



Each data entered by each key is stored as follows and read by a READ Command, starting from the last significant bit. When the most significant bit of the data (b7) has been read, the least significant bit of the next data (b0) is read.

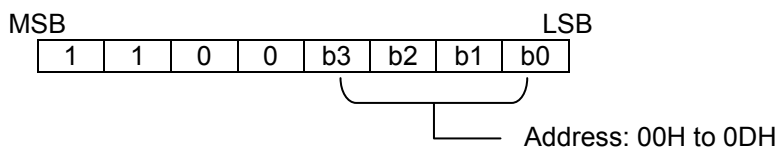


Note: b6 and b7 do not care.

COMMANDS 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of 00H to 0DH. If the address is set to 0EH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at 00H.

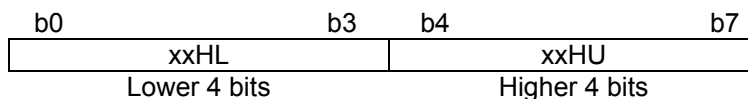
Please refer to the diagram below.



DISPLAY MODE AND RAM ADDRESS

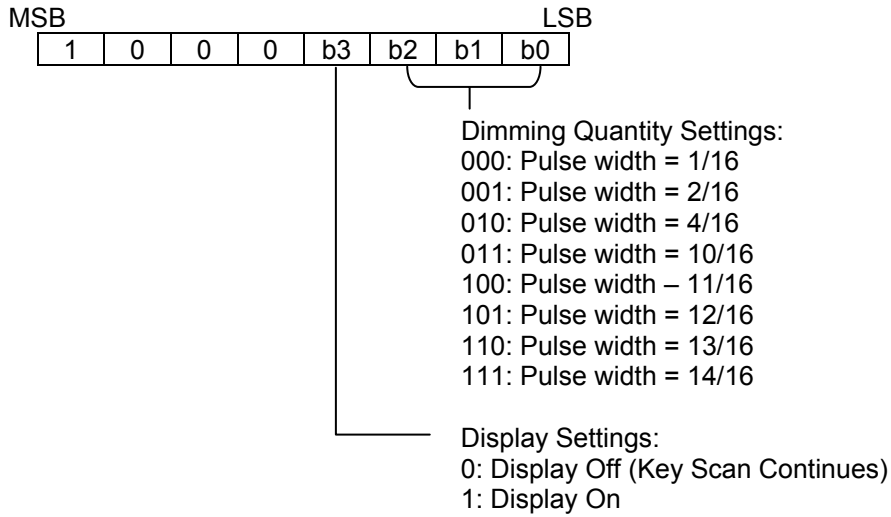
Data transmitted from an external device to PT6963 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM addresses of PT6963 are given below in 8 bits unit.

SG1	SG4	SG5	SG8	SG9	SG12	SG13	SG14	
00HL		00HU		01HL		01HU		DIG1
02HL		02HU		03HL		03HU		DIG2
04HL		04HU		05HL		05HU		DIG3
06HL		06HU		07HL		07HU		DIG4
08HL		08HU		09HL		09HU		DIG5
0AHL		0AHU		0BHL		0BHU		DIG6
0CHL		0CHU		0DHL		0DHU		DIG7

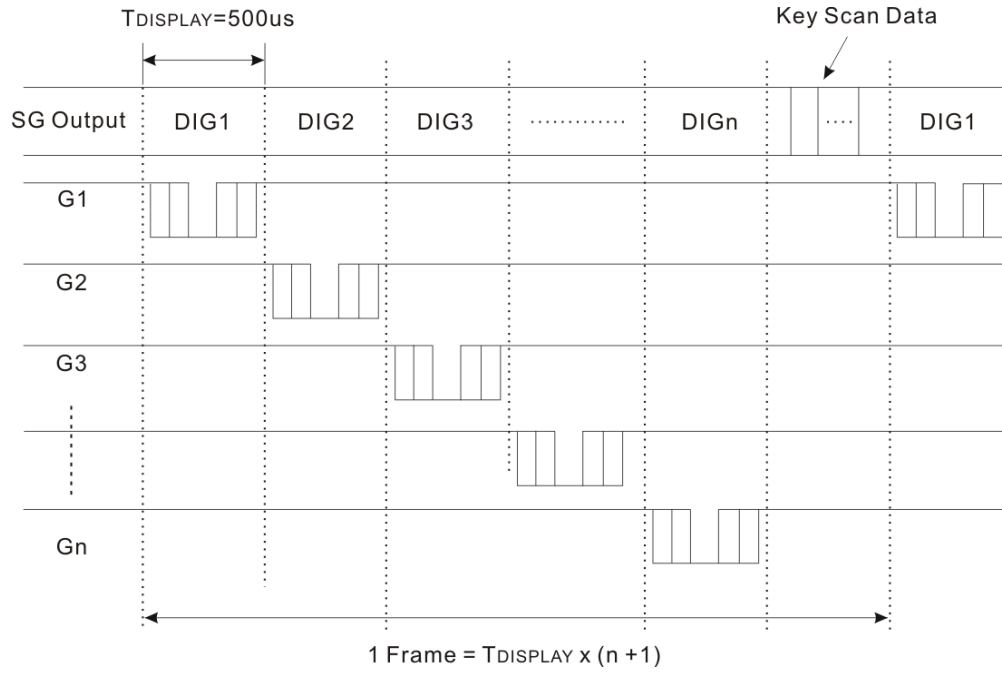


COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is started).



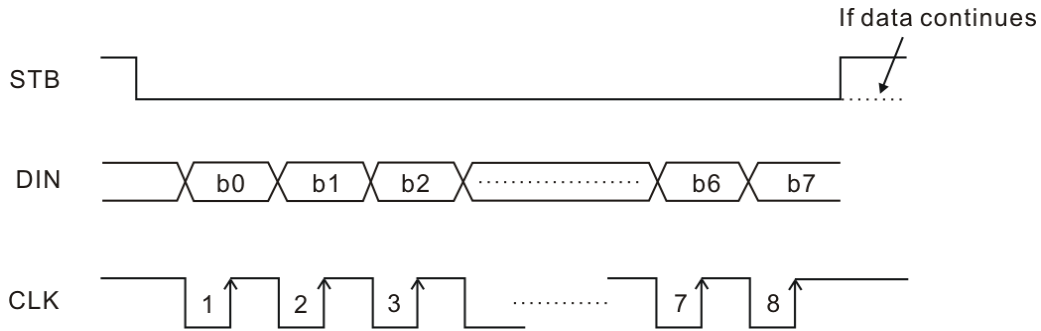
SCANNING AND DISPLAY TIMING



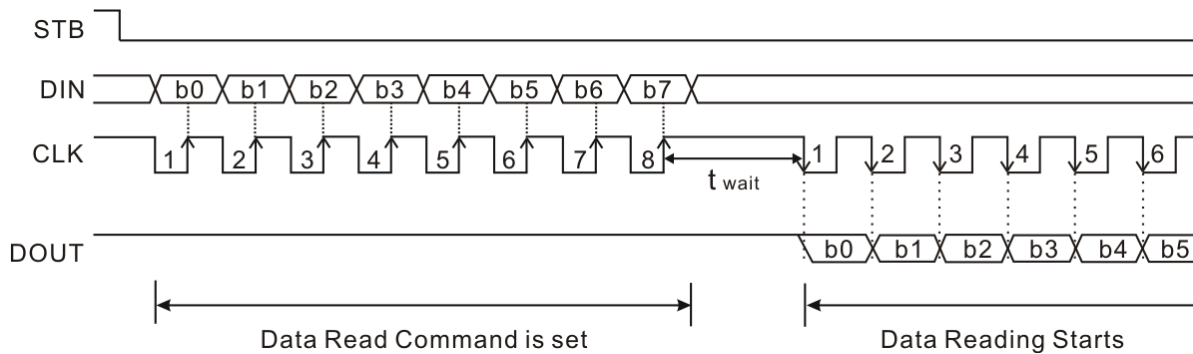
SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6963 serial communication format. The DOUT Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1 KΩ to 10 KΩ) must be connected to DOUT.

RECEPTION (DATA/COMMAND WRITE)



TRANSMISSION (DATA READ)

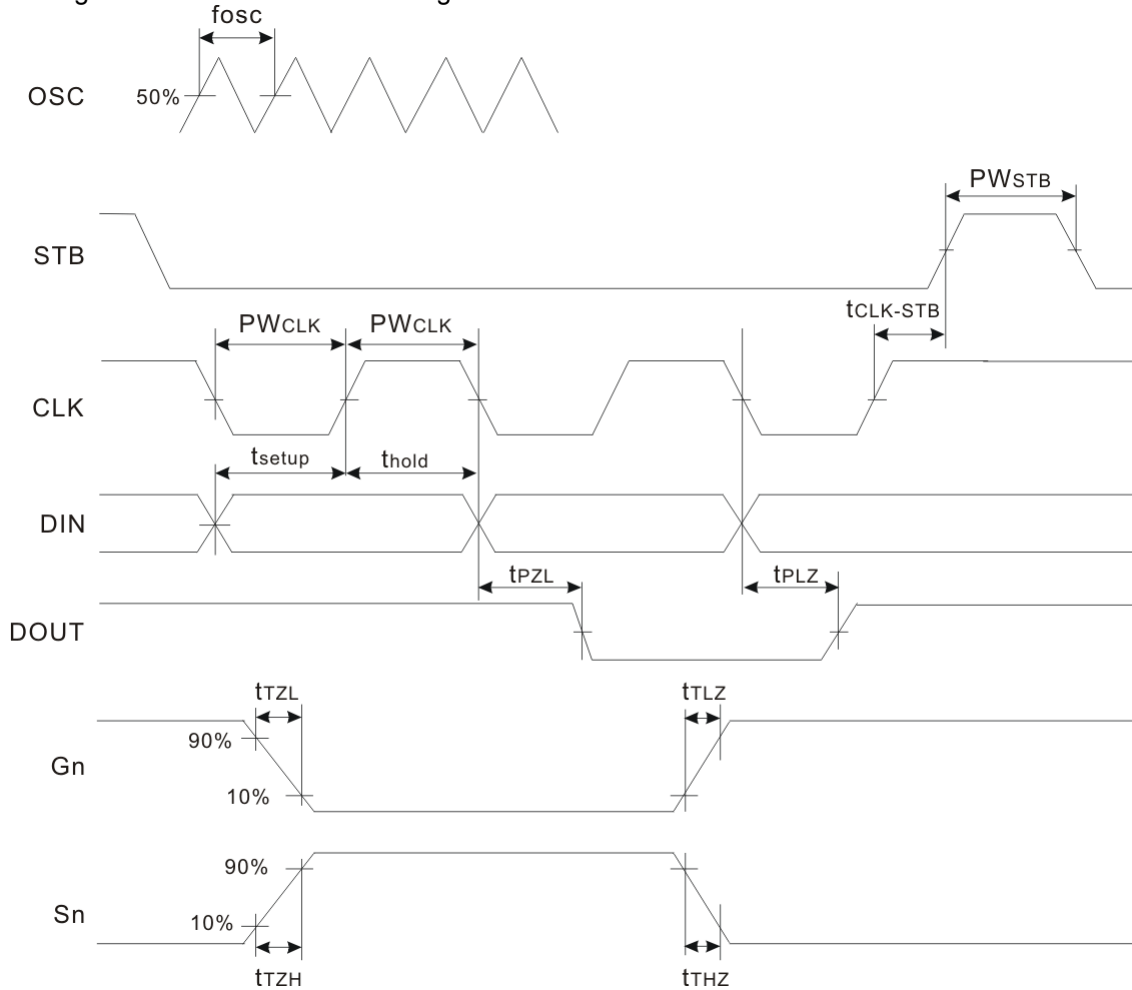


where: t_{wait} (waiting time) $\geq 1\mu s$

It must be noted that when the data is read, the waiting time (t_{wait}) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to $1\mu s$.

SWITCHING CHARACTERISTIC WAVEFORM

PT6963 Switching Characteristics Waveform is given below.



where:

PW_{CLK} (Clock Pulse Width) $\geq 400ns$

t_{setup} (Data Setup Time) $\geq 100ns$

$t_{CLK-STB}$ (Clock - Strobe Time) $\geq 1\mu s$

t_{TZH} (Rise Time) $\leq 1\mu s$

f_{osc} = Oscillation Frequency

$t_{TZL} \leq 1\mu s$

PW_{STB} (Strobe Pulse Width) $\geq 1\mu s$

t_{hold} (Data Hold Time) $\geq 100ns$

t_{THZ} (Fall Time) $\leq 10\mu s$

t_{PZL} (Propagation Delay Time) $\leq 100ns$

t_{PLZ} (Propagation Delay Time) $\leq 300ns$

$t_{TLZ} \leq 10\mu s$

Note:

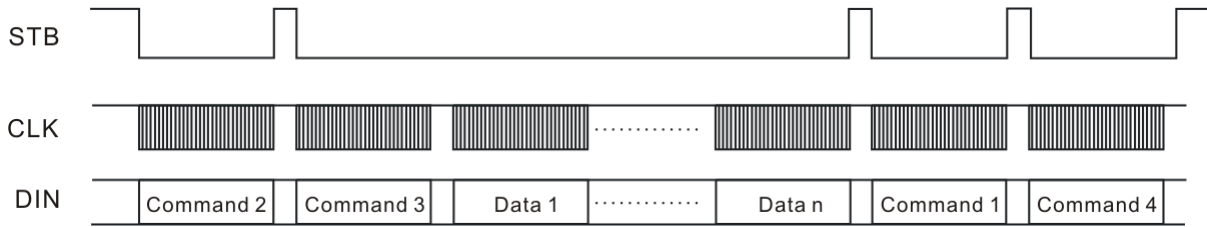
Test Condition Under

t_{THZ} (Pull low resistor) = 10K Ω , Loading capacitor = 300pF

t_{TLZ} (Pull high resistor) = 10K Ω , Loading capacitor = 300pF

APPLICATIONS

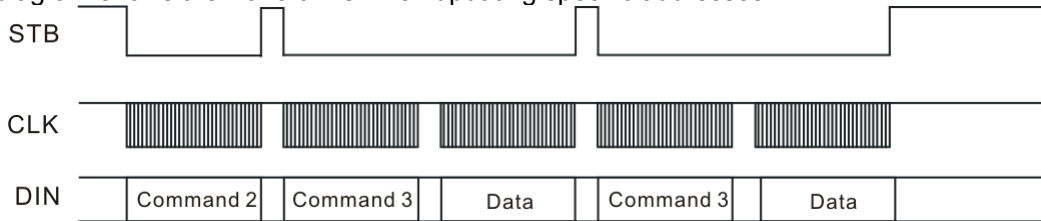
Display memory is updated by incrementing addresses. Please refer to the following diagram.



where:

- Command 1: Display mode setting command
- Command 2: Data setting command
- Command 3: Address setting command
- Data 1 to n: Transfer display data (14 bytes max.)
- Command 4: Display control command

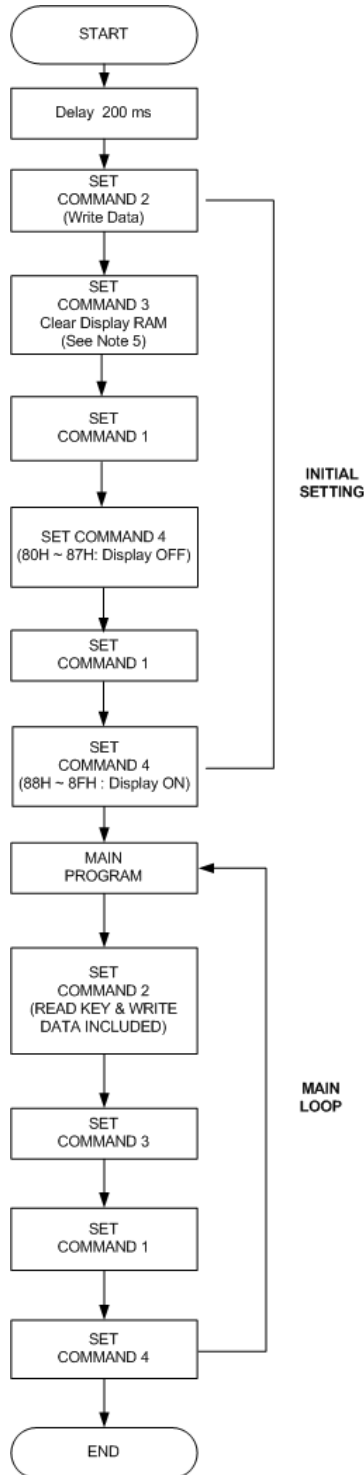
The following diagram shows the waveforms when updating specific addresses.



where:

- Command 2: Data setting command
- Command 3: Address setting command
- Data: Display data

RECOMMENDED SOFTWARE FLOWCHART

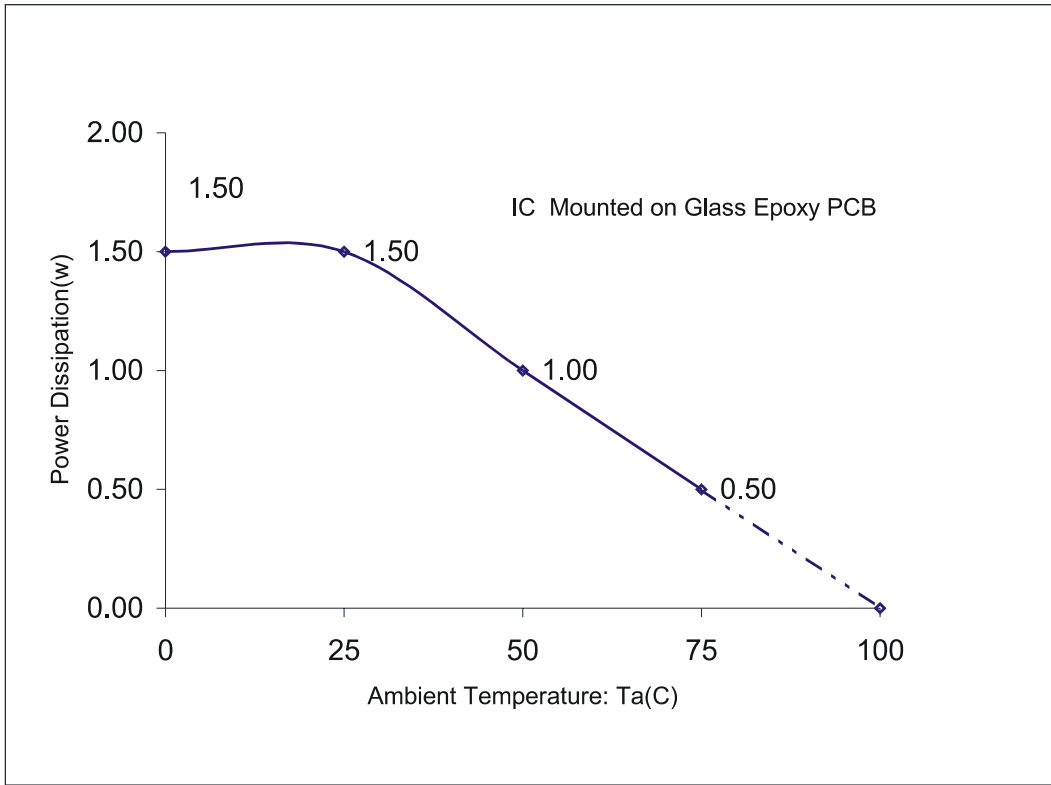


Notes:

1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM be cleared during the initial setting.

SOP 32 (300MIL) THERMAL PERFORMANCE IN STILL AIR

JUNCTION TEMPERATURE: 100°C



ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25°C, GND=0V)

Parameter	Symbol	Ratings	Unit
Supply Voltage	VDD	-0.3 to +7	V
Logic Input Voltage	VI	-0.3 to VDD+0.3	V
Driver Output Current	IOLGR	+250	mA
	IOHSG	-50	mA
Maximum Driver Output Current/Total	ITOTAL	400	mA
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-65 ~ +150	°C

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Topr=-40~+85°C, GND=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	VDD	4.5	5	5.5	V
Dynamic Current (Note 1)	IDDdyn	-	-	5	mA
High-Level Input Voltage	VIH	2.4	-	3.3V/VDD (Note 2)	V
Low-Level Input Voltage	VIL	0	-	1	V

Notes:

1. Test Condition: Set Display Control Commands = 80H (Display Turn OFF State & under no load).
2. The maximum value of VIH (High-Level Input Voltage) depends on user's MCU supply voltage. Which means the maximum value of VIH is 3.3V (VDD) when user's MCU supply voltage is 3.3V(VDD).

ELECTRICAL CHARACTERISTICS

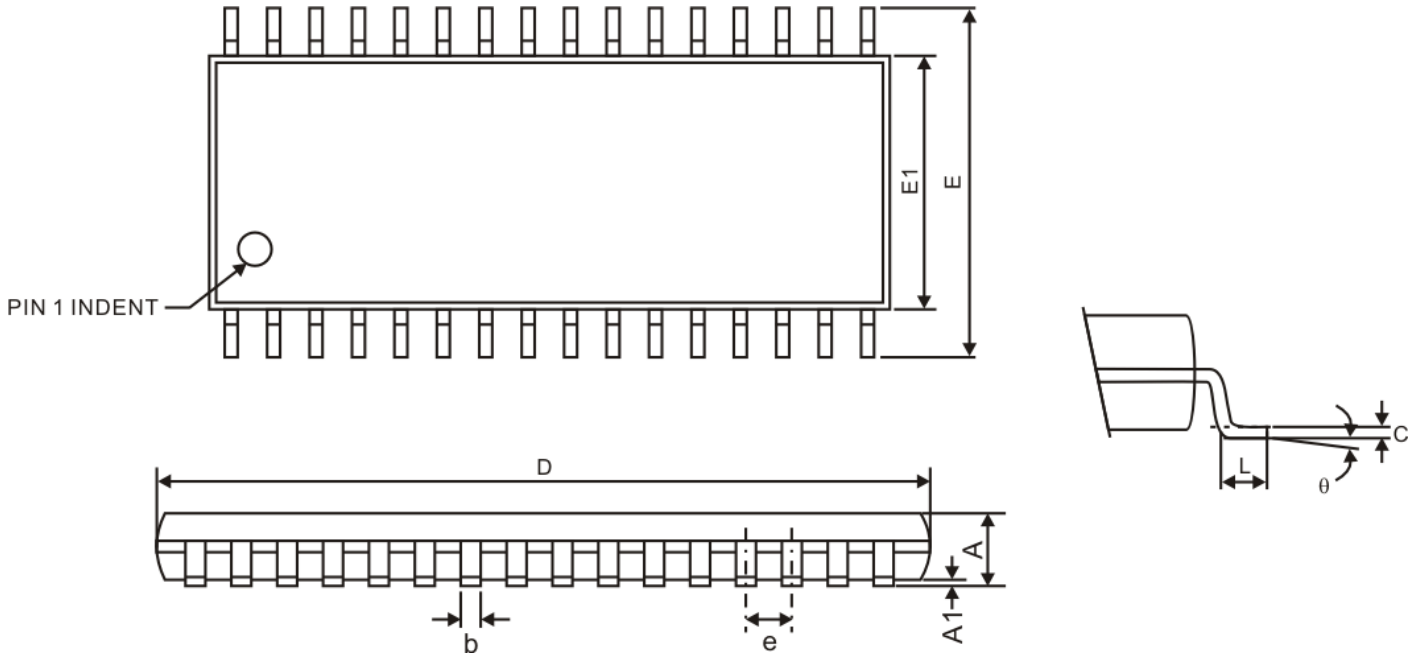
(Unless otherwise stated, VDD=5V, GND=0V, Ta=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Current	IOHSG(1)	VO=VDD-2V SG1 to SG11, SG12/GR7 to SG14/GR5	-20	-25	-40	mA
	IOHSG(2)	VO=VDD-3V SG1 to SG11, SG12/GR7 to SG14/GR5	-25	-30	-50	mA
Low-Level Output Current	IOLGR	VO=0.3V GR1 to GR4, SG12/GR7 to SG14/GR5	100	140	-	mA
Low-Level Output Current	IOLDOUT	VO=0.4V	4	-	-	mA
Segment High-Level Output Current Tolerance	ITOLSG	VO=VDD-3V SG1 to SG11, SG12/GR7 to SG14/GR5	-	-	±5	%
High-Level Input Voltage	VIH	-	2.4	-	3.3 /VDD (note)	V
Low-Level Input Voltage	VIL	-	0	-	1	V
Oscillation Frequency	fosc	R=51KΩ	350	500	650	KHz
K1 to K3 Pull Down Resistor	RKN	K1 to K3 VDD=5V	40	-	100	KΩ

Note: The maximum value of VIH (High-Level Input Voltage) depends on user's MCU supply voltage. Which means the maximum value of VIH is 3.3V (VDD) when user's MCU supply voltage is 3.3V (VDD).

PACKAGE INFORMATION

32 PINS, SOP, 300 MIL



Symbol	Min.	Typ.	Max.
A	-	-	2.65
A1	0.10	-	-
b	0.31	-	0.51
c	0.20	-	0.33
e	1.27 BSC.		
D	20.32	-	20.73
E	7.40	-	7.60
E1	10.00	-	10.65
L	0.38	-	1.27
θ	0		8

- Notes:
1. Refer to JEDEC MO-119 AC
 2. Unit: mm

IMPORTANT NOTICE

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