

## DESCRIPTION

PT6955 is an LED Controller driven on a 1/4 to 1/7 duty factor. Twelve/nine segment output lines, 4 to 7 grid output lines, one display memory, control circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to PT6955 via a three-line serial interface. Housed in a 24-pin SOP, PT6955's pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

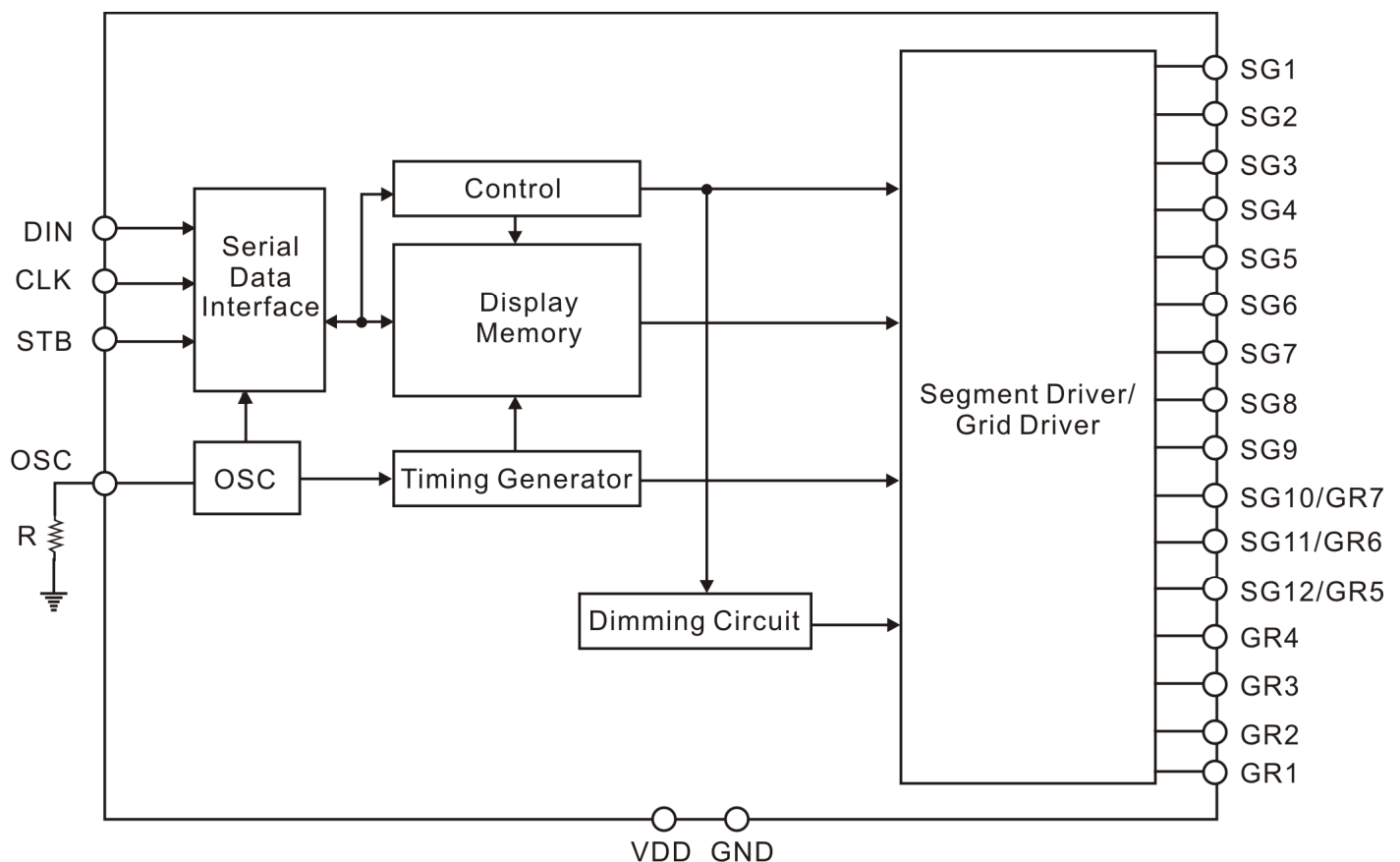
## FEATURES

- CMOS Technology
- Low Power Consumption
- 8-Step Dimming Circuitry
- Serial Interface for Clock, Data Input, Strobe Pins
- Available in 24-pin, SOP

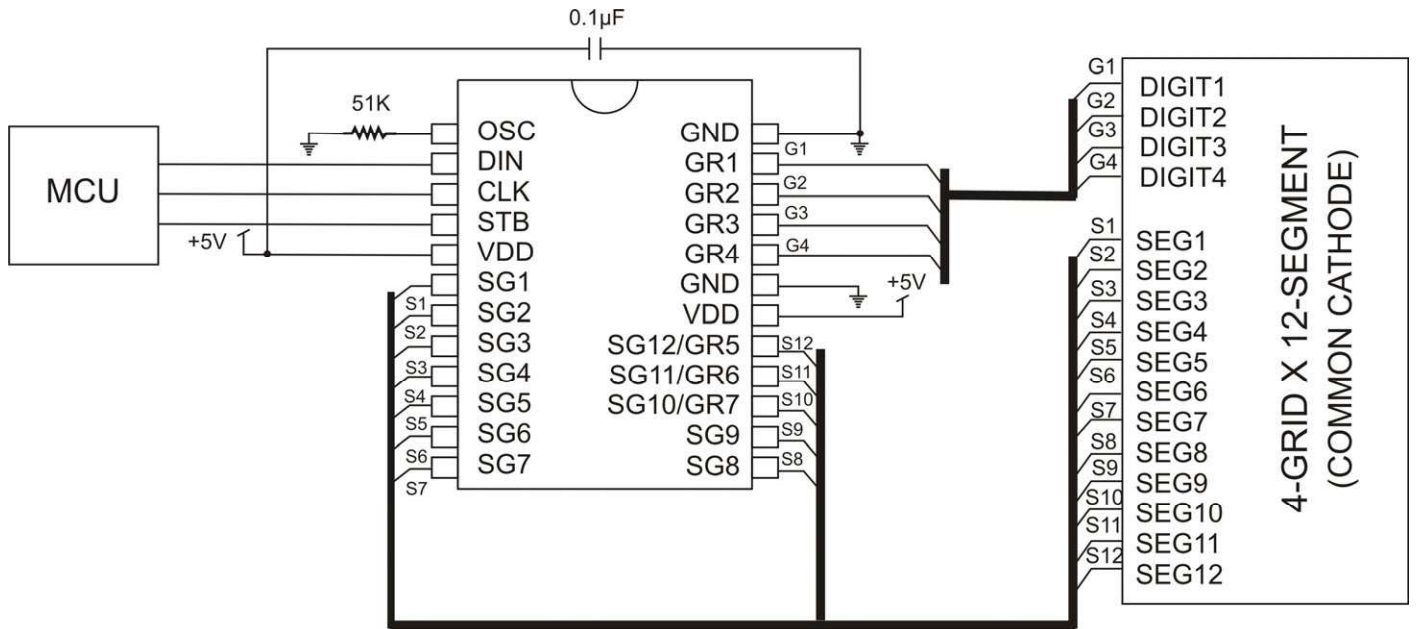
## APPLICATION

- Micro-computer Peripheral Device

## BLOCK DIAGRAM



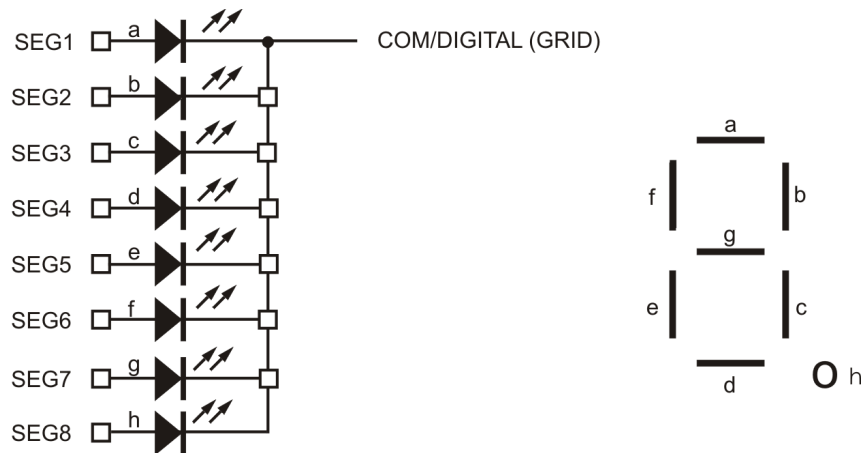
# APPLICATION CIRCUIT



**Notes:**

1. The capacitor (0.1µF) connected between the GND and VDD Pins must be located as near as possible to the PT6955 chip.
2. The PT6955 power supply is separate from the application system power supply.

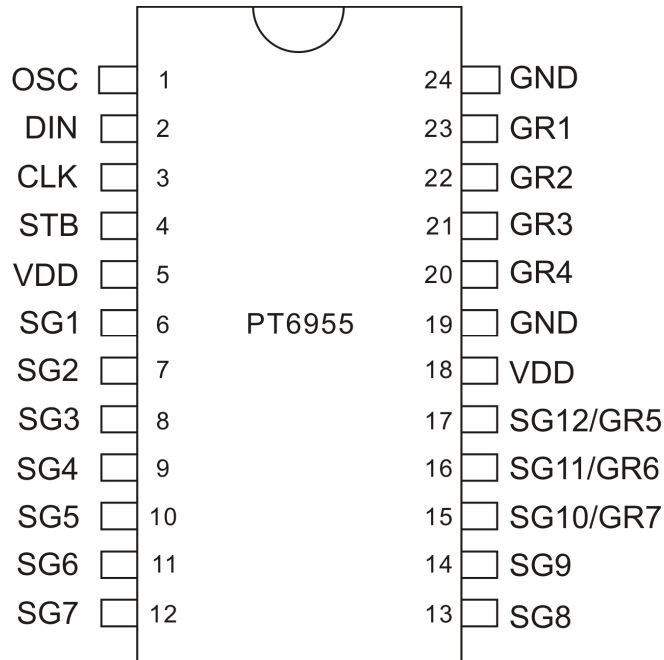
## COMMON CATHODE TYPE LED PANEL



## ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6955	24pins, SOP, 300mil	PT6955

## PIN CONFIGURATION



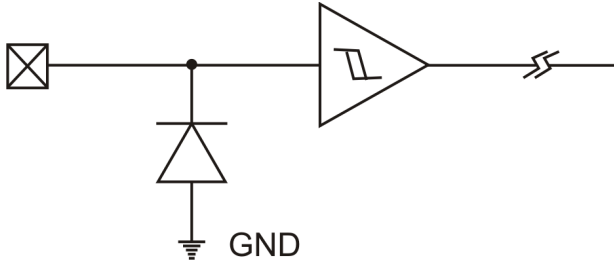
## PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency	1
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	2
CLK	I	Clock Input Pin This pin reads serial data at the rising edge.	3
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is "HIGH", CLK is ignored.	4
VDD	-	Power Supply	5, 18
SG1 ~ SG9	O	Segment Output Pins (p-channel, open drain)	6 ~ 14
SG10/GR7 ~ SG12/GR5	O	Segment Output Pin/Grid Output Pin (CMOS Output)	15 ~ 17
GND	-	Ground Pin	19, 24
GR4 ~ GR1	O	Grid Output Pins (n-channel, open drain)	20 ~ 23

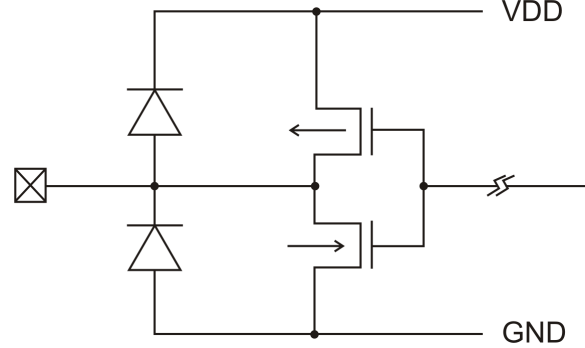
# INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below.

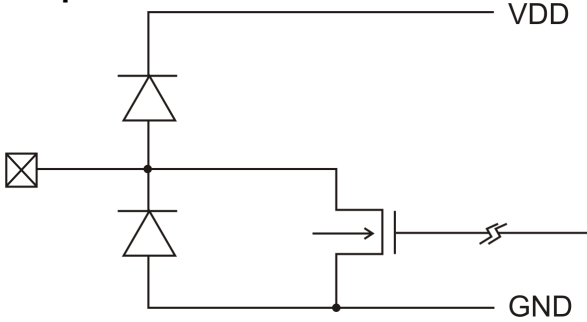
**Input Pins: CLK, STB & DIN**



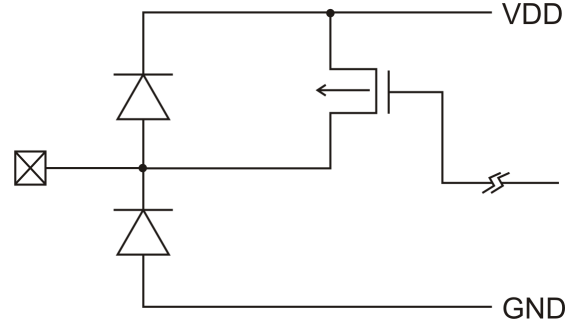
**Output Pins: SG10/GR7, SG11/GR6, SG12/GR5**



**Output Pins: GR1 to GR4**



**Output Pins: SG1 to SG9**

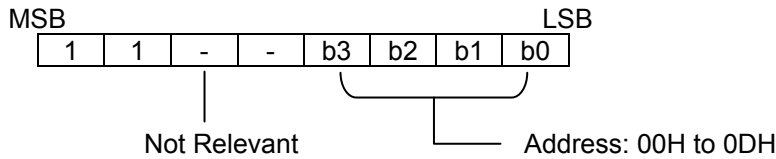




### COMMAND 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of "00H" to "0DH". If the address is set to "0EH" or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at "00H".

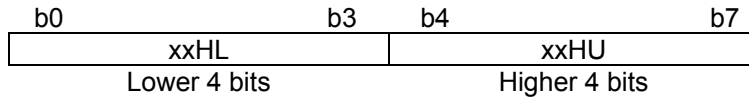
Please refer to the diagram below.



### DISPLAY MODE AND RAM ADDRESS

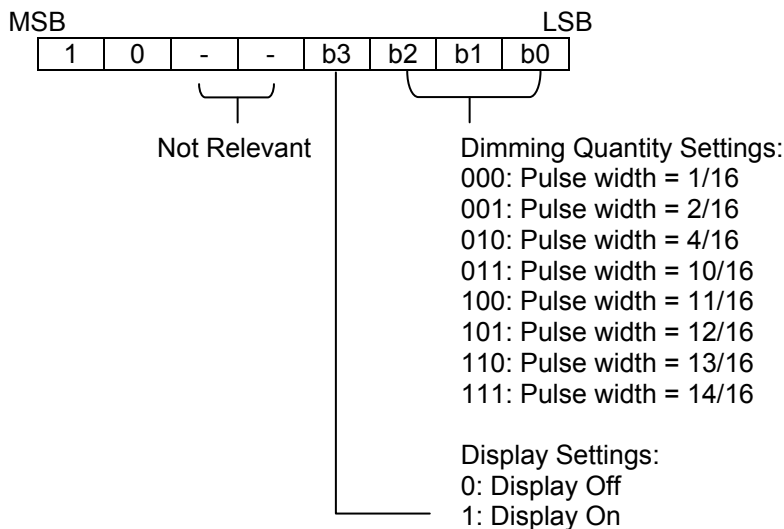
Data transmitted from an external device to PT6955 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6955 are given below in 8 bits unit.

SG1	SG4	SG5	SG8	SG9	SG12	
00HL	00HU	01HL	DIG1			
02HL	02HU	03HL	DIG2			
04HL	04HU	05HL	DIG3			
06HL	06HU	07HL	DIG4			
08HL	08HU	09HL	DIG5			
0AHL	0AHU	0BHL	DIG6			
0CHL	0CHU	0DHL	DIG7			

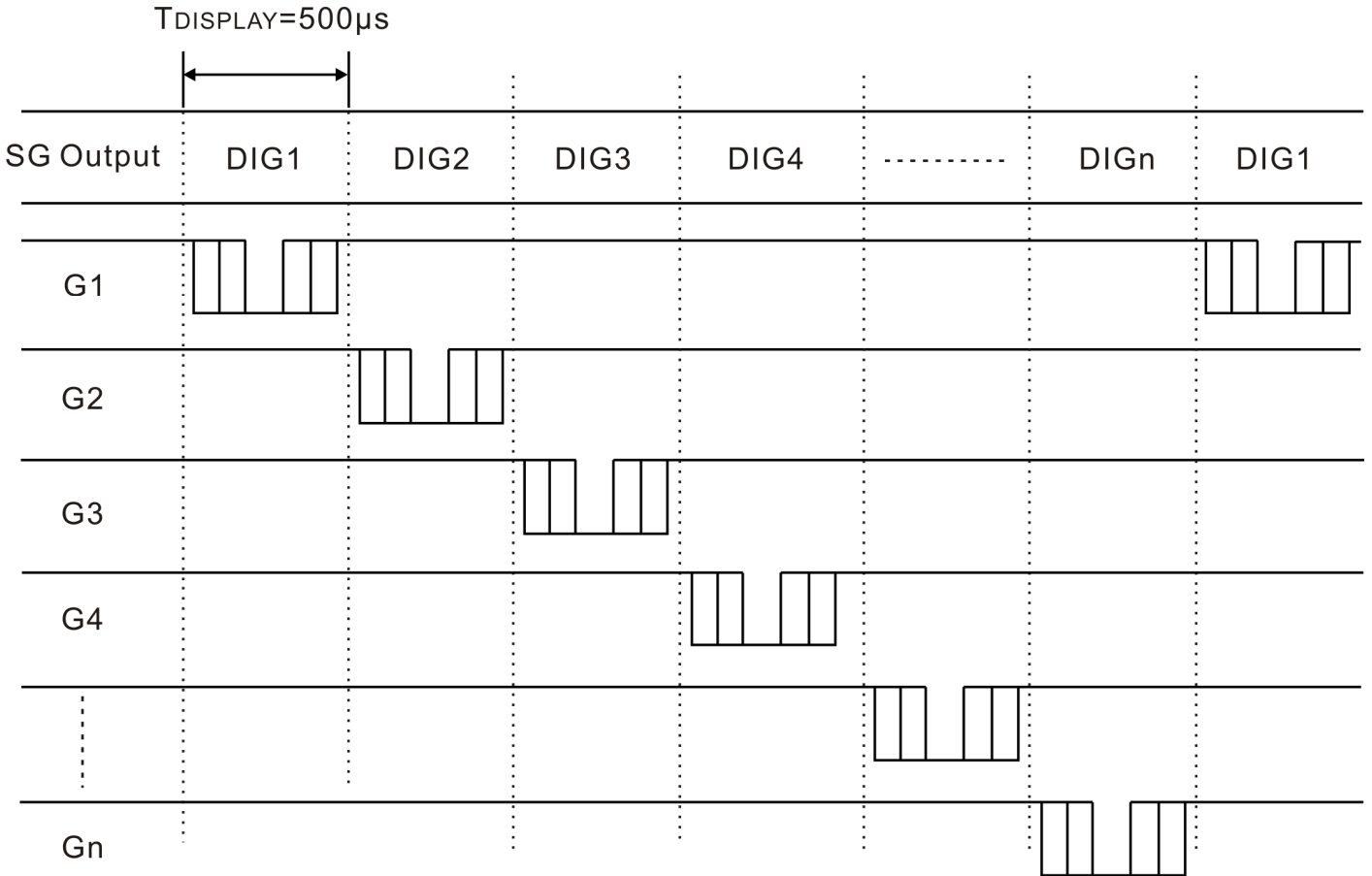


### COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF.



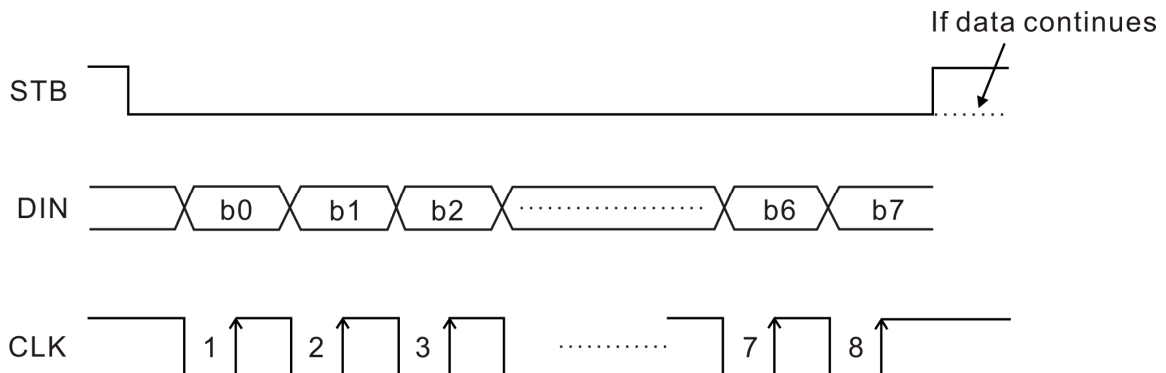
# DISPLAY TIMING WAVEFORM



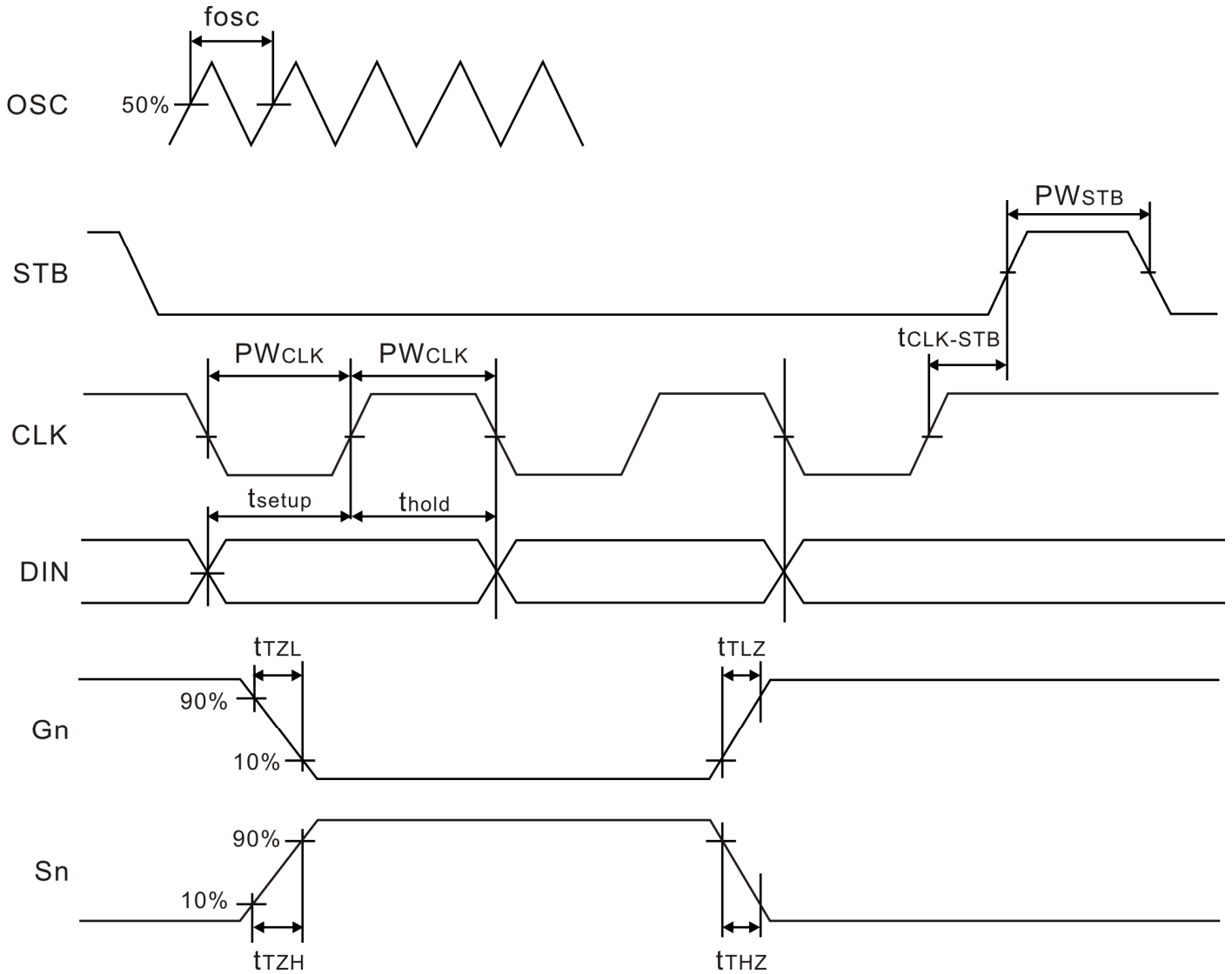
# SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6955 serial communication format.

## RECEPTION (DATA/COMMAND WRITE)



# SWITCHING CHARACTERISTICS WAVEFORM



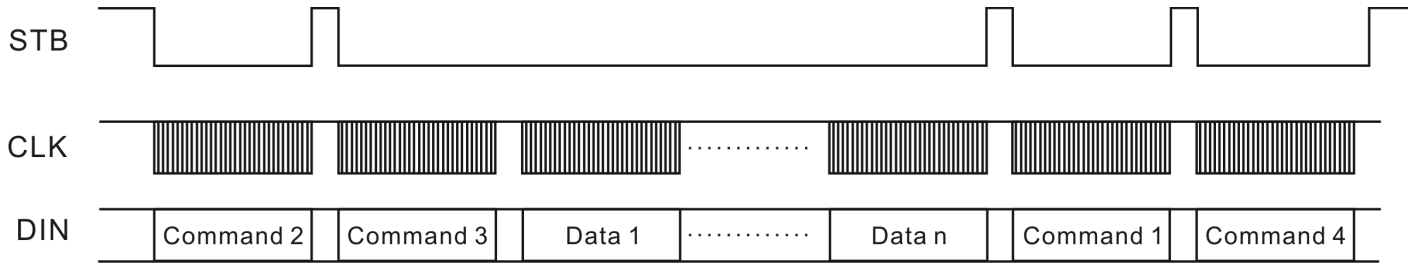
where:

$PW_{CLK}$  (Clock Pulse Width)  $\geq 400ns$   
 $t_{setup}$  (Data Setup Time)  $\geq 100ns$   
 $t_{CLK-STB}$  (Clock - Strobe Time)  $\geq 1\mu s$   
 $t_{TZH}$  (Rise Time)  $\leq 1\mu s$   
 $t_{TLZ}$   $\leq 1\mu s$

$PW_{STB}$  (Strobe Pulse Width)  $\geq 1\mu s$   
 $t_{hold}$  (Data Hold Time)  $\geq 100ns$   
 $t_{THZ}$  (Fall Time)  $\leq 10\mu s$   
 $f_{osc}$  = Oscillation Frequency  
 $t_{TLZ}$   $\leq 10\mu s$

# APPLICATIONS

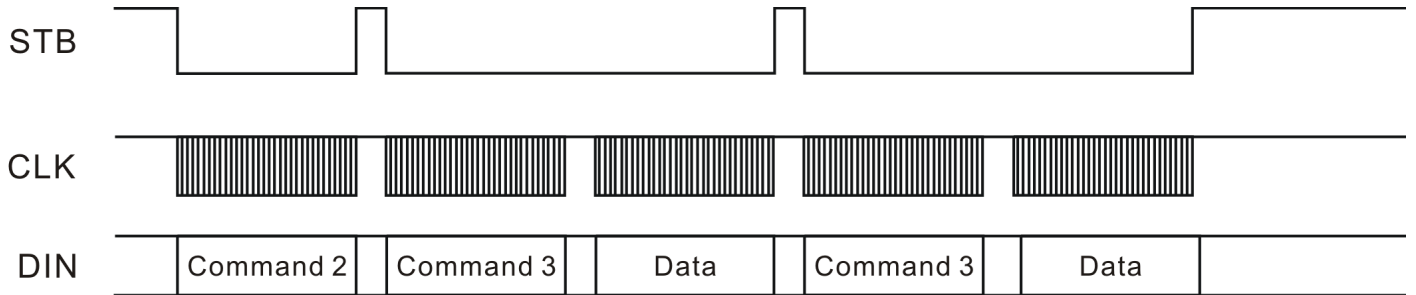
Display memory is updated by incrementing addresses. Please refer to the following diagram.



where:

- Command 1: Display Mode Setting Command
- Command 2: Data Setting Command
- Command 3: Address Setting Command
- Data 1 to n: Transfer Display Data (14 Byte max.)
- Command 4: Display Control Command

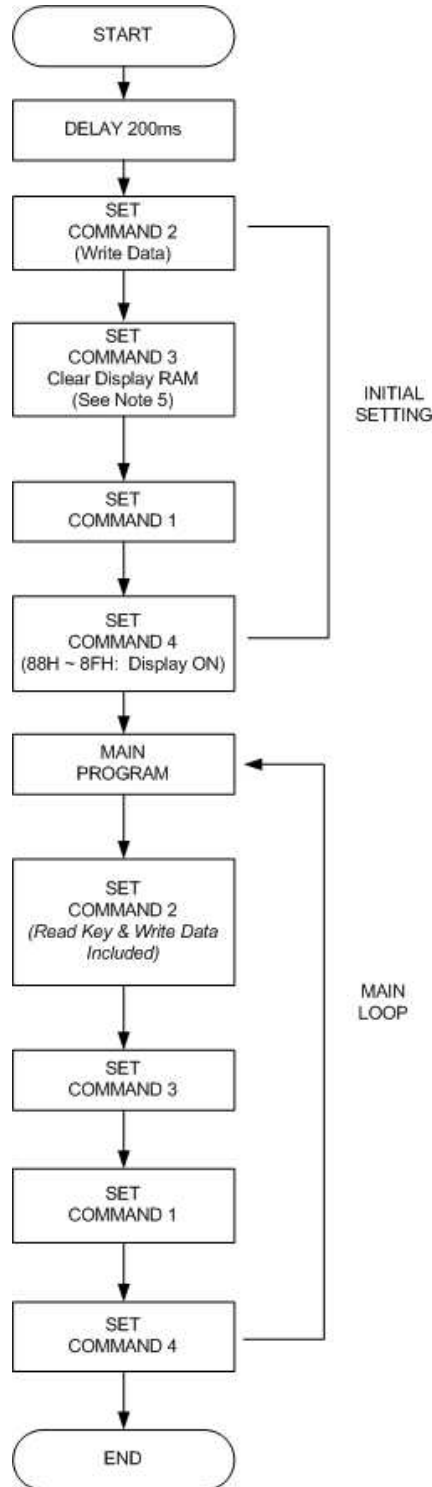
The following diagram shows the waveforms when updating specific addresses.



where:

- Command 2: Data Setting Command
- Command 3: Address Setting Command
- Data: Display Data

# RECOMMENDED SOFTWARE FLOWCHART

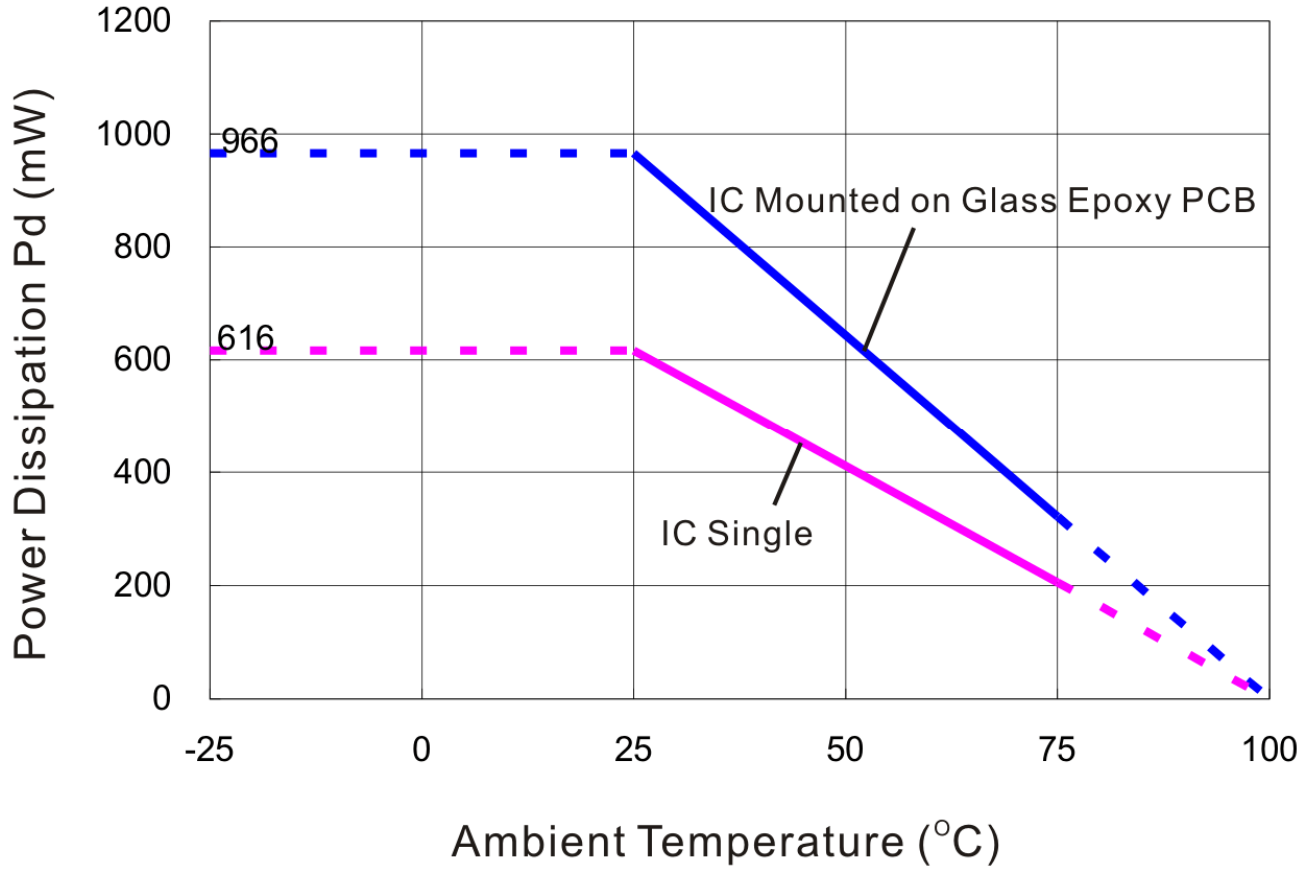


Notes:

1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

# SOP 24L (300MIL) THERMAL PERFORMANCE IN STILL AIR

JUNCTION TEMPERATURE: 100°C



## ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25°C, GND=0V)

Parameter	Symbol	Rating	Units
Supply Voltage	VDD	-0.3 to +7.0	V
Logic Input Voltage	VI	-0.3 to VDD+0.3	V
Driver Output Current/Pin	IOLGR	+250	mA
	IOHSG	-50	mA
Maximum Driver Output Current/Total	ITOTAL	400	mA
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-40 ~ +150	°C

## RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Topr=-40 to +85°C, GND=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	VDD	4.5	5	5.5	V
Dynamic Current (see note)	IDDdyn	-	-	5	mA
High-Level Input Voltage	VIH	0.8VDD	-	VDD	V
Low-Level Input Voltage	VIL	0	-	0.3VDD	V

Note: Test Condition: Set Display Control Commands=80H (Display Turn Off State)

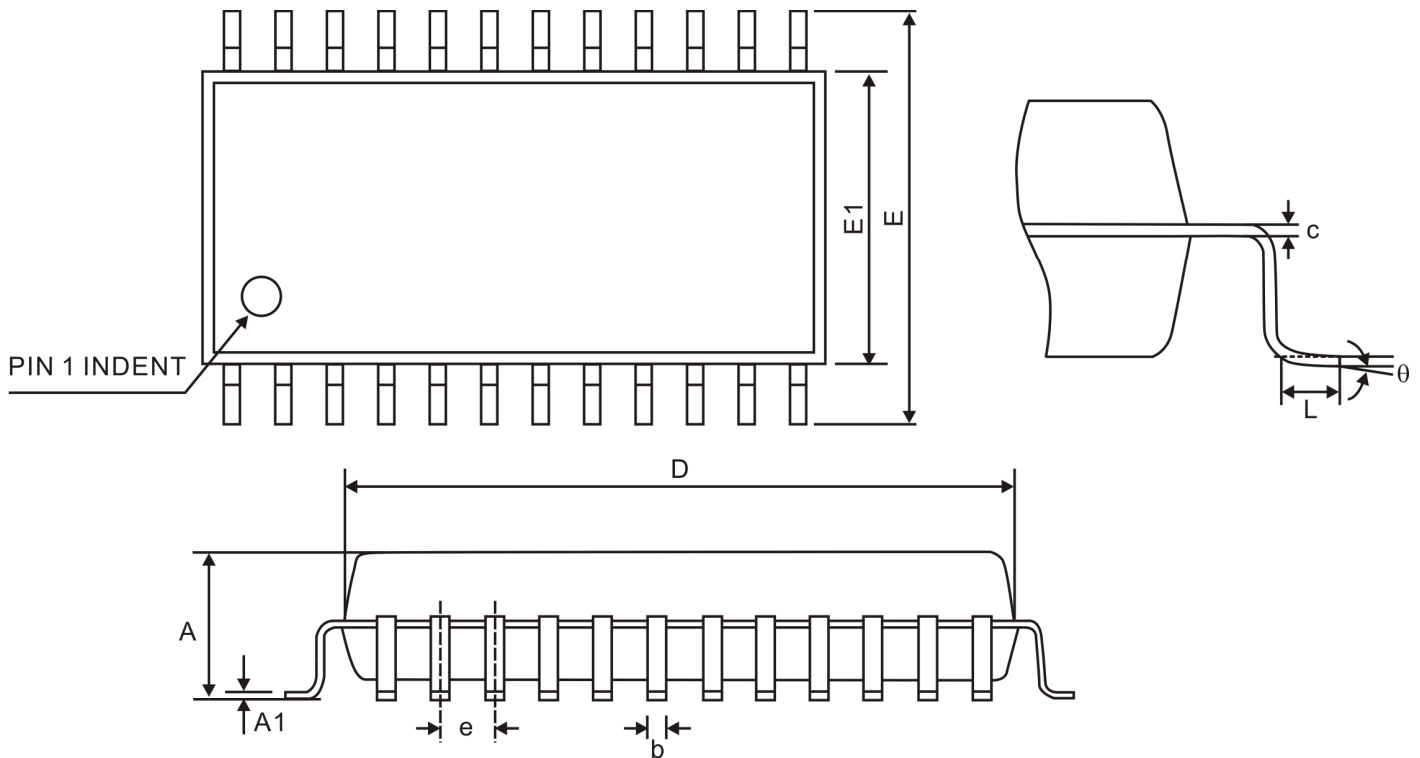
## ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, Ta=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Current	IOHSG(1)	VO=VDD-1V SG1 to SG9, SG10/GR7 to SG12/GR5	-10	-14	-30	mA
	IOHSG(2)	VO=VDD-2V SG1 to SG9, SG10/GR7 to SG12/GR5	-20	-25	-50	mA
Low-Level Output Current	IOLGR	VO=0.3V GR1 to GR4, SG10/GR7 to SG12/GR5	100	140	-	mA
Segment High-Level Output Current Tolerance	ITOLSG	VO=VDD-1V SG1 to SG9, SG10/GR7 to SG12/GR5	-	-	±5	%
High-Level Input Voltage	VIH	-	0.8VDD	-	-	V
Low-Level Input Voltage	VIL	-	-	-	0.3VDD	V
Oscillation Frequency	fosc	R=51KΩ	350	500	650	KHz

# PACKAGE INFORMATION

## 24-PIN, SOP, 300MIL



Symbol	Min.	Nom.	Max.
A	2.35	-	2.65
A1	0.10	-	0.30
b	0.33	-	0.51
c	0.23	-	0.32
D	15.20	-	15.60
E	10.00	-	10.65
E1	7.40	-	7.60
e	1.27 BSC.		
L	0.40	-	1.27
$\theta$	0°	-	8°

- Notes:
1. All controlling dimensions are in millimeters.
  2. Refer to JEDEC MS-013 AD.

**IMPORTANT NOTICE**

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