DESCRIPTION

PT6554 is a high performance Liquid Crystal Display (LCD) Driver IC utilizing CMOS technology specially designed with Key Input function. It can drive up to a maximum of 164 segments and control up to 4 general purpose output ports. It includes a Key Scan Circuit that can support up to 30 key inputs and provides On-Chip Voltage Detection Type Reset Circuit which prevents incorrect display. Display Data can be directly displayed without using any decoder. PT6554 also supports both 1/4 duty-1/2 bias and 1/4 duty-1/3 bias drive techniques. Pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

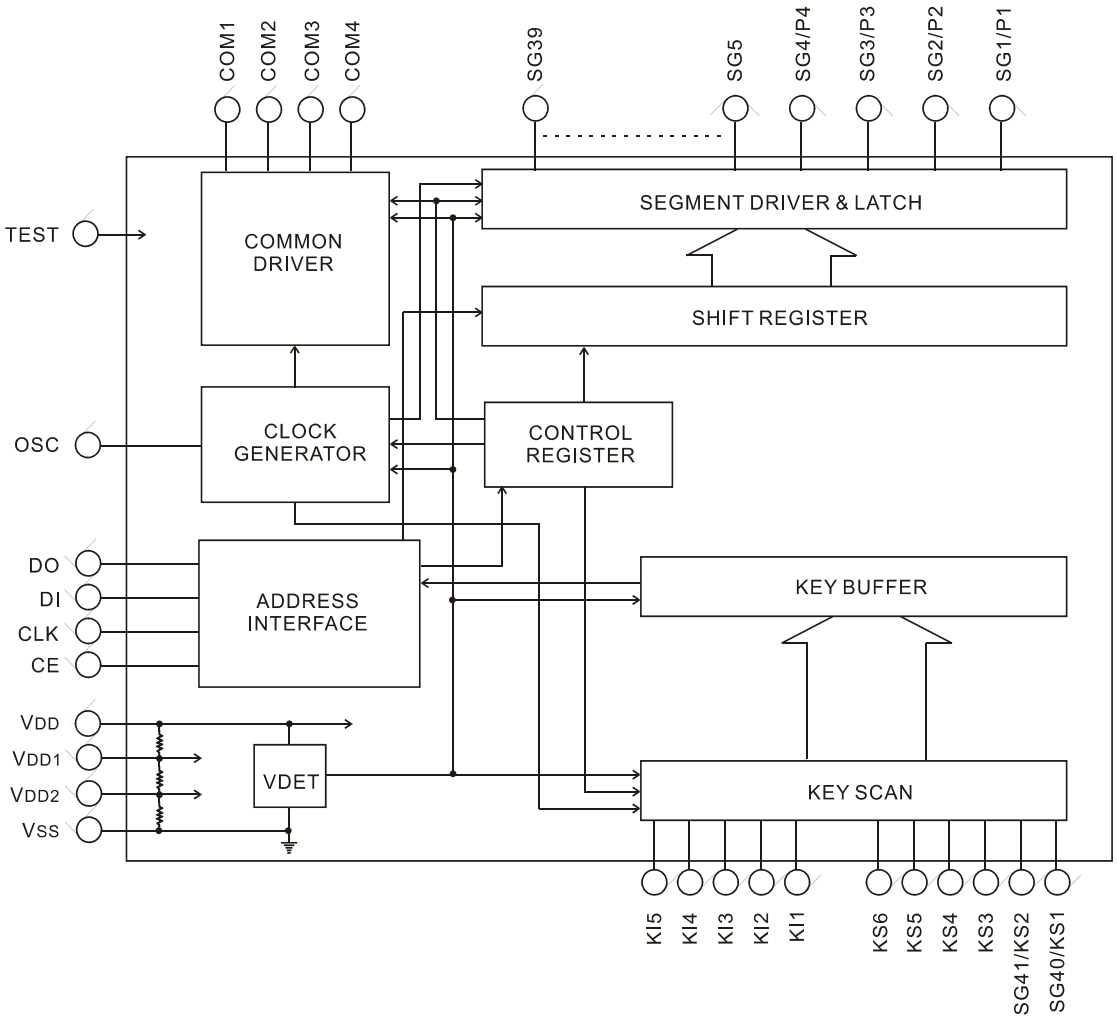
FEATURES

- CMOS technology
- Up to 164 segment drivers (4 Com x 41 Seg)
- Up to 4 general purpose output ports
- Key input function
- 1/4 duty-1/2 bias and 1/4 duty-1/3 bias drive techniques
- Sleep mode & all segment OFF function
- On-Chip voltage detection type reset circuit
- RC oscillation circuit
- Available in 64 pins, QFP or LQFP package

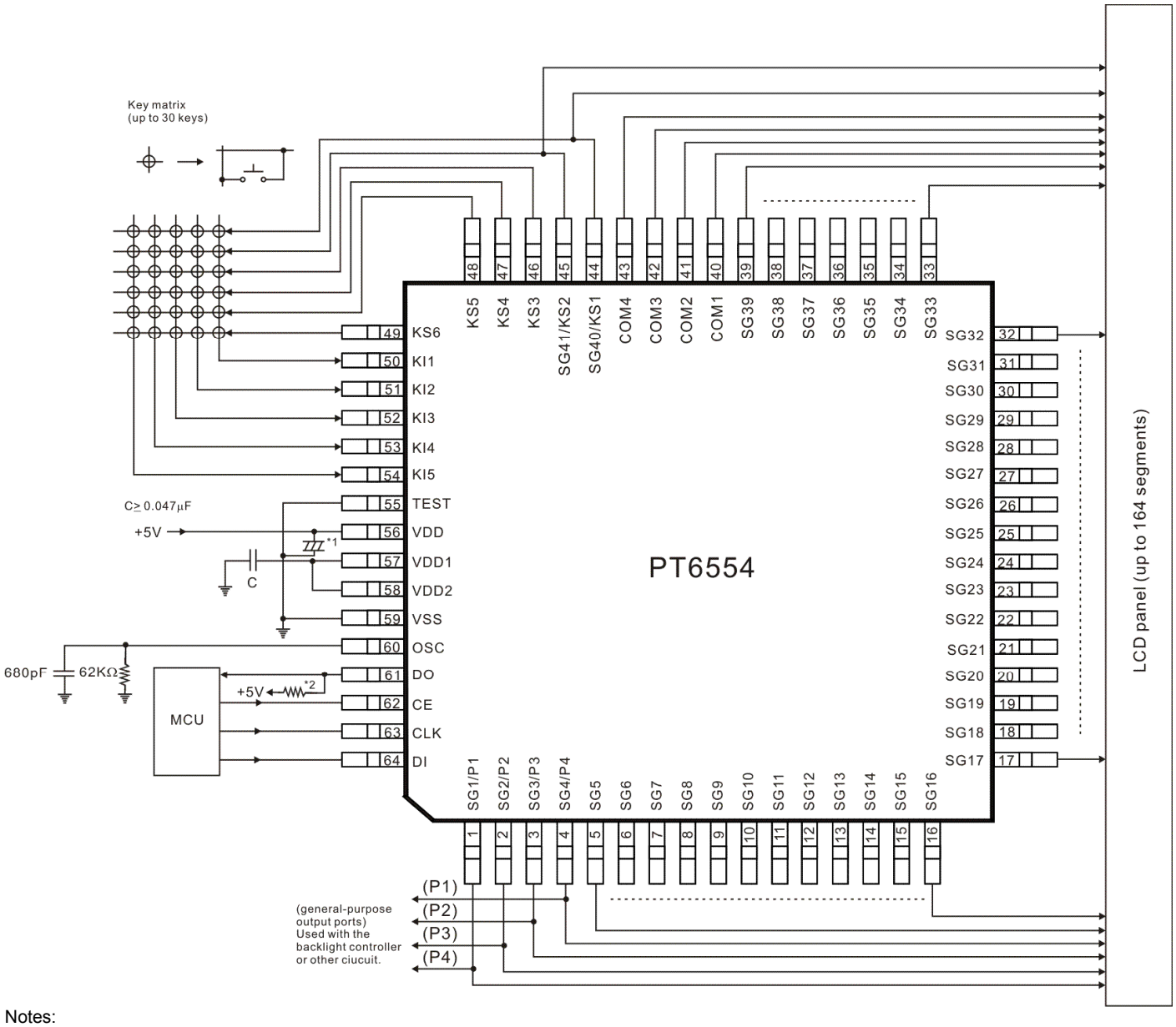
APPLICATION

- Electronic equipment with LCD display

BLOCK DIAGRAM

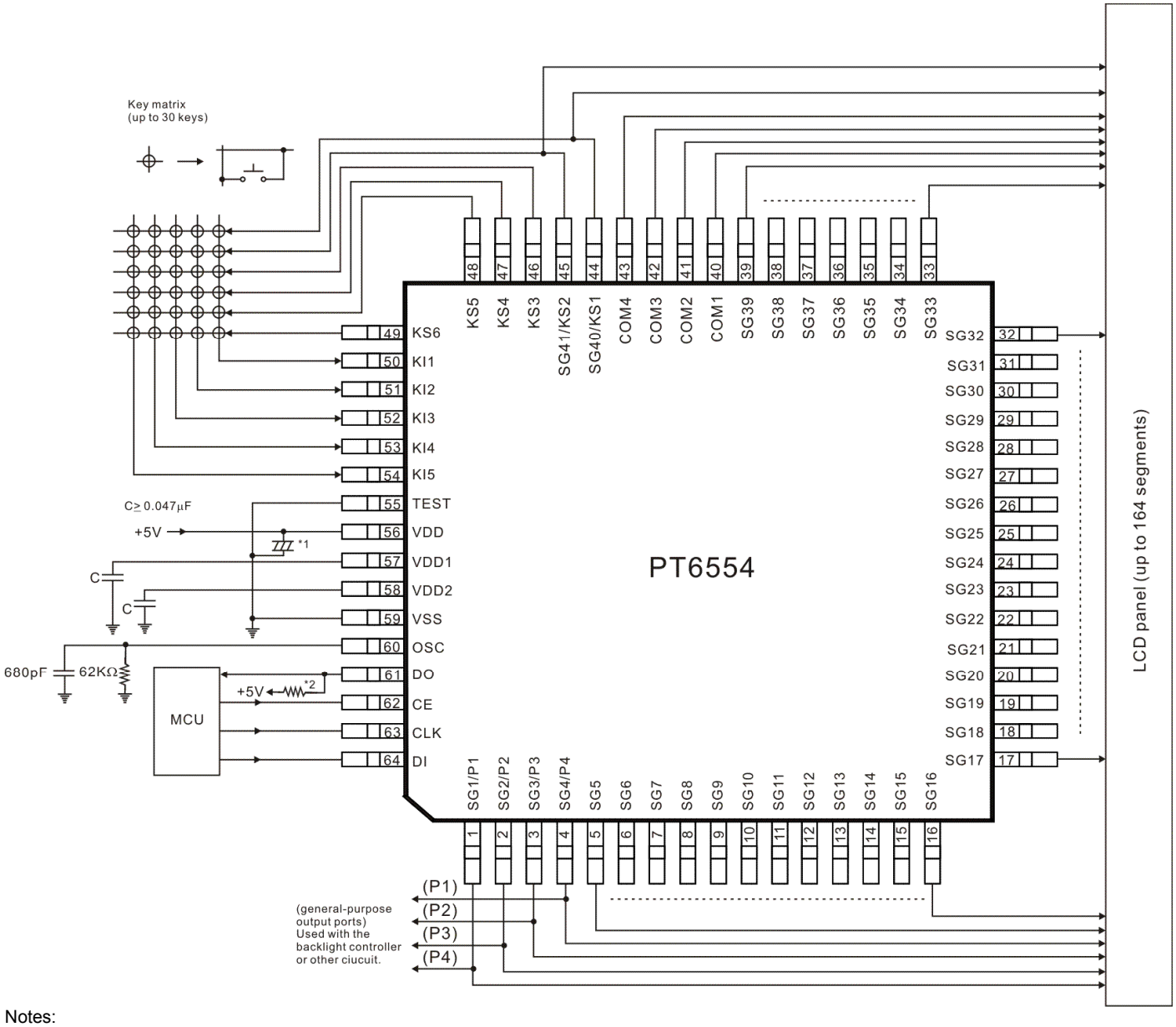


APPLICATION CIRCUITS



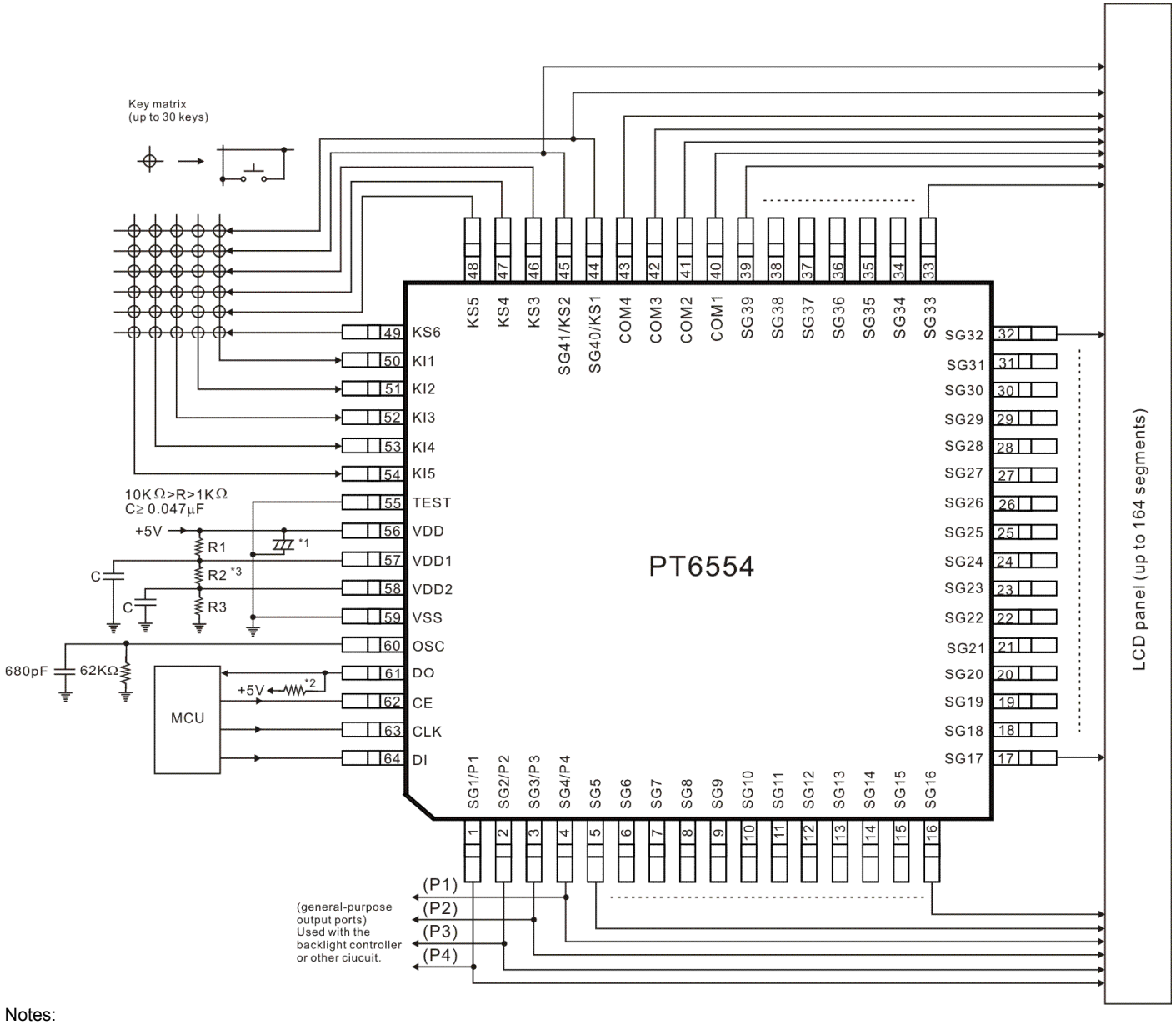
Notes:

1. A capacitor must be added to the power line so that both the power supply voltage (VDD) rise time when power is applied and the power supply voltage (VDD) fall time when power drops are at least 1ms.
2. DO is an open – drain output and requires a pull-high resistor between 1KΩ to 10KΩ. The pull-up resistor value must be appropriate to the capacitor of the external wiring so that the signal wave forms are not degraded.



Notes:

1. A capacitor must be added to the power line so that both the power supply voltage (VDD) rise time when power is applied and the power supply voltage (VDD) fall time when power drops are at least 1ms.
2. DO is an open – drain output and requires a pull-high resistor between 1KΩ to 10KΩ. The pull-up resistor value must be appropriate to the capacitor of the external wiring so that the signal wave forms are not degraded.



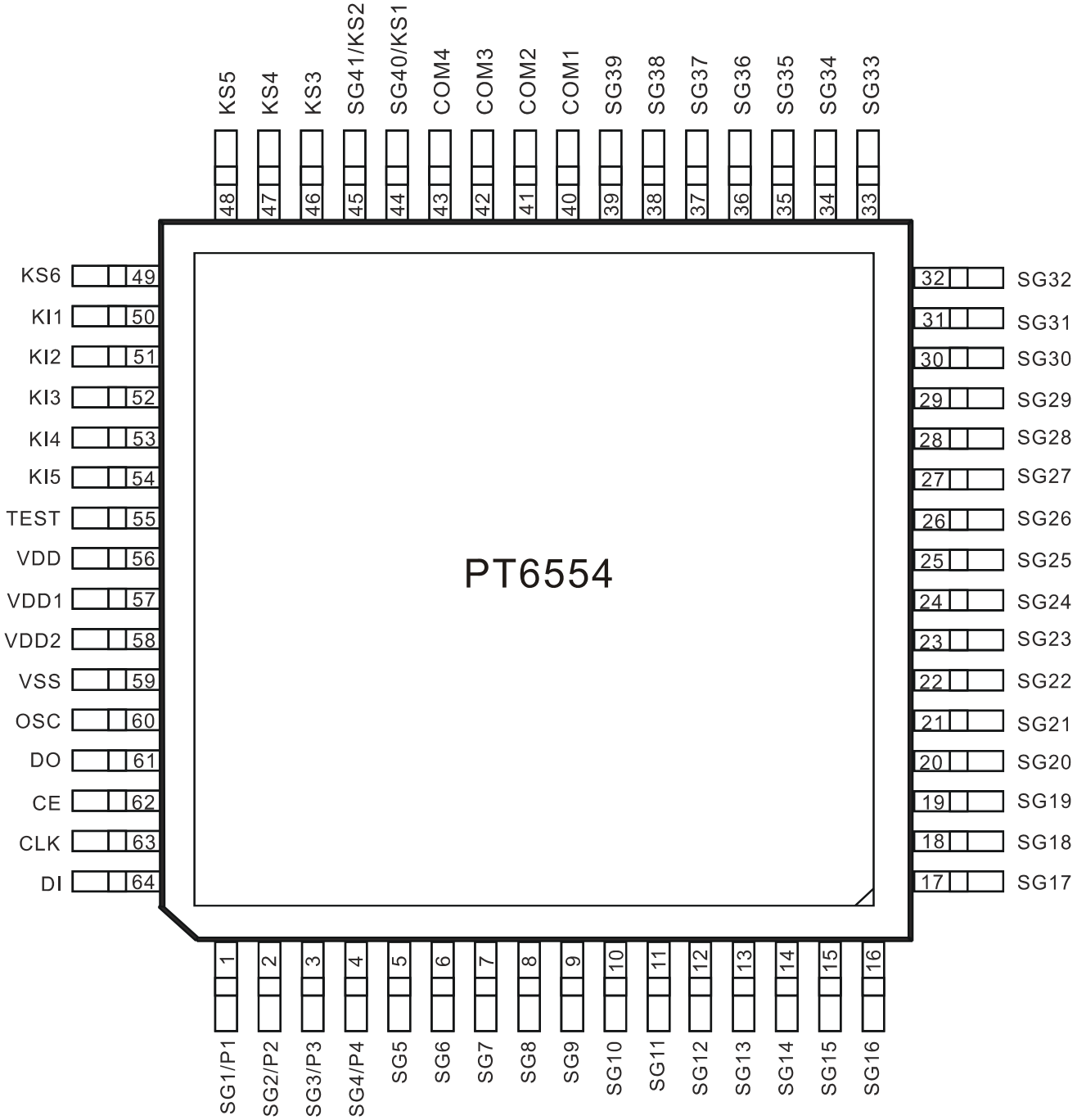
Notes:

1. A capacitor must be added to the power line so that both the power supply voltage (VDD) rise time when power is applied and the power supply voltage (VDD) fall time when power drops are at least 1ms.
2. DO is an open-drain output and requires a pull-high resistor between 1KΩ to 10KΩ. The pull-up resistor value must be appropriate to the capacitor of the external writing so that the signal wave forms are not degraded.
3. R1=R2=R3, the resistance value must be decide by the LCD panel size.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6554	64-Pin, QFP	PT6554
PT6554LQ	64-Pin, LQFP	PT6554LQ

PIN CONFIGURATION



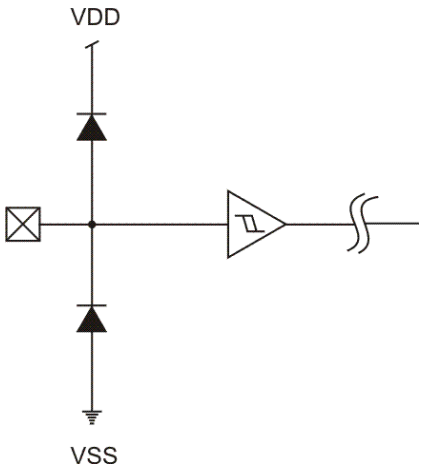
PIN DESCRIPTION

Pin	Pin No.	Function	Active	I/O	Handling when unused
SG1/P1 to SG4/P4 SG5 to SG39	1 to 4 5 to 39	Segment outputs for displaying the display data transferred by serial data input. The SG1/P1 to SG4/P4 pins can be used as general-purpose output ports under serial data control.	-	O	Open
COM1 COM2 COM3 COM4	40 41 42 43	Common driver outputs The frame frequency f_O is given by: f_O=(fosc/512)Hz	-	O	Open
KS1/SG40, KS2/SG41, KS3 to KS6	44 45 46 to 49	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to from a key matrix. The KS1/SG40 and KS2/SG41 pins can be used as segment outputs when so specified by the control data	-	O	Open
KI1to KI5	50 to 54	Key scan inputs. These pins have built-in pull-down resistors.	H	I	GND
OSC	60	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor at this pin.	-	I/O	VDD
CE CLK DI	62 63 64	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. CE: Chip enable CLK: Synchronization clock DI: Transfer data DO: Output data	H - -	I I I	GND
DO	61			O	Open
TEST	55	This pin must be connected to ground.	-	I	-
VDD1	57	Used for applying the LCD drive 2/3 bias voltage externally. Must be connected to VDD1 when a 1/2 bias drive scheme is used.	-	I	Open
VDD2	58	Used for applying the LCD drive 1/3 bias voltage externally. Must be connected to VDD1 when a 1/2 bias drive scheme is used.	-	I	Open
VDD	56	Power supply connection. Provide a voltage of between 4.5 and 6.0V	-	-	-
VSS	59	Power supply connection. Connect to ground.	-	-	-

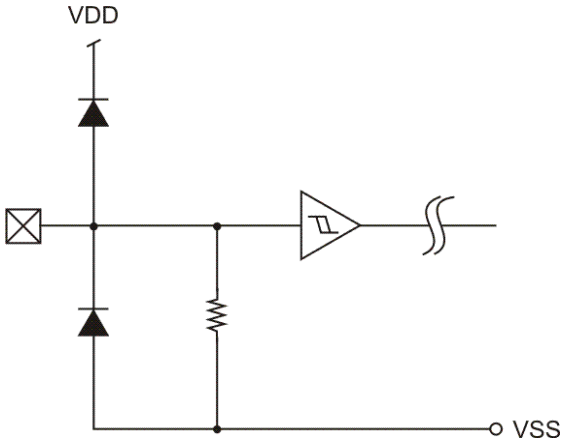
INPUT/OUPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below:

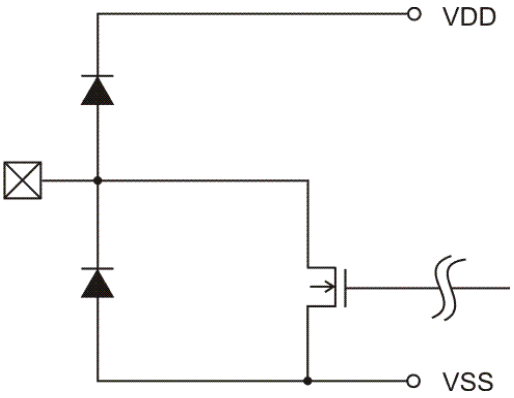
INPUT PIN: CLK, CE, DI



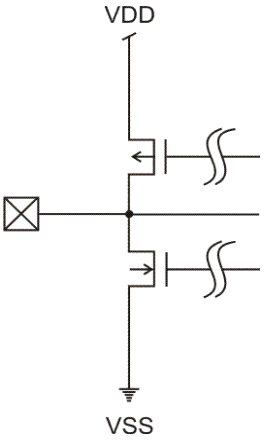
INPUT PIN: KI1 TO KI5



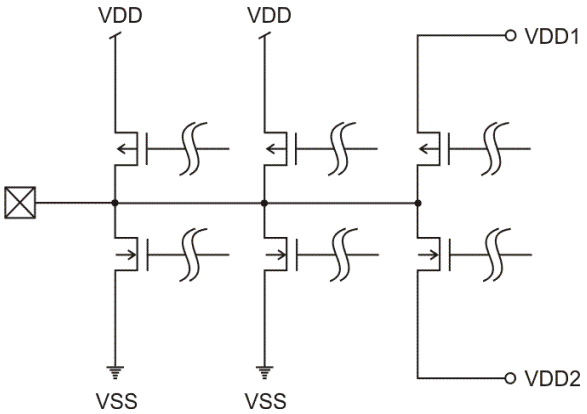
OUTPUT PIN: DO



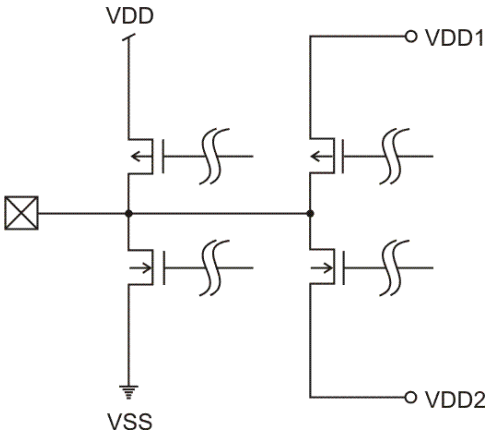
OUTPUT PIN: KS3 TO KS6



OUTPUT PIN: SG1/P1 TO SG4/P4, SG5 TO SG39, S40/KS1, S41/KS2



OUTPUT PIN: COM1 TO COM4



FUNCTION DESCRIPTION

CONTROL DATA BITS

SLEEP CONTROL BITS: S0, S1

S0 and S1 are control bits used to select either the Normal or Sleep Mode as well as set the state of the key scan output pins, namely: KS1 to KS6 during the key scan stand-by. Please refer to the table below.

Control data		Mode	OSC controller	Segment outputs Common outputs	Output pin states during key scan stand-by					
S0	S1				KS1	KS2	KS3	KS4	KS5	KS6
0	0	Normal	Operating	Operating	H	H	H	H	H	H
0	1	Sleep	Stopped	L	L	L	L	L	L	H
1	0	Sleep	Stopped	L	L	L	L	L	H	H
1	1	Sleep	Stopped	L	H	H	H	H	H	H

Note: This table is under the assumption that the pins – SG40/KS1 and SG41/KS2 are used as Key Scan Output Pins.

KEY SCAN OUTPUT / SEGMENT DRIVER OUTPUT SELECT BIT: K0, K1

K0 and K1 are control bits used to select the function of the pins – SG40/KS1 and SG41/KS2.
These pins (SG40/KS1 and SG41/KS2) may either be used as Key Scan Output Pins or Segment Driver Output Pins. Please refer to the following table.

Control data		Output pin state		Maximum number of input keys
K0	K1	SG40/KS1	SG41/KS2	
0	0	KS1	KS2	30
0	1	SG40	KS2	25
1	X	SG40	SG41	20

Note: x = Not Relevant

SEGMENT DRIVER OUTPUT / GENERAL PURPOSE OUTPUT PORT SELECT BIT: P0, P1

P0 and P1 are control bits used to select the function of the pins – SG1/P1 to SG4/P4. These pins (SG1/P1 to SG4/P4) may be used either as Segment Driver Output Pins or General Purpose Output Ports. Please refer to the table below.

Control data		Output state			
P0	P1	SG1/P1	SG2/P2	SG3/P3	SG4/P4
0	0	SG1	SG2	SG3	SG4
0	1	P1	P2	SG3	SG4
1	0	P1	P2	P3	SG4
1	1	P1	P2	P3	P4

When the output pins (SG1/P1 to SG4/P4) are used as General Output Ports, the correspondence between the display data and these pins are shown in the table below.

Output pin	Corresponding display data
SG1/P1	D1
SG2/P2	D5
SG3/P3	D9
SG4/P4	D13

To further clarify the table above, the following example is given. If the output pin – SG1/P1 is used as a General Output Port, then SG1/P1 Pin will output a “HIGH” Level if the corresponding Display Data,
D1 – is set to “1”. Likewise, if the output pin – SG4/P4 is used as a General Output Port, then the SG4/P4 Pin will output “HIGH” Level, if the corresponding Display Data, D13 – is set to “1”.

SEGMENT ON / OFF CONTROL BIT: SC

SC is the control bit used to control the state (ON or OFF) of the Segment Drivers. Please refer to the table below. It should be noted that turning OFF the Segment by setting SC Bit means that the Segments are turned OFF by outputting segment OFF waveforms from the Segment Driver Output Pins.

SC	Display state
0	On
1	Off

1/2 BIAS OR 1/3 BIAS DRIVE TECHNIQUE SELECT BIT: DR

DR is the control bit used to select either the 1/2 or 1/3 Bias Drive Technique. Please refer to the table below.

DR	Drive scheme
0	1/3 bias drive
1	1/2 bias drive

KEY OUTPUT DATA BITS: KD1 TO KD30

KD1 to KD30 are key data bits of the key matrix formed by the KS1 to KS6 lines and the KI1 to KI5 lines. Please refer to the table below for the correspondence between the output pins – KS1 to KS6, input pins KI1 to KI5 and the Key Data Bits KD1 to KD30.

	KI1	KI2	KI3	KI4	KI5
KS1/SG40	KD1	KD2	KD3	KD4	KD5
KS2/SG41	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

Note: Output Pins – SG40/KS1 and SG41/KS2 are used as Key Scan Output Pins.

As stated earlier, key matrix having up to a maximum of 30 keys may be constructed using the KS1 to KS6 and KI1 to KI5 lines. If any one of the keys is pressed, the corresponding key output data is set to 1. For example, the key data bit, KD23 is set to “1”, when the corresponding key is pressed.

If the output pins, SG40/KS1 and SG41/KS2 are used as Segment Driver Output Pins (by setting the K1 and K0 control bits), a key matrix having up to a maximum of 20 keys may be constructed using the KS3 to KS6 and KI1 to KI5 lines. The key output data bits KD1 to KD10 are set to 0.

SLEEP ACKNOWLEDGE DATA BIT: SA

SA is an output data bit that is used to set the state when the key is pressed. When DO is in “LOW” state and the serial data is inputted, then the mode can be set either to Normal or Sleep Mode during this period. SA will be “1” in sleep mode and “0” in normal mode.

DISPLAY DATA & OUTPUT PIN CORRESPONDENCE

Output	COM1	COM2	COM3	COM4
SG1/P1	D1	D2	D3	D4
SG2/P2	D5	D6	D7	D8
SG3/P3	D9	D10	D11	D12
SG4/P4	D13	D14	D15	D16
SG5	D17	D18	D19	D20
SG6	D21	D22	D23	D24
SG7	D25	D26	D27	D28
SG8	D29	D30	D31	D32
SG9	D33	D34	D35	D36
SG10	D37	D38	D39	D40
SG11	D41	D42	D43	D44
SG12	D45	D46	D47	D48
SG13	D49	D50	D51	D52
SG14	D53	D54	D55	D56
SG15	D57	D58	D59	D60
SG16	D61	D62	D63	D64
SG17	D65	D66	D67	D68
SG18	D69	D70	D71	D72
SG19	D73	D74	D75	D76
SG20	D77	D78	D79	D80

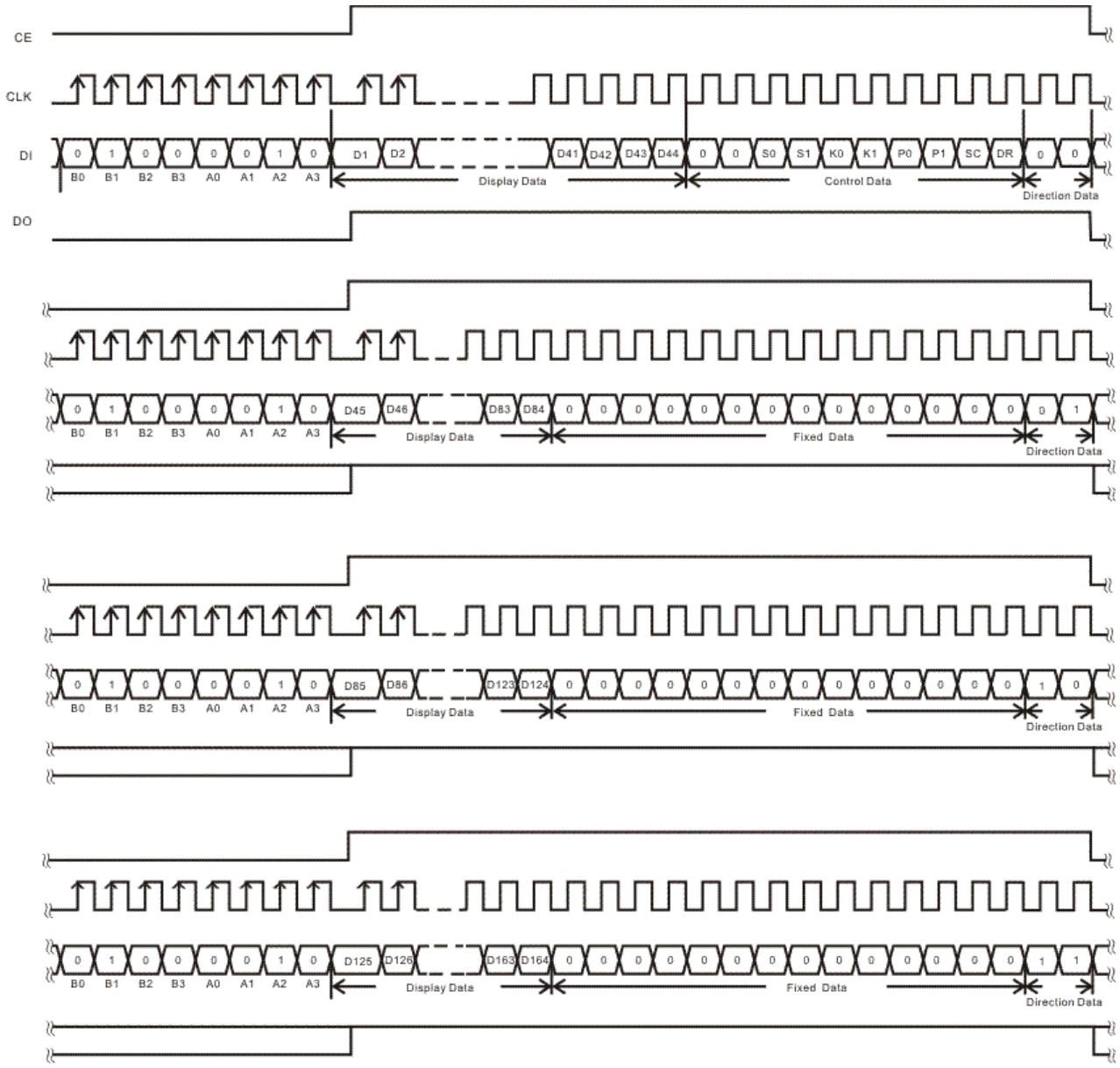
Output pin	COM1	COM2	COM3	COM4
SG21	D81	D82	D83	D84
SG22	D85	D86	D87	D88
SG23	D89	D90	D91	D92
SG24	D93	D94	D95	D96
SG25	D97	D98	D99	D100
SG26	D101	D102	D103	D104
SG27	D105	D106	D107	D108
SG28	D109	D110	D111	D112
SG29	D113	D114	D115	D116
SG30	D117	D118	D119	D120
SG31	D121	D122	D123	D124
SG32	D125	D126	D127	D128
SG33	D129	D130	D131	D132
SG34	D133	D134	D135	D136
SG35	D137	D138	D139	D140
SG36	D141	D142	D143	D144
SG37	D145	D146	D147	D148
SG38	D149	D150	D151	D152
SG39	D153	D154	D155	D156
KS1/SG40	D157	D158	D159	D160
KS2/SG41	D161	D162	D163	D164

To provide further clarity, an example is given in the table below showing the SG11 – Segment Driver Output State and its corresponding Display Data – D41, D42, D43, D44 relationship.

Display data				Output pin state
D41	D42	D43	D44	SG11
0	0	0	0	The LCD segments for COM1, COM2, COM3 and COM4 are off.
0	0	0	1	The LCD segment for COM4 is on.
0	0	1	0	The LCD segment for COM3 is on.
0	0	1	1	The LCD segments for COM3 and COM4 are on.
0	1	0	0	The LCD segment for COM2 is on.
0	1	0	1	The LCD segments for COM2 and COM4 are on.
0	1	1	0	The LCD segments for COM2 and COM3 are on.
0	1	1	1	The LCD segments for COM2, COM3 and COM4 are on.
1	0	0	0	The LCD segment for COM1 is on.
1	0	0	1	The LCD segments for COM1 and COM4 are on.
1	0	1	0	The LCD segments for COM1 and COM3 are on.
1	0	1	1	The LCD segments for COM1, COM3 and COM4 are on.
1	1	0	0	The LCD segments for COM1 and COM2 are on.
1	1	0	1	The LCD segments for COM1, COM2 and COM4 are on.
1	1	1	0	The LCD segments for COM1, COM2 and COM3 are on.
1	1	1	1	The LCD segments for COM1, COM2, COM3 and COM4 are on.

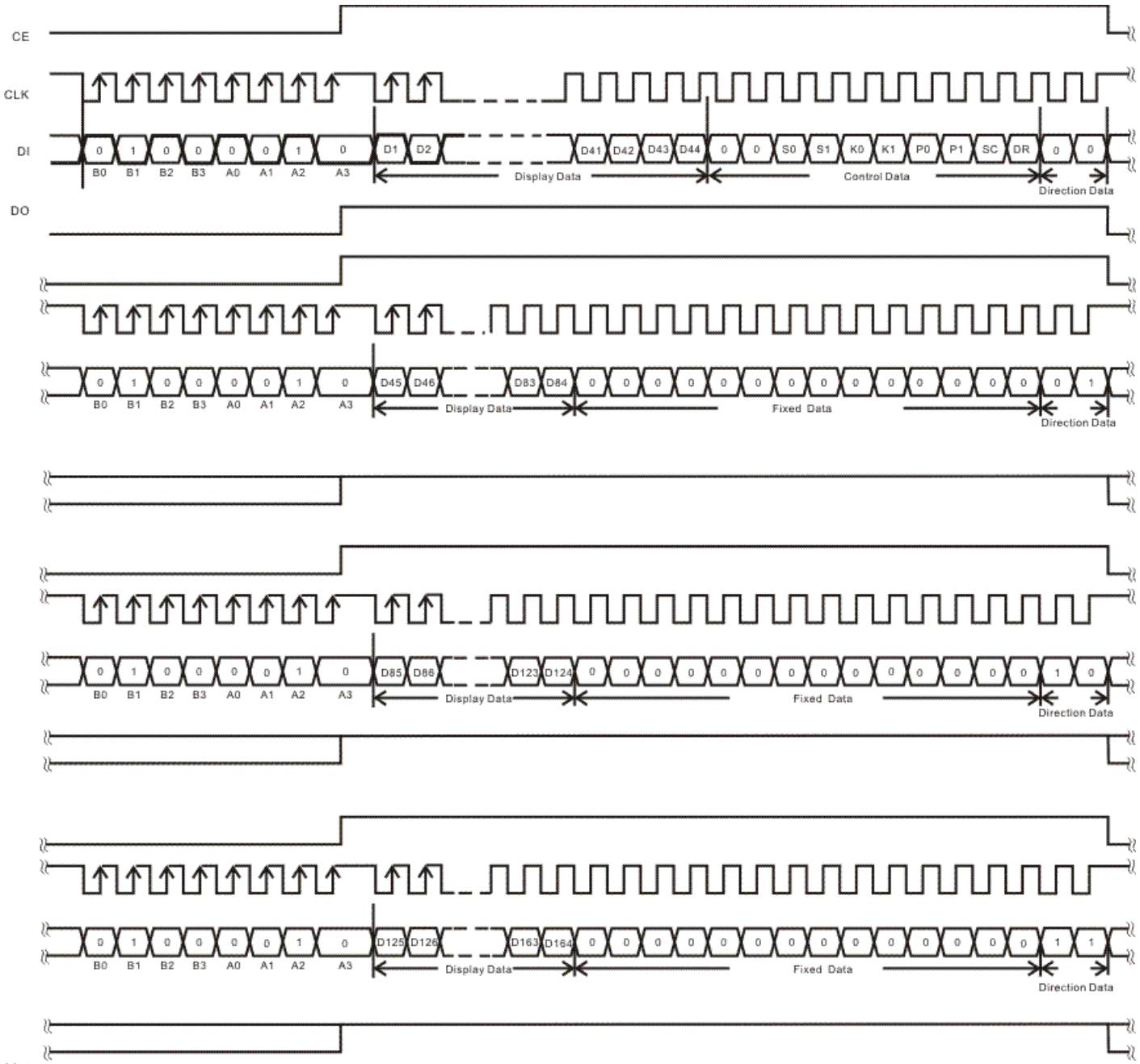
SERIAL DATA INPUT

CASE 1: CLK IS TERMINATED AT "LOW" LEVEL



Notes:
1. Address: 42H
2. Display Data Bits: D1 to D164
3. Sleep Control Data: S0, S1
4. Key Scan Output / Segment Driver Output Select Bits: K0, K1
5. Segment Driver Output / General Purpose Output Port Select Bits: P0, P1
6. Segment ON / OFF Control Bit: SC
7. 1/2 Bias or 1/3 Bias Drive Select Bit: DR

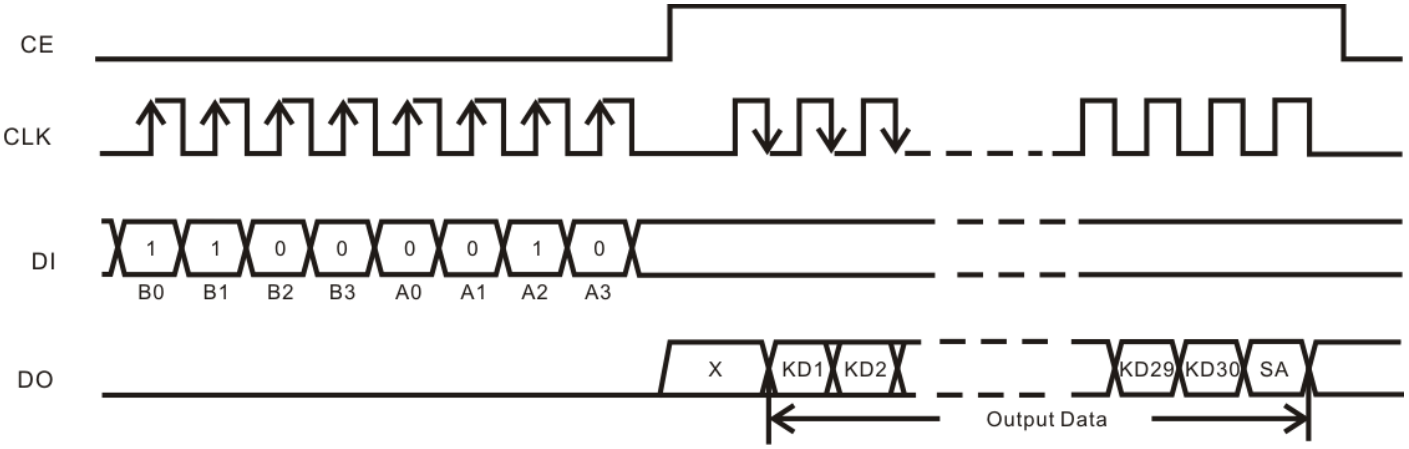
CASE 2: CLK IS TERMINATED AT "HIGH" LEVEL



Notes:
1. Address: 42H
2. Display Data Bits: D1 to D164
3. Sleep Control Data: S0, S1
4. Key Scan Output / Segment Driver Output Select Bits: K0, K1
5. Segment Driver Output / General Purpose Output Port Select Bits: P0, P1
6. Segment ON / OFF Control Bit: SC
7. 1/2 Bias or 1/3 Bias Drive Select Bit: DR

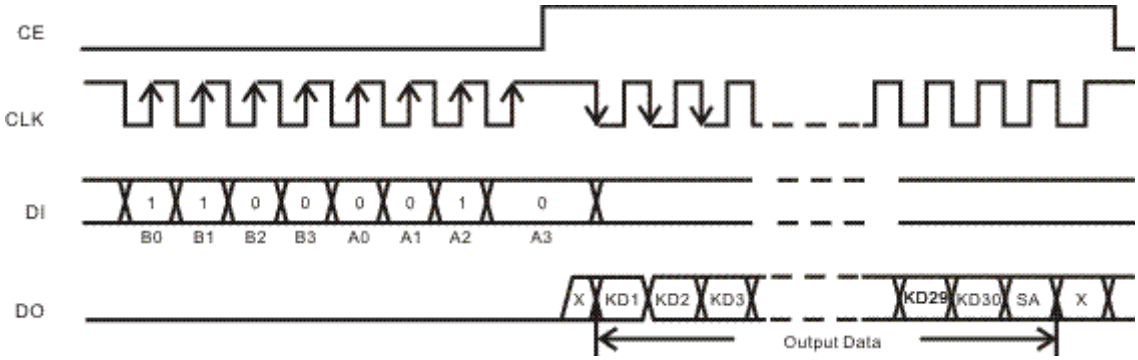
SERIAL DATA OUTPUT

CASE 1: CLK IS TERMINATED AT "LOW" LEVEL



Notes:
1. Address: 43H
2. Key Output Data Bits: KD1 to KD30
3. Sleep Acknowledge Bit: SA
4. If the Key Data Read Operation is executed when DO is in "HIGH" state, then the Read Key Data Bits (KD1 to KD30) and the Sleep Acknowledge Bit (SA) will not be valid.

CASE 2: CLK IS TERMINATED AT "HIGH" LEVEL



Notes:
1. Address: 43H
2. Key Output Data Bits: KD1 to KD30
3. Sleep Acknowledge Bit: SA
4. If the Key Data Read Operation is executed when DO is in "HIGH" state, then the Read Key Data Bits (KD1 to KD30) and the Sleep Acknowledge Bit (SA) will not be valid.

SLEEP MODE

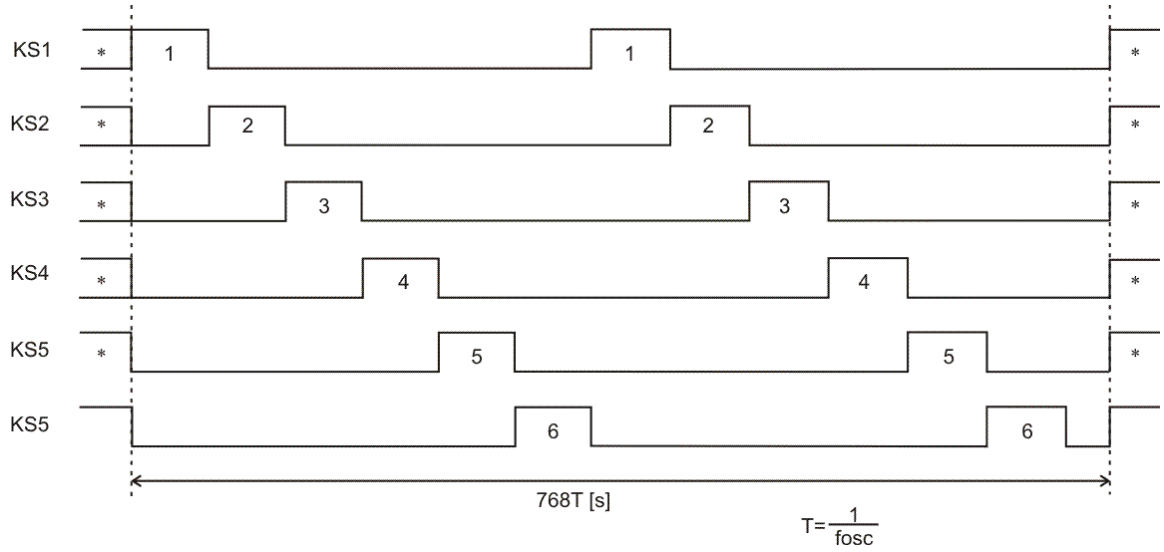
The Sleep Mode is enabled when any one of the Sleep Acknowledge Control Bits – S0 or S1 is set to “1”. Under the Sleep Mode, the all the segment and common driver outputs are set to “LOW” level and the oscillation operation is terminated. Oscillation operation will only commence again if a key is pressed. Please note that this reduces power dissipation. The Sleep Mode is cleared when both control bits – S0 and S1 are set to “0”.

It should be noted, however, that the output pins – SG1/P1 and SG2/P2 might still be used as General Purpose Output Ports by setting the control bits – P0 and P1 even under the Sleep Mode. In other words, the Sleep Mode does not in anyway affect the SG1/P1 and SG2/P2 pins from being used as General Purpose Output Ports.

KEY SCAN OPERATION

KEY SCAN TIMING

PT6554 scans the keys twice (reads the key data twice) and if the key data matches, this key is defined as PRESSED (or ON). A key scan period is equivalent to 384T (s). 800T (s) after the key scan commences, PT6554 outputs a key data read request. If the key data from the does not match and a key was pressed at that point, the keys are scanned again. It must be noted that PT6554 cannot detect a key which is pressed shorter than 800T (s).



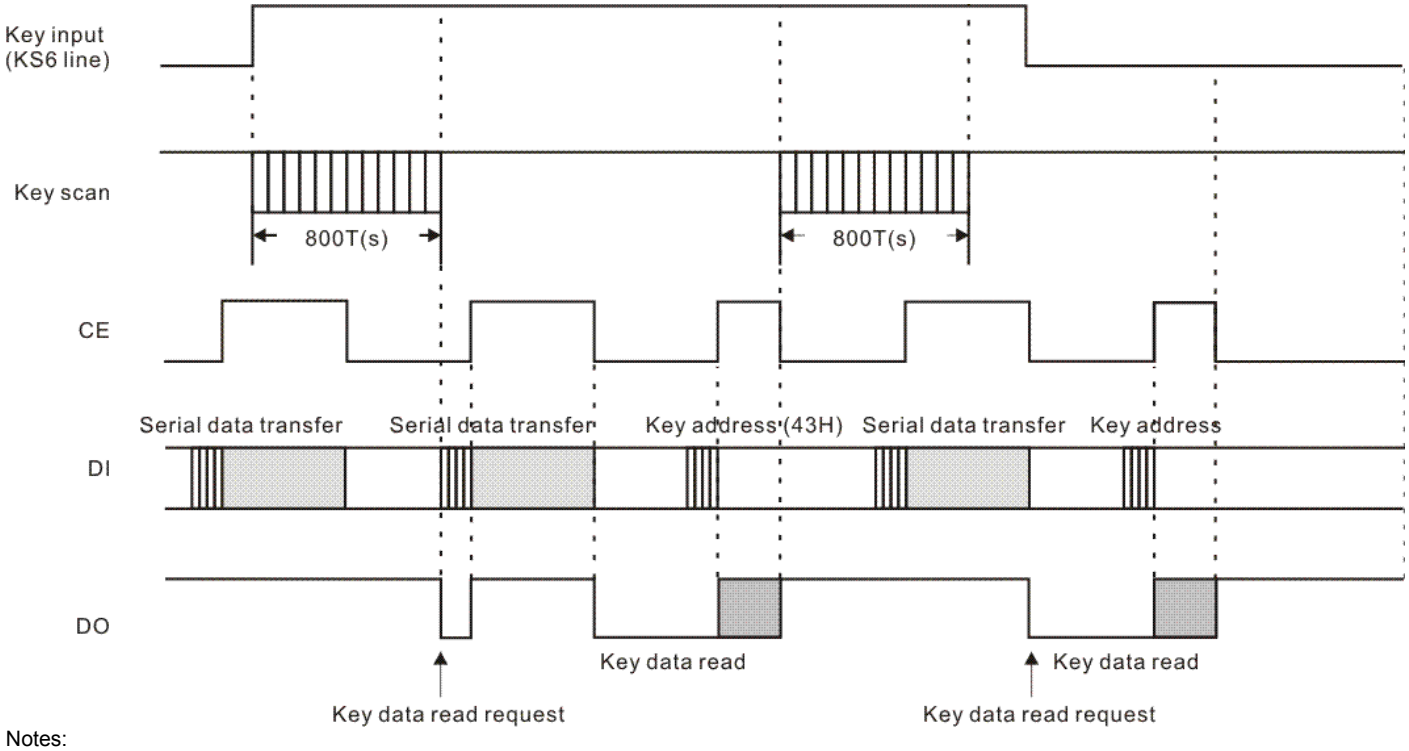
Notes:
1. T=1/fosc where fosc=oscillation frequency
2. The Sleep Mode, the state of these pins is determined by the control bits – S0 and S1. Key Scan signals are not outputted from pins that are set to “LOW” Level.

KEY SCAN OPERATING UNDER THE NORMAL MODE

Under the Normal Mode, the Key Scan Output Pins – KS1 to KS6 are set to HIGH. When a key is pressed, a key scan operation commences. The keys are scanned until all keys are released. For multiple key press operation, a multiple key press is valid only if multiple key data bits have set and verified by the key scan.

If a key is pressed longer than 800T(s), PT6554 outputs a key read data request (DO is set to “LOW” level) to the controller. The controller acknowledges the request and reads the key data. It must be noted that if CE is HIGH during a serial data transfer, then DO is set to “HIGH”.

After the controller reads the key data, the key data request is cleared (DO is set to HIGH) and another key scan operation is performed.



Notes:
1. T=1/fosc, where fosc is the oscillation frequency.
2. DO is an open – drain output and requires a pull-high resistor between 1KΩ to 10KΩ.

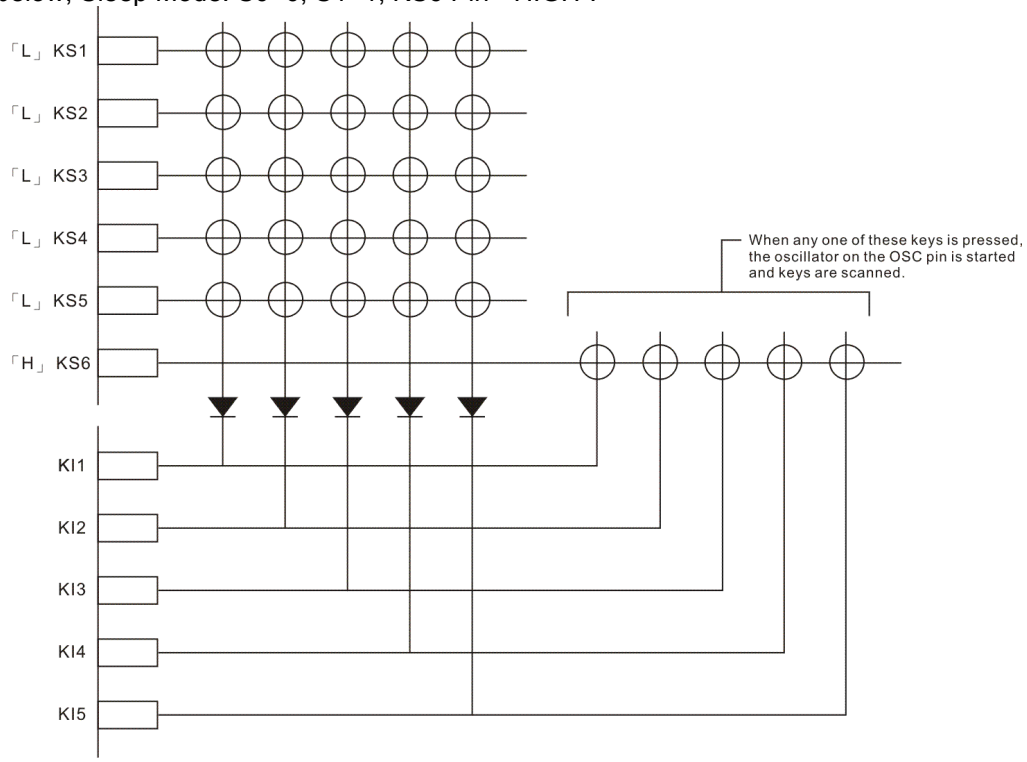
KEY SCAN OPERATION UNDER THE SLEEP MODE

Under the Sleep Mode, the key scan output pins – KS1 to KS6 are set either to HIGH or LOW" State by the Sleep Acknowledge Control Bits – S0 and S1. If a key that is located on one of the lines corresponding to a KS1 to KS6 pin that has been set to "HIGH" is pressed, then the oscillation commences and the key scan operation is executed. The keys are scanned until all keys are released. For multiple key press operation, a multiple key press is valid only if multiple key data bits have been set and verified by the key scan.

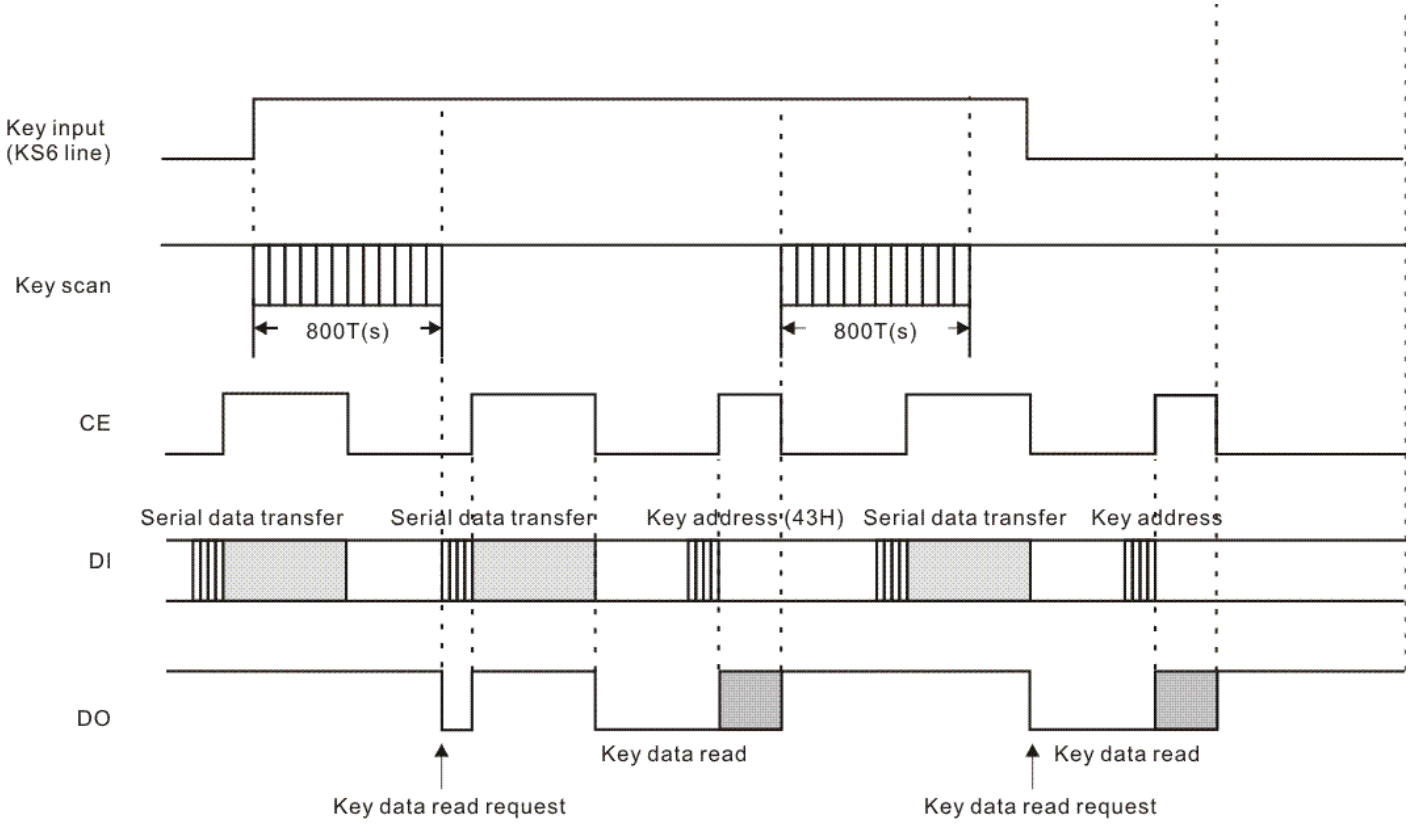
If a key is pressed longer than 800T (s), PT6554 outputs a key read data request (DO is set to LOW" level) to the controller. The controller acknowledges the request and reads the key data. It must be noted that if CE is "HIGH" during a serial data transfer, then DO is set to "HIGH".

After the controller reads the key data, the key data request is cleared (DO is set to "HIGH") and another key scan operation is performed. It must be noted that the Sleep Mode is not cleared. Please refer to the Sleep Mode Key Scan example given below.

In the example below, Sleep Mode: S0=0, S1=1, KS6 Pin="HIGH".



Notes:
1. T=1/fosc, where fosc is the oscillation frequency.
2. In order to prevent erroneous operation due to sneak current in the KS6 scan output signal when keys on the KS1 to KS5 lines are pressed at the same time, diodes must be connected as shown in the diagram above.



Note: DO is an open - drain output and requires a pull-high resistor between 1KΩ to 10KΩ.

KEY SCAN OPERATION FOR MULTIPLE KEY PRESSES

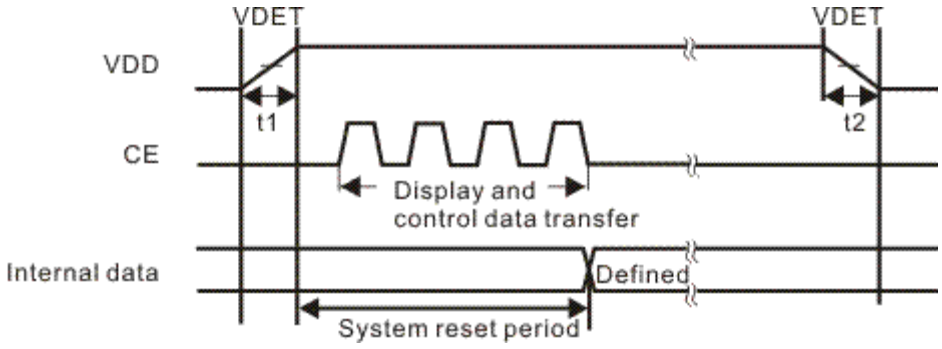
For dual key press operation, PT6554 can perform key scan operations without any need for a diode to be connected. For triple key press on the KI 1 to KI5 lines, multiple key presses on the KS1 to KS6 lines, and other multiple key presses require a diode to be connected in series with each key. Connecting a diode will ensure that only the keys that were pressed will be recognized. Applications that cannot determine triple or more multiple key presses must check the key data for three or more 1 bit and ignore such data.

VOLTAGE DETECTION TYPE RESET CIRCUIT (VDET)

The Voltage Detection Type Reset Circuit generates an output signal and resets the system when power is applied for the first time and when voltage drops (that is, for example, the power supply voltage is less than or equal to the power down detection voltage (VDET=3.0V typ).) To ensure that this reset function works properly, it is recommended that a capacitor be connected to the power supply line such that both the power supply voltage (VDD) rise time when power is first applied and the power supply voltage (VDD) fall time when the voltage drops are at least 1ms.

SYSTEM RESET

If the supply voltage (VDD) rise time when power is first applied is at least 1ms, then the VDET output signal will initiate a system reset when the supply voltage is increased. Likewise, if the supply voltage (VDD) fall time when power drops is at least 1ms, then the VDET output signal will initiate a system reset when the supply voltage is decreased. It must be noted that the reset function is cleared at the point when all the serial data (Display Data – D1 to D164 and the control data) have been completely transferred. Please refer to the figure below.



Power supply voltage VDD rise time: t1 > 1ms
Power supply voltage VDD fall time: t2 > 1ms

During the reset period, the internal states of the various blocks of PT6554 are enumerated below. It should be noted that the Address Interface, Control Register and the Shift Register Blocks are not reset during this period since serial data transfer is possible. (Please also refer to the Block Diagram Section)

CLOCK GENERATOR BLOCK

When the reset function is applied, the base clock is terminated. The state of the OSC pin (either Normal or Sleep Mode) is determined after the control bits – S0 and S1 have been transferred.

COMMON DRIVER, SEGMENT DRIVER & LATCH BLOCKS

When the reset function is applied the display is turned OFF. It should be noted, however, that the display data may be inputted to the latch circuit during the reset period.

KEY SCAN BLOCK

When the reset function is applied, the key scan circuit is set to the initial state and the key scan operation is disabled.

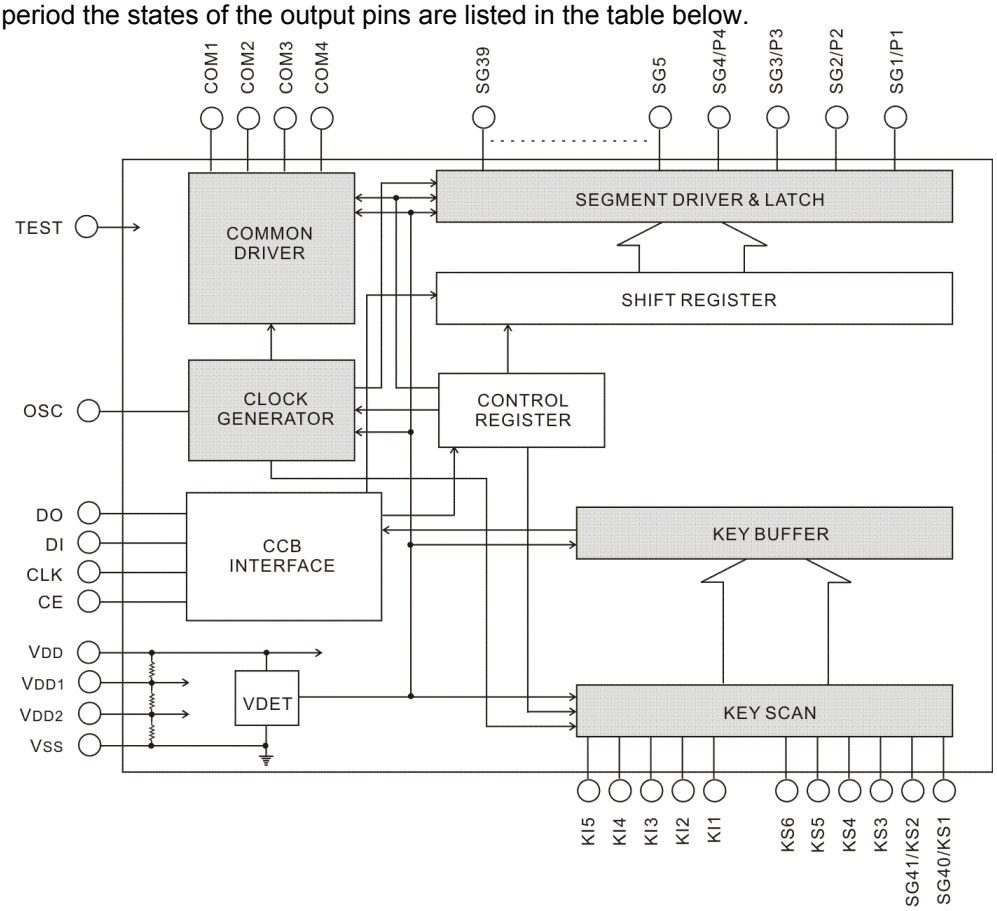
KEY BUFFER BLOCK

When the reset function is applied, all the key data are set to “LOW”.

CONTROL REGISTER & SHIFT REGISTER

Since serial data transfer is possible, these circuits are not reset.

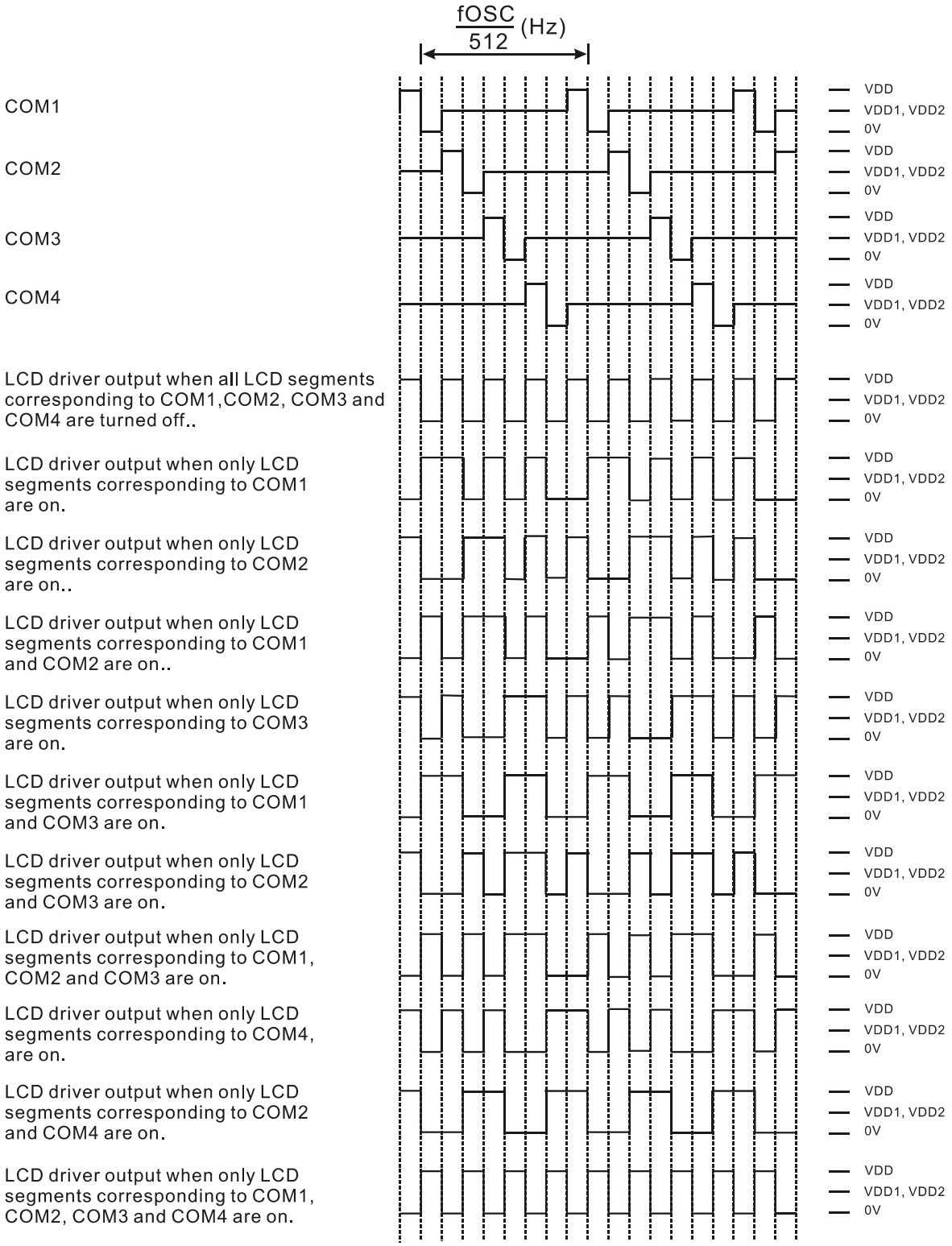
During the reset period the states of the output pins are listed in the table below.



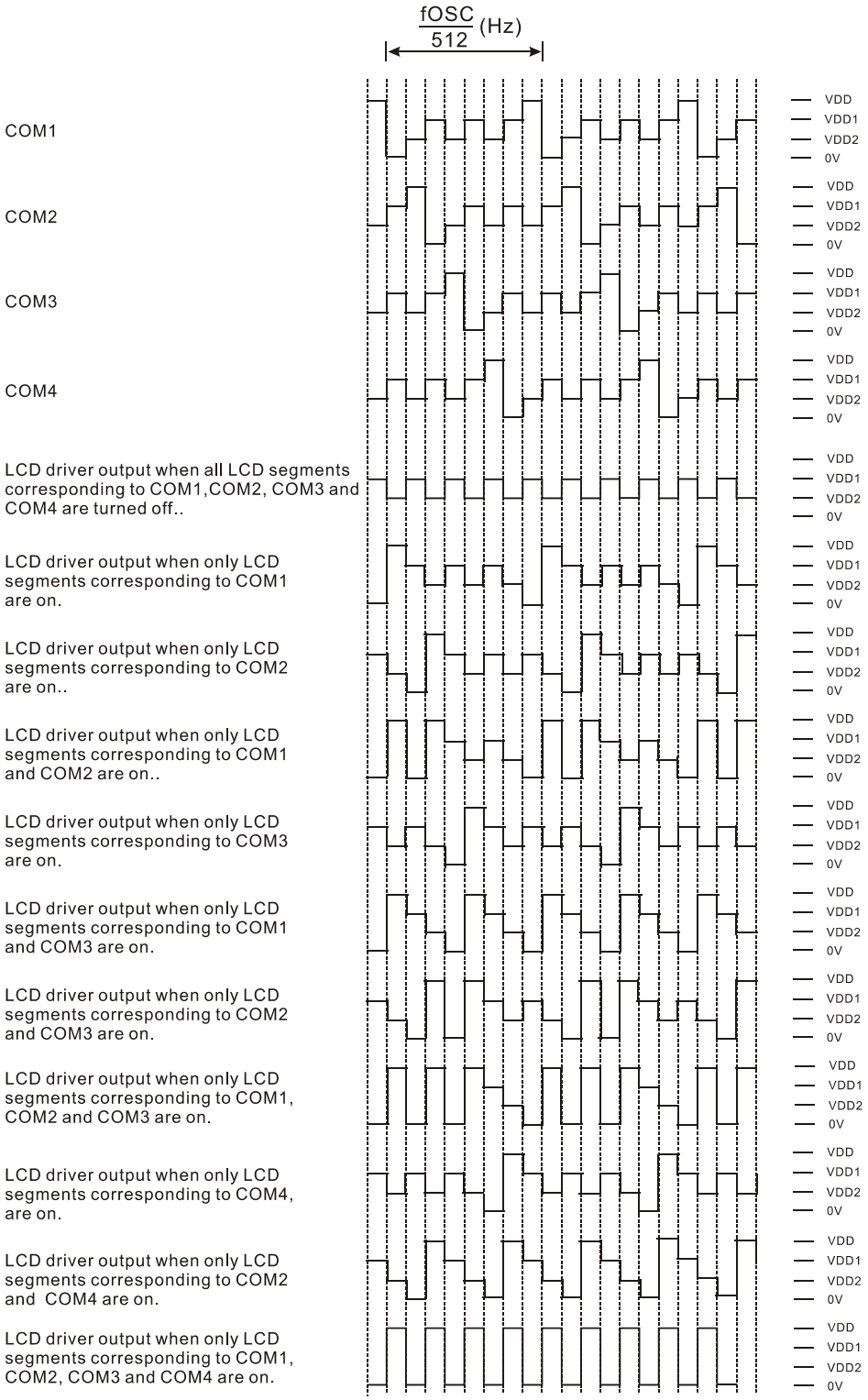
Output pin	State during reset
SG1/P1 to SG4/P4	L (Note 1)
SG5 to SG39	L
COM1 to COM4	L
KS1/SG40, KS2/SG41	L (Note 1)
KS3 to KS5	X (Note 2)
KS6	H
DO	H (Note 3)

Notes:
1. x = Not Relevant
2. These output pins are forcibly set to be used as Segment Driver Output Pins and are held at “LOW” State.
3. When power is first applied, these pins are not defines until the control bits – S0 and S1 have been completely transferred.
4. DO is an open - drain output and requires a pull-high resistor between 1KΩ to 10KΩ. It is kept at “HIGH” state during the reset period even if a key data read operation is executed..

1/4 DUTY, 1/2 BIAS DRIVE TECHNIQUE



1/4 DUTY, 1/3 BIAS DRIVE TECHNIQUE

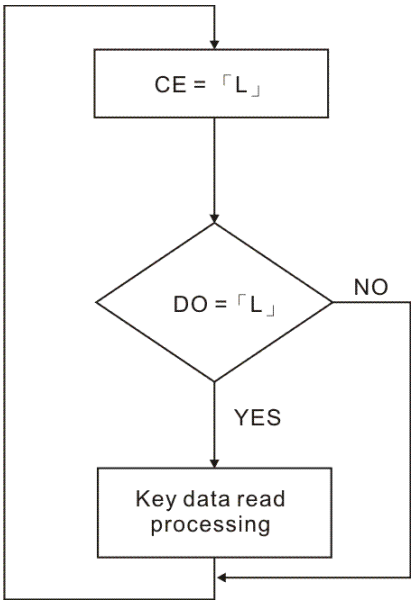


CONTROLLER KEY DATA READ TECHNIQUES

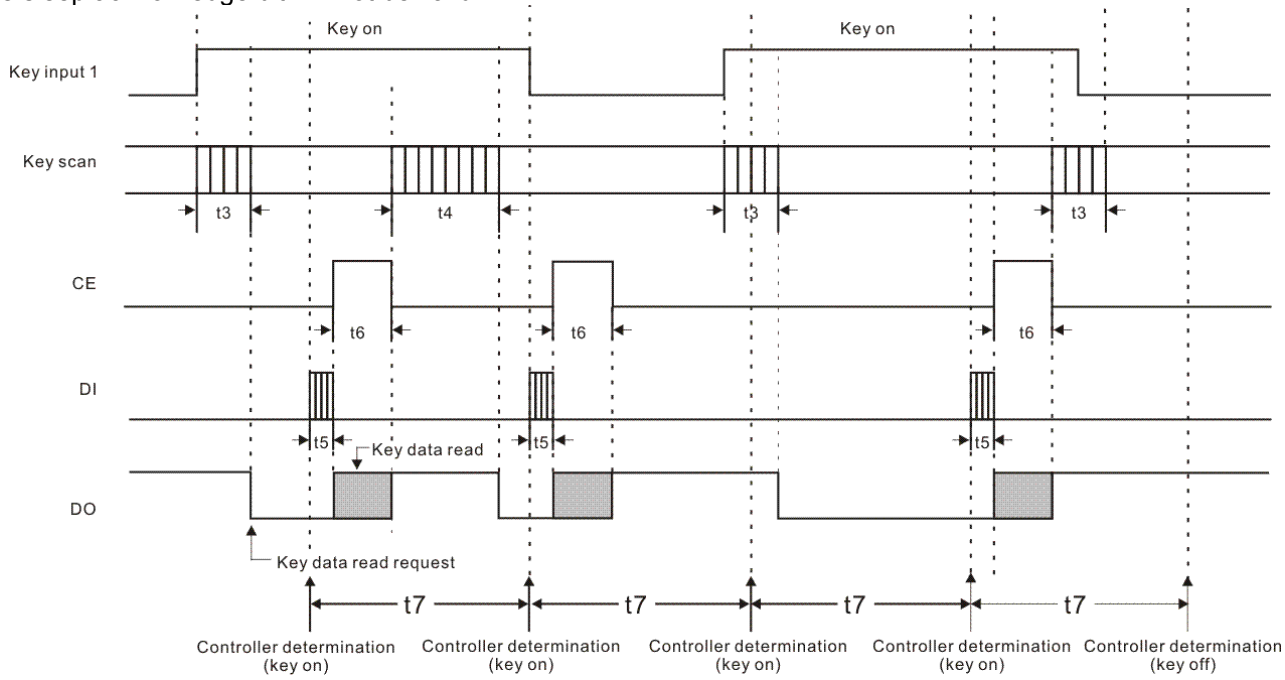
When the controller receives a key data read request from PT6554, it performs a key data read acquisition operation using either the Timer Based Key Data Acquisition or the Interrupt Based Key Data Acquisition.

TIMER BASED KEY DATA ACQUISITION TECHNIQUE

Under the Timer Based Key Data Acquisition Technique, the controller uses a timer to determine the states of the keys (ON or OFF) and read the key data. Please refer to the flowchart below.

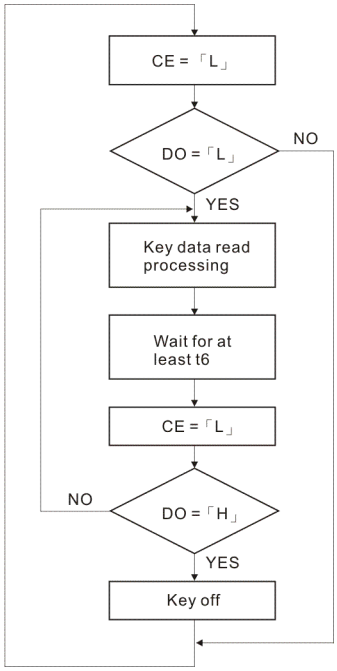


Every t7 period, the controller checks the state of DO when the CE is at “LOW” level. If DO is “LOW”, then the controller validates that a key has been pressed and performs a key data read operation. Please refer to the timing diagram below. It must be noted that if the key data read operation is performed when the DO is “HIGH”, the read key data (KD1 to KD30) and the sleep acknowledge bit will not be valid.

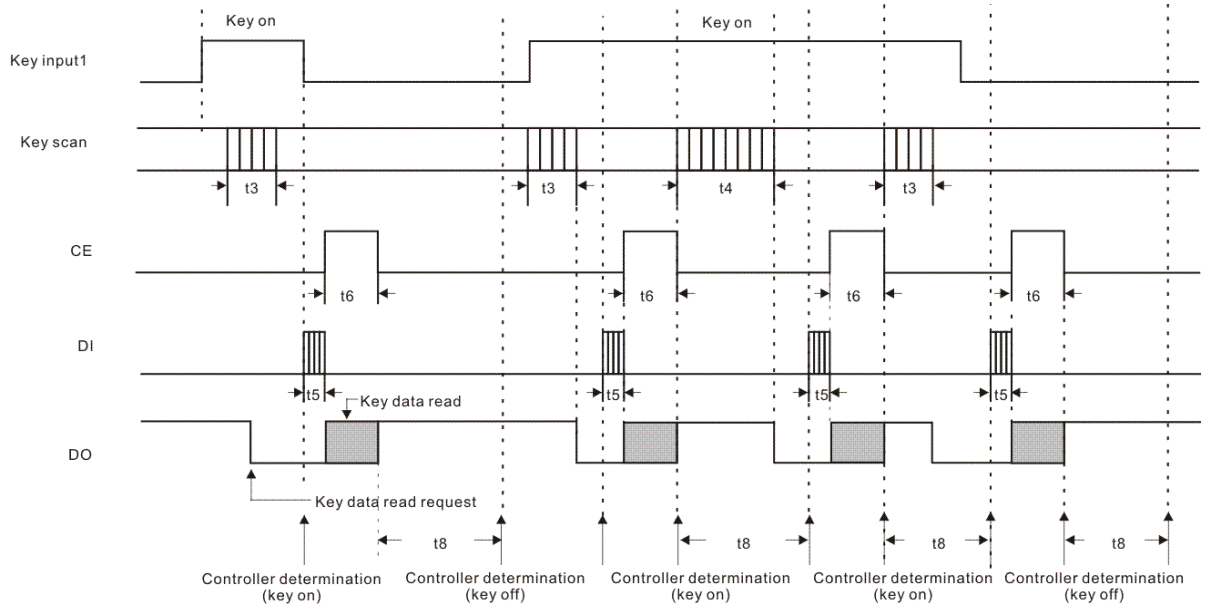


INTERRUPT BASED KEY DATA ACQUISITION TECHNIQUE

Under the Interrupt Based Key Data Acquisition Technique, the controller uses interrupts to determine the state of the keys (ON or OFF) and read the key data. Please refer to the flow chart diagram below.



Every t8 period, the controller checks the state of the DO Pin when CE is at “LOW” state. If the DO is at “LOW” level, then the controller validates that a key has been pressed and a key data read operation is performed. Please refer to the timing diagram below. It must be noted however, that if a key data read operation is performed when DO is held “HIGH”, the read key data – KD1 to KD30 and the sleep acknowledge bit SA will not be valid.



Notes:

1. t8 > t4
2. t3 is the Key Scan Execution Time when the key data matches (2 key scan operations): 800T (s)
3. t4 is the Key Scan Execution Time when the key data do not match (2 key scan operations) and the key scan operation is once again performed: 1600T (s).
4. T=1/fosc where fosc is the oscillation frequency.
5. t5 is the Key Address Transfer Time (43H)
6. t6 is the Key Data Read Time
7. T7 > (t5 + t6 + t4)

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, Ta=25℃, Vss=0V)

Parameter	Symbol	Conditions	Rating	Unit
Maximum supply voltage	VDD_{max}	VDD	-0.3 to +7.0	V
Input voltage	VIN1	CE, CLK, DI	-0.3 to VDD+0.3	V
	VIN2	OSC, KI1 to KI5, TEST, VDD1, VDD2	-0.3 to VDD+0.3	V
Output voltage	VOUT1	DO	-0.3 to VDD+0.3	V
	VOUT2	OSC, SG1 to SG41, COM1 to COM4, P1 to P4	-0.3 to VDD+0.3	V
Output current	IOUT1	SG1 to SG41	300	μA
	IOUT2	COM1 to COM4	3	mA
	IOUT3	KS1 to KS6	1	mA
	IOUT4	P1 to P4	5	mA
Allowable power dissipation	Pd max	Ta = 85℃	200	mW
Operating temperature	Topr		-40 to +85	℃
Storage temperature	Tstg		-40 to +150	℃

ALLOWABLE OPERATING CONDITIONS

(Unless otherwise specified, Ta=25℃, Vss=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VDD	VDD	4.5	-	6.0	V
Input voltage	VDD1	VDD1	-	2/3 VDD	VDD	V
	VDD2	VDD2	-	1/3 VDD	VDD	V
Input high level voltage	VIH1	CE, CLK, DI	0.8 VDD	-	VDD	V
	VIH2	KI1 to KI5	0.6 VDD	-	VDD	V
Input low level voltage	VIL	CE, CLK, DI, KI1 to KI5	0	-	0.2 VDD	V
Recommended external resistance	ROSC	OSC	-	62	-	KΩ
Recommended external capacitance	COSC	OSC	-	680	-	pF
Guaranteed oscillation range	fosc	OSC	25	50	100	KHz
Data setup time	tds	CLK, DI	160	-	-	ns
Data hold time	tdh	CLK, DI	160	-	-	ns
CE wait time	tcp	CE, CLK	160	-	-	ns
CE setup time	tcs	CE, CLK	160	-	-	ns
CE hold time	tch	CE, CLK	160	-	-	ns
High level clock pulse width	toH	CL	160	-	-	ns
Low level clock pulse width	toL	CL	160	-	-	ns
Rise time		CE, CLK, DI	-	160	-	ns
Fall time		CE, CLK, DI	-	160	-	ns
DO output delay time	tdc	DO, RPU=4.7KΩ, CL=10pF*1	-	-	1.5	μs
DO rise time	tdr	DO, RPU=4.7KΩ, CL=10pF*1	-	-	1.5	μs

ELECTRICAL CHARACTERISTICS FOR THE ALLOWABLE OPERATING CONDITIONS

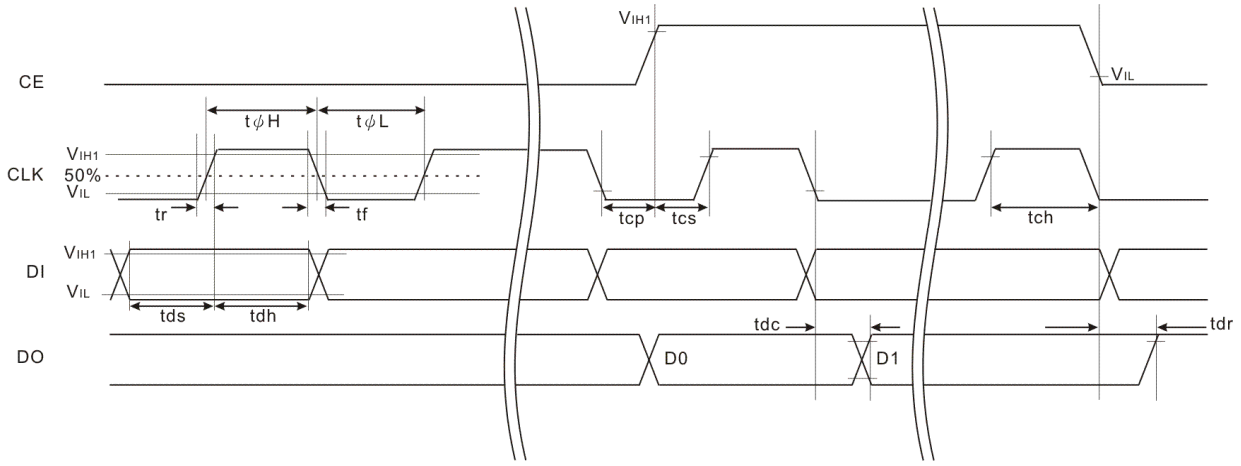
(Unless otherwise specified, Ta=25℃, V_{SS}=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Hysteresis	VH	CE, CLK, DI	-	0.1 VDD	-	V
Power-down detection voltage	VDET		2.7	3.0	-	V
Input high level voltage	IIH	CE, CLK, DI: VI=VDD	-	-	5.0	μA
Input high level current	IIL	CE, CLK, DI: VI=0V	-5.0	-	-	μA
Input floating voltage	VIF	KI1 to KI5	-	-	0.05VDD	V
Pull-down resistance	RPD	KI1 to KI5: VDD=5.0V	50	100	250	KΩ
Output off leakage current	IOFFH	DO: VO=6.0V	-	-	6.0	μA
Output high level voltage	VOH1	KS1 to KS6: IO=-500μA	VDD -1.2	VDD -0.5	VDD -0.2	V
	VOH2	P1 to P4: IO=-1mA	VDD -1.0	-	-	V
	VOH3	SG1 to SG41: IO=-20μA	VDD -1.0	-	-	V
	VOH4	COM1 to COM4: IO=-100μA	VDD -1.0	-	-	V
Output low level voltage	VOL1	KS1 to KS6: IO=25μA	0.2	0.5	1.5	V
	VOL2	P1 to P4: IO=1mA	-	-	1.0	V
	VOL3	SG1 to SG41: IO=20μA	-	-	1.0	V
	VOL4	COM1 to COM4: IO=100 μA	-	-	1.0	V
	VOL5	DO: IO=1mA	-	0.1	0.5	V
Output middle level voltage *2	VMID1	COM1 to COM4:1/2 bias, IO=±100μA	1/2VDD -1.0	-	1/2VDD +1.0	V
	VMID2	SG1 to SG41:1/3 bias, IO=±20μA	2/3VDD -1.0	-	2/3VDD +1.0	V
	VMID3	SG1 to SG41:1/3 bias, IO=±20μA	1/3VDD -1.0	-	1/3VDD +1.0	V
	VMID4	COM1 to COM4:1/3 bias, IO=±100μA	2/3VDD -1.0	-	2/3VDD +1.0	V
	VMID5	COM1 to COM4:1/3 bias, IO=±100μA	1/3VDD -1.0	-	1/3VDD +1.0	V
Oscillator frequency	fosc	OSC:R=62KΩ, C=680pF	40	50	60	KHz
Current drain	IDD1	Sleep mode	-	-	100	μA
	IDD2	VDD=6.0V, output open, 1/2 bias, fosc=50KHz	-	250	500	μA
	IDD3	VDD=6.0V, output open, 1/3 bias, fosc=50KHz	-	200	400	μA

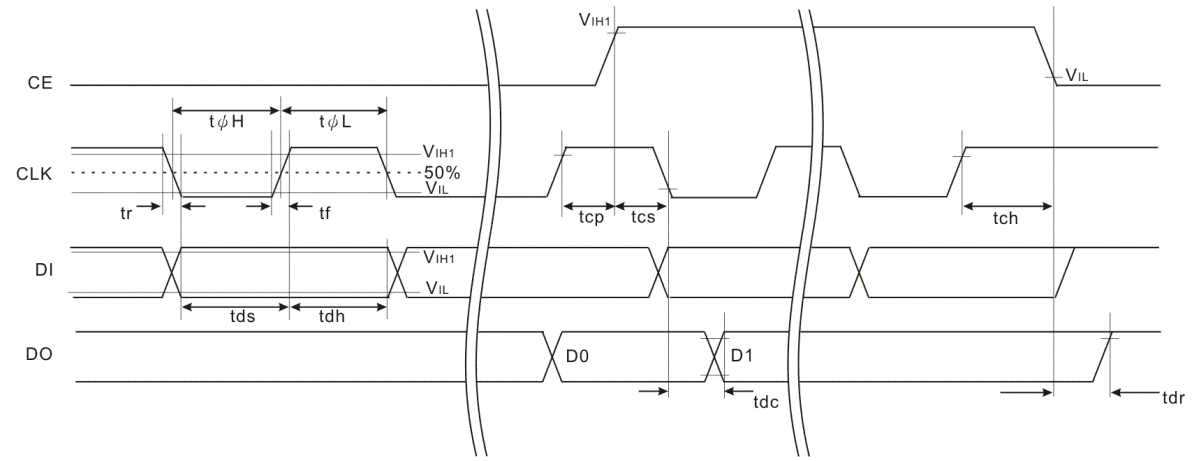
Notes:

1. A capacitor must be added to the power line so that both the power supply voltage (VDD) rise time when power is applied and the power supply voltage (VDD) fall time when power drops are at least 1 ms.
2. DO is an open – drain output and requires a pull-high resistor between 1KΩ to 10KΩ. The pull-up resistor value must be appropriate to the capacitor of the external wiring so that the signal wave forms are not degraded.

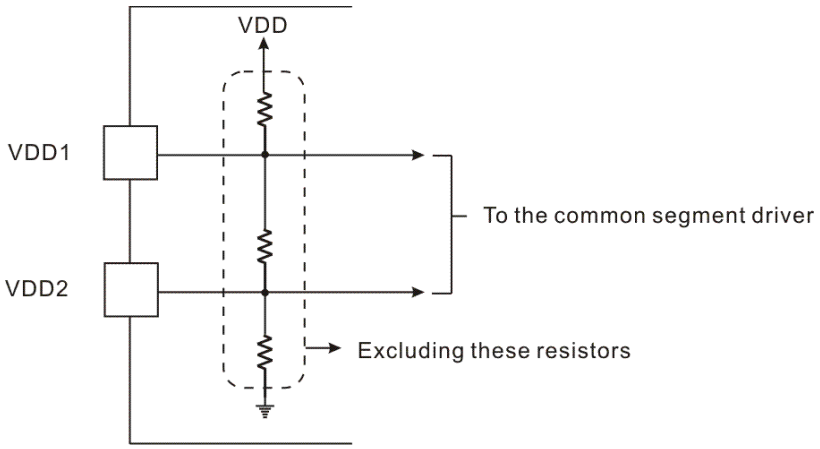
CASE 1: WHEN CLK IS TERMINATED AT LOW LEVEL.



CASE 2: WHEN CLK IS TERMINATED AT HIGH LEVEL.

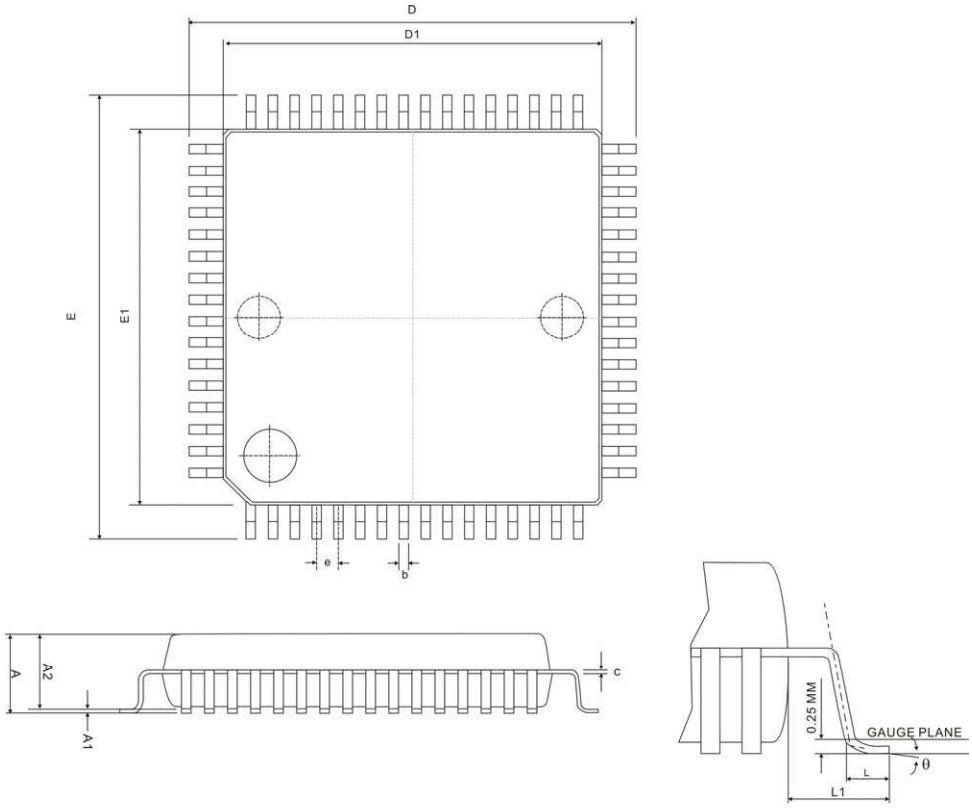


The Bias Voltage Generation Driver built-into VDD1 and VDD2 are not included. Please refer to the diagram below.



PACKING INFORMATION

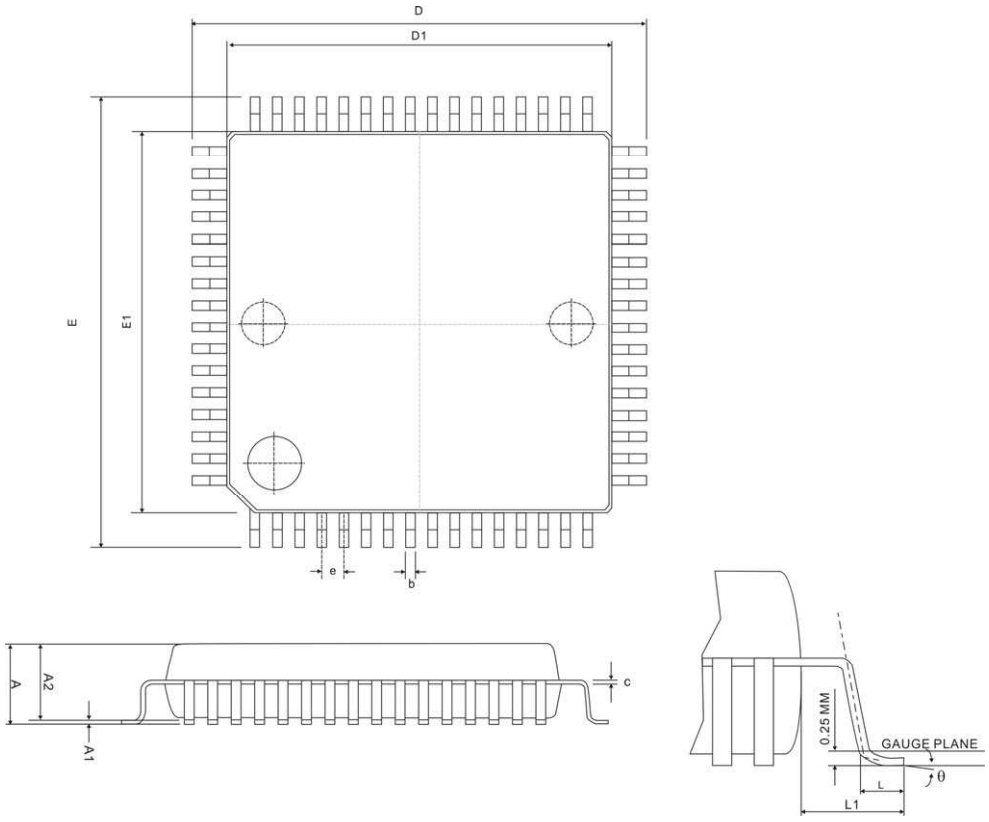
64-PINS, LQFP



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Notes:
1. All dimensions are in millimeter
2. Refer to JEDEC MS-026 BCD

64-PIN, QFP



Symbol	Min.	Nom.	Max.
A	-	-	3.15
A1	0.00	-	0.25
A2	1.90	-	2.90
b	0.29	0.35	0.41
c	0.11	-	0.23
D		17.20 BSC	
D1		14.00 BSC	
E		17.20 BSC	
E1		14.00 BSC	
e		0.80 BSC	
L	0.65	-	1.05
L1		1.60 REF	
θ	0°	-	8°

Notes:
1. Refer to JEDEC MC-022BE
2. All dimensions are in millimeter

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

Princeton Technology Corp.
2F, 233-1, Baociao Road,
Sindian Dist., New Taipei City 23145, Taiwan
Tel: 886-2-66296288
Fax: 886-2-29174598
http://www.princeton.com.tw