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DESCRIPTION

PT6553 is an LCD Driver IC providing key scan circuitry which can accept up to a maximum of 30 keys, thereby, reducing printed circuit board wiring. It can drive up to 126 segments and is capable of controlling up to 4 general purpose output ports. The reset circuit provides on-chip voltage detection making it possible to prevent incorrect displays. Pin assignments and application circuit are optimized for easy PCB layout and cost saving advantages.

FEATURES

- Up to 126 segments outputs
- Up to 4 general purpose output ports
- Key input function (up to 30 Keys)
- 1/3 duty - 1/2 bias and 1/3 duty - 1/3 bias drive techniques
- Sleep mode and all segments off function
- Direct display of display data without using a decoder
- On-chip voltage-detection type reset circuit
- RC oscillation circuit

APPLICATIONS

- Cellular phone
- Data bank, Organizer
- Electronic dictionary/Translator
- P.D.A.
- P.O.S.
- Information appliance
- Caller ID
- Pager
- Electronic equipment with LCD display

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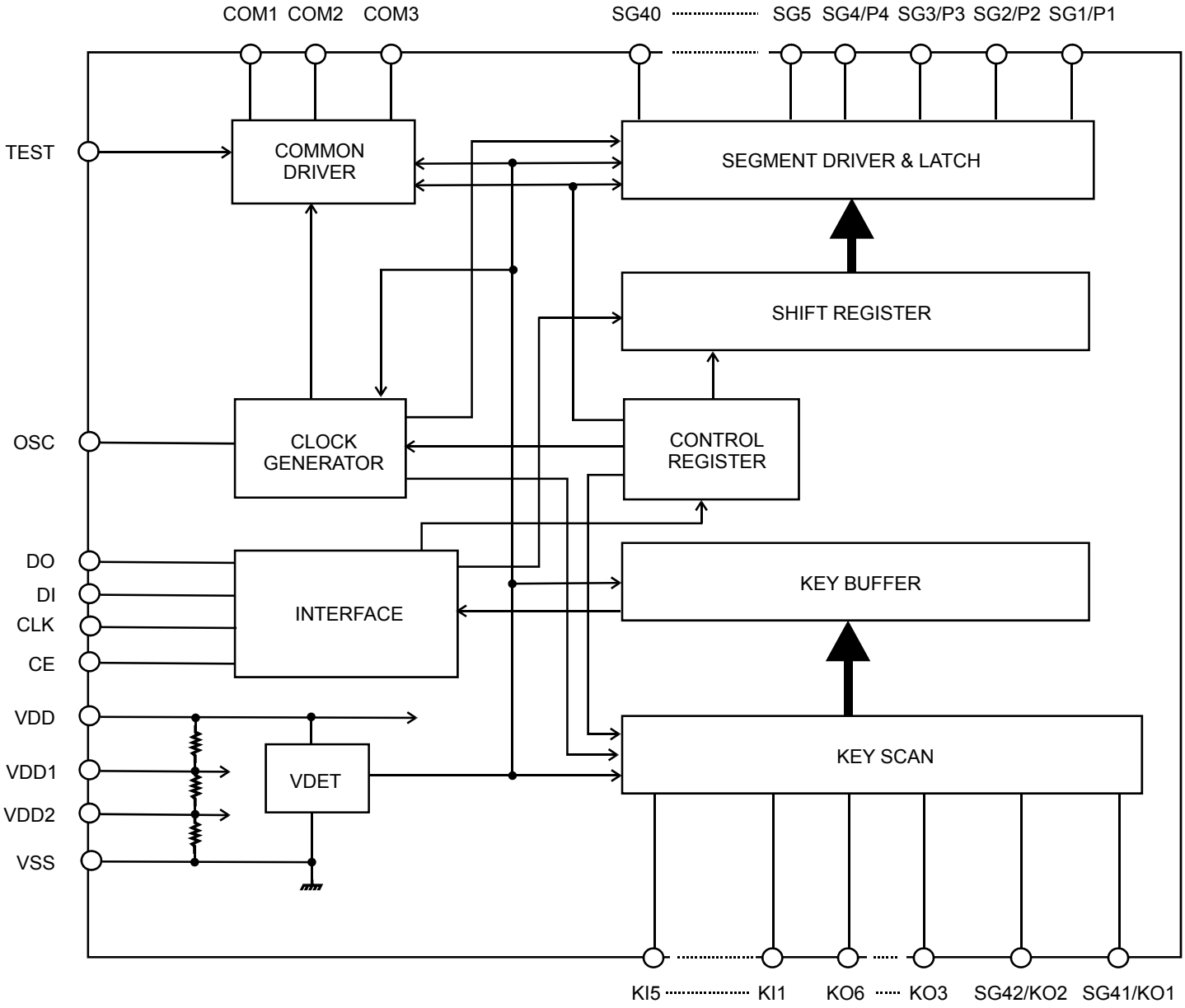
BLOCK DIAGRAM



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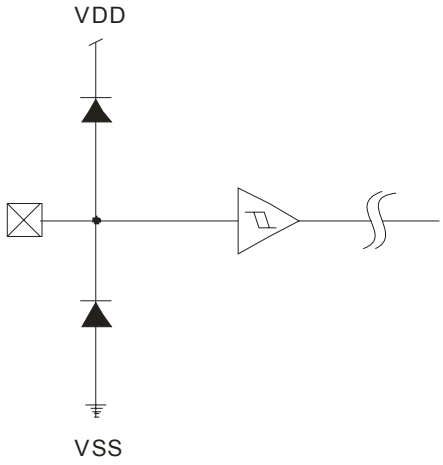
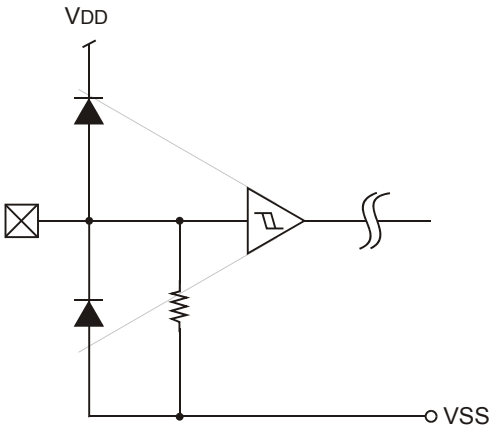
INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below:

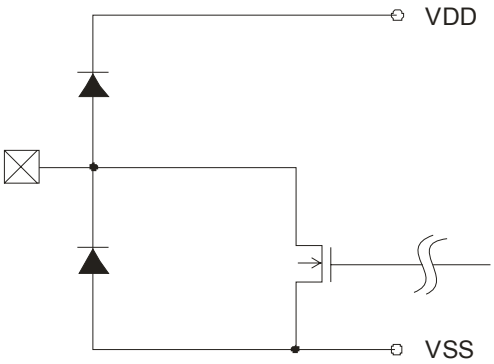
INPUT PIN: CLK, CE, DI



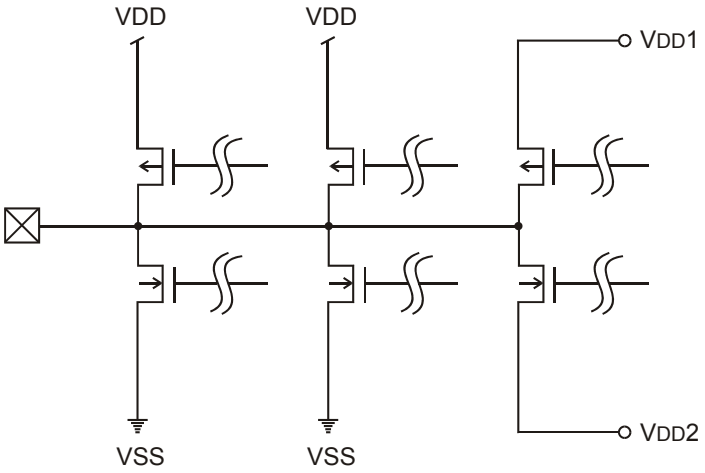
INPUT PIN: KI1 TO KI5



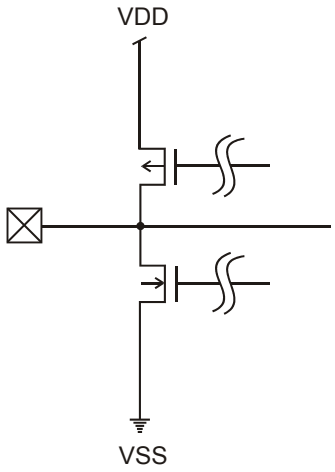
OUTPUT PIN: DO



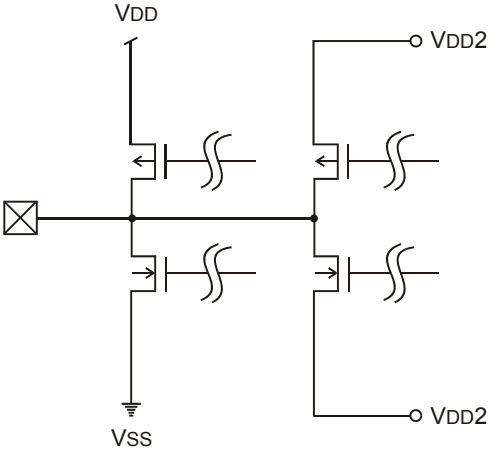
OUTPUT PIN: SG1/P1 TO SG4/P4, SG5 TO SG40, SG41/KO1, SG42/KO2



OUTPUT PIN: KO3 TO KO6



OUTPUT PIN: COM1 TO COM3



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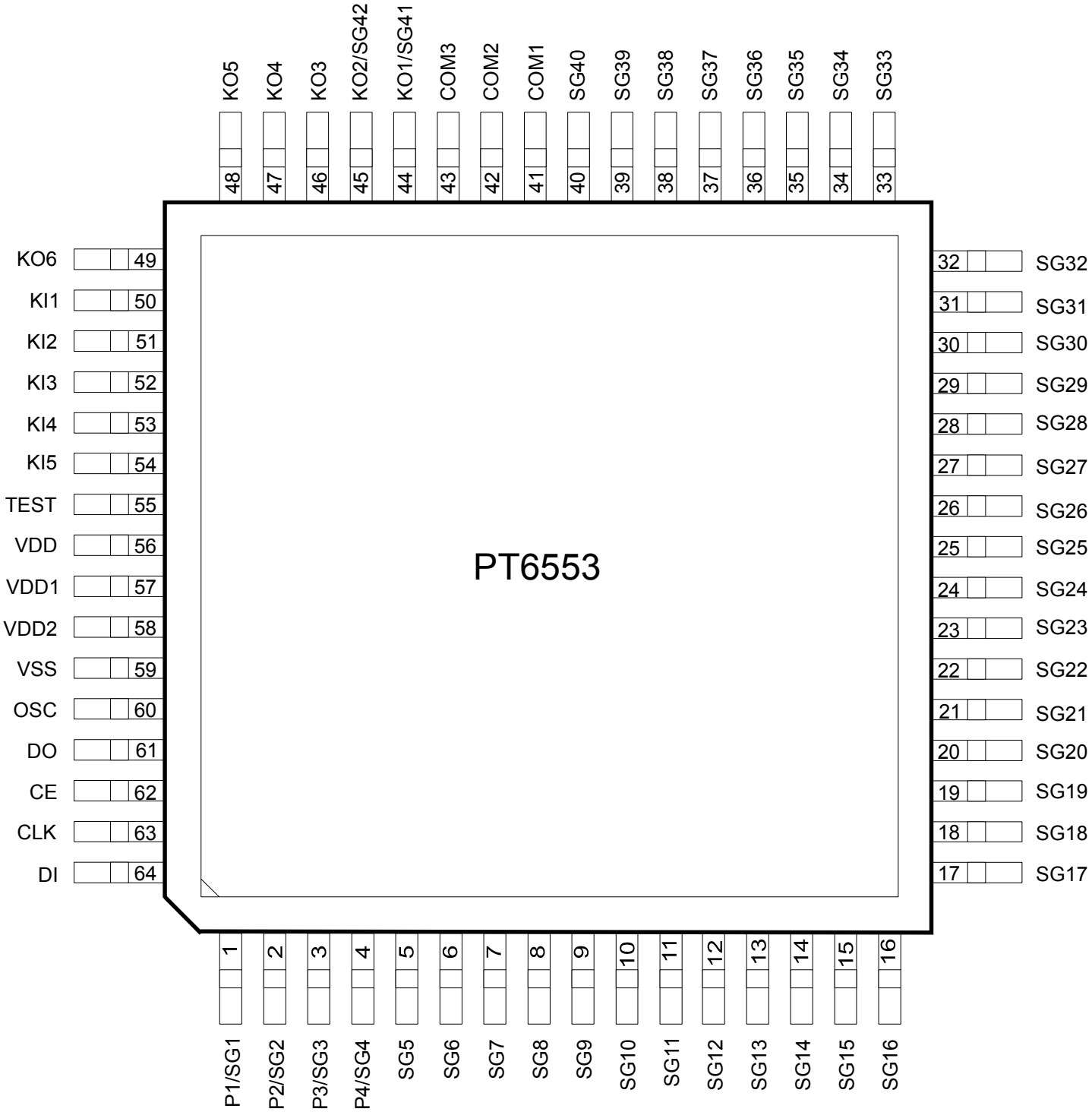
PIN CONFIGURATION



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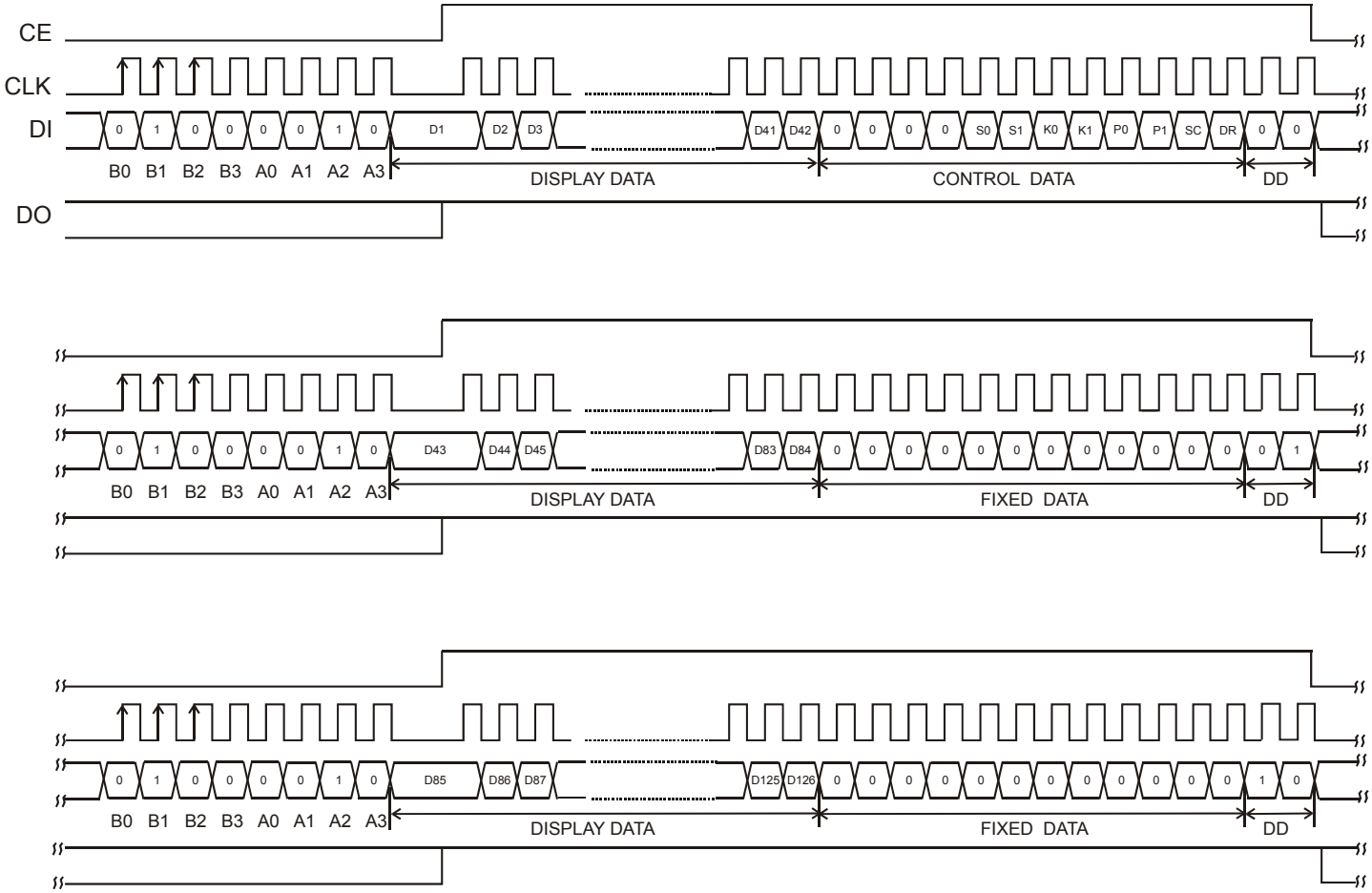
PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
SG1/P1 ~ SG4/P4	O	Segment Output/General Purpose Output Pins Under serial data control, these pins may be used a General Purpose Output Ports.	1 ~ 4
SG5 ~ SG40	O	Segment Output	5 ~ 40
COM1, COM2, COM3	O	Common Driver Output Pins	41, 42, 43
KO1/SG41	O	Key Scan Output/Segment Output Pin	44
KO2/SG42	O	Key Scan Output/Segment Output Pin	45
KO3 ~ KO6	O	Key Scan Output Pins	46 ~ 49
KI1 ~ KI5	I	Key Scan Input Pins	50 ~ 54
TEST	I	Test Pin	55
VDD	-	Power Supply	56
VDD1	-	Power Supply This power supply pin is used for applying the LCD Drive 2/3 bias voltage externally and must be connected to VDD2 when using 1/2 bias drive.	57
VDD2	-	Power Supply This power supply pin is used for applying the LCD Drive 1/3 bias voltage externally and must be connected to VDD1 when using 1/2 bias drive.	58
VSS	-	Ground	59
OSC	I/O	Oscillator Pin	60
DO	O	Data Output Pin	61
CE	I	Chip Enable Pin	62
CLK	I	Synchronization Clock Input Pin	63
DI	I	Data Transfer Input Pin	64

FUNCTION DESCRIPTION

SERIAL DATA INPUT

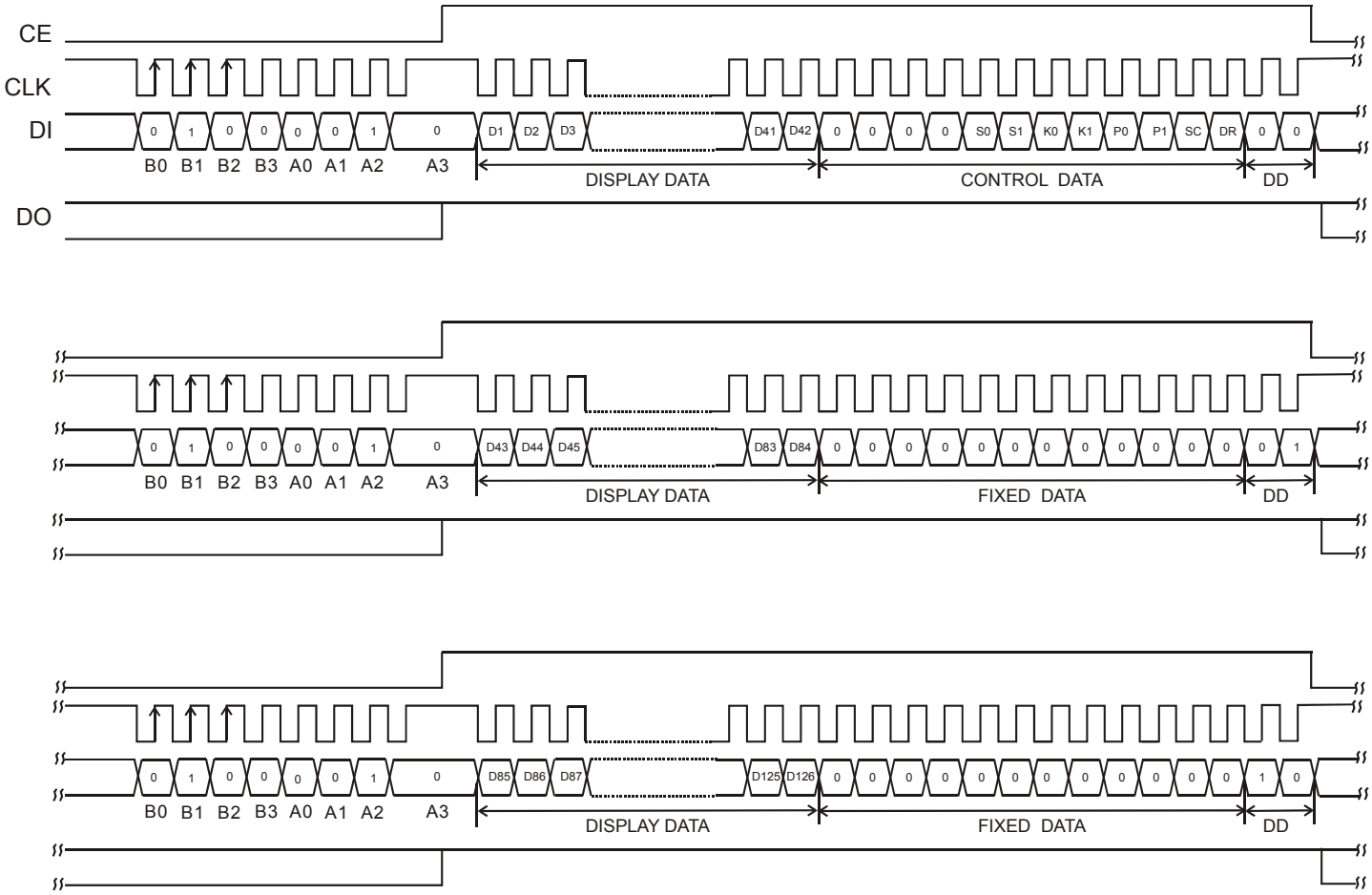
CONDITION 1: CLK IS TERMINATED AT THE "LOW" LEVEL



Where: DD= Direction Data

- Address: 42H
- D1 to D126: Display Data
- S0, S1: Sleep Control Data
- K0, K1: Key Scan Output/Segment Output Selection Data
- P0, P1: Segment Output Port/General Purpose Output Port Selection Data
- SC: Segment ON/OFF Control Data
- DR: 1/2 Bias or 1/3 Bias Drive Selection Data

CONDITION 2: CLK IS TERMINATED AT THE "HIGH" LEVEL



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- DR: 1/2 Bias or 1/3 Bias Drive Selection Data

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CONTROL DATA FUNCTIONS

SLEEP CONTROL DATA BITS: S0, S1

S0 and S1 are sleep control data bits which can be switched between the normal and the sleep modes. They are used to set the states of the KO1 to KO6 Key Scan Outputs when the key scan is in a standby mode.

Control Data		Mode	OSC	Segment Outputs Common Outputs	State of Output Pin during Key Scan Standby Condition					
S0	S1				KO1	KO2	KO3	KO4	KO5	KO6
0	0	Normal	Operating	Operating	H	H	H	H	H	H
0	1	Sleep	Stopped	L	L	L	L	L	L	H
1	0	Sleep	Stopped	L	L	L	L	L	H	H
1	1	Sleep	Stopped	L	H	H	H	H	H	H

Note: This is under the assumption that the KO1/SG41 and KO2/SG42 Pins are selected for Key Scan Output.

KEY SCAN OUTPUT/SEGMENT OUTPUT SELECTION CONTROL DATA BITS: K0, K1

K0 and K1 are control data bits which may be used for key scan output or segment output.

Control Data		State of Output Pins		Maximum Number of Input Keys
K0	K1	KO1/SG41	KO2/SG42	
0	0	KO1	KO2	30
0	1	SG41	KO2	25
1	x	SG41	SG42	20

Note: x = Irrelevant

SEGMENT OUTPUT/GENERAL PURPOSE OUTPUT PORTS SELECTION DATA BITS: P0, P1

P1 and P0 are control data bits which may be used for segment output port or general purpose output port.

Control Data		State of Output Pin			
P0	P1	SG1/P1	SG2/P2	SG3/P3	SG4/P4
0	0	SG1	SG2	SG3	SG4
0	1	P1	P2	SG3	SG4
1	0	P1	P2	P3	SG4
1	1	P1	P2	P3	P4

Condition 1: P0 and P1 are selected as General Purpose Output Port

When the control data bits, P0 and P1 are selected as General Purpose Output Port, the corresponding display data and output pins are listed below.

Output Pin	Corresponding Display Data
SG1/P1	D1
SG2/P2	D4
SG3/P3	D7
SG4/P4	D10

This means that, if for example the output pin -- SG4/P4 is used as a General Purpose Output Port, SG4/P4 Pin will output a high level when the display data , D10 is given a value of "1".

SEGMENT ON/OFF CONTROL DATA BITS: SC

SC is used to control the ON/OFF state of segments.

SC	Display State
0	On
1	Off

When SC is set to "0", the segment display state is "ON". When SC is set to "1", the segment display is "OFF". This "OFF" state is achieved by outputting segment "OFF" waveforms from the segment output pins.

1/2 BIAS OR 1/3 BIAS DRIVE SELECTION DATA BIT: DR

DR is the control data bit used to select either an LCD 1/2 or 1/3 bias drive. When DR is set to "0", the 1/3 LCD Bias Drive is selected. On the other hand, if DR is set to "1", the 1/2 LCD Bias Drive is selected.

DR	LCD Bias Drive
0	1/3
1	1/2

DISPLAY DATA AND OUTPUT PINS

The display data and their corresponding output pins are listed in the table below.

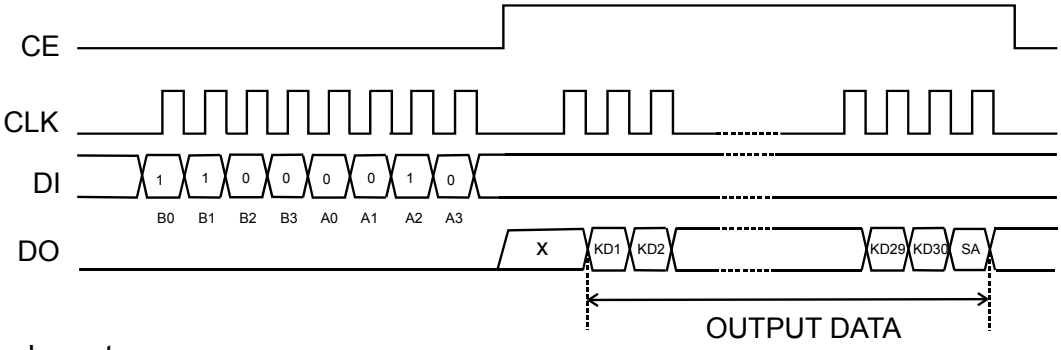
Output Pin	COM1	COM2	COM3	Output Pin	COM1	COM2	COM3
SG1/P1	D1	D2	D3	SG22	D64	D65	D66
SG2/P2	D4	D5	D6	SG23	D67	D68	D69
SG3/P3	D7	D8	D9	SG24	D70	D71	D72
SG4/P4	D10	D11	D12	SG25	D73	D74	D75
SG5	D13	D14	D15	SG26	D76	D77	D78
SG6	D16	D17	D18	SG27	D79	D80	D81
SG7	D19	D20	D21	SG28	D82	D83	D84
SG8	D22	D23	D24	SG29	D85	D86	D87
SG9	D25	D26	D27	SG30	D88	D89	D90
SG10	D28	D29	D30	SG31	D91	D92	D93
SG11	D31	D32	D33	SG32	D94	D95	D96
SG12	D34	D35	D36	SG33	D97	D98	D99
SG13	D37	D38	D39	SG34	D100	D101	D102
SG14	D40	D41	D42	SG35	D103	D104	D105
SG15	D43	D44	D45	SG36	D106	D107	D108
SG16	D46	D47	D48	SG37	D109	D110	D111
SG17	D49	D50	D51	SG38	D112	D113	D114
SG18	D52	D53	D54	SG39	D115	D116	D117
SG19	D55	D56	D57	SG40	D118	D119	D120
SG20	D58	D59	D60	KO1/SG41	D121	D122	D123
SG21	D61	D62	D63	KO2/SG42	D124	D125	D126

Example: The segment output pin -- SG11 has the corresponding display data bits -- D31, D32, D33. The table below gives the segment output states of SG11 Pin.

Display Date			State of Output Pin
D31	D32	D33	SG11
0	0	0	LCD Segments for Com1, Com2, and Com3 are "Off"
0	0	1	LCD Segments for Com3 is "On"
0	1	0	LCD Segment for Com2 is "On"
0	1	1	LCD Segments for Com2 and Com3 are "On"
1	0	0	LCD Segments for Com1 is "On"
1	0	1	LCD Segments for Com1 and Com3 are "On"
1	1	0	LCD Segments for Com 1 and Com2 are "On"
1	1	1	LCD Segments for Com1, Com2, and Com3 are "On

SERIAL DATA OUTPUT

CONDITION 1: CLK IS TERMINATED AT THE "LOW" LEVEL

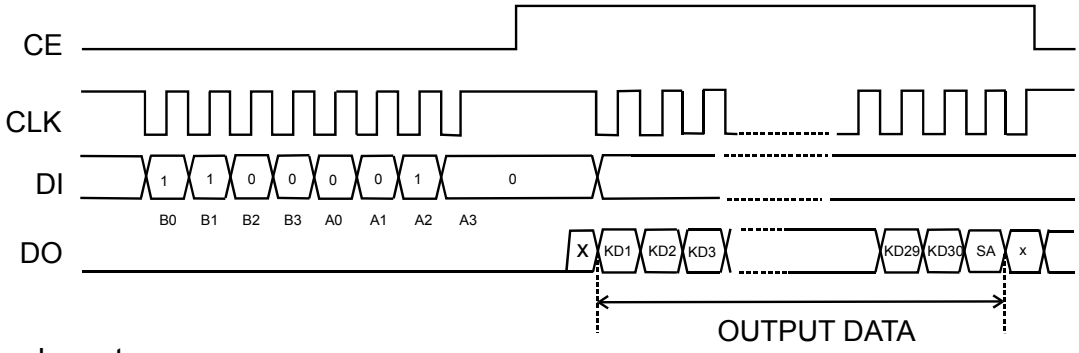


Where: x = Irrelevant

- Address: 43H
- KD1 to KD30: Key Data
- SA: Sleep Acknowledge Data

Notes:
1. The SA (Sleep Acknowledge data) will not be valid if the key data read operation is executed when the DO is in "HIGH" level.
2. To be able to read the data correctly, the data reading process must be performed in the midpoint of the rising and falling edge of the clock.

CONDITION 2: CLK IS TERMINATED AT THE "HIGH" LEVEL



Where: x = Irrelevant

- Address: 43H
- KD1 to KD30: Key Data
- SA: Sleep Acknowledge Data

Notes:
1. The SA (Sleep Acknowledge data) will not be valid if the key data read operation is executed when the DO is in "HIGH" level.
2. To be able to read the data correctly, the data reading process must be performed in the midpoint of the rising and falling edge of the clock.

OUTPUT DATA

KEY DATA: KD1 TO KD30

A key matrix having a maximum of 30 keys maybe constructed using the KO1 to KO6, and KI1 to KI5 lines. If any one of these keys are pressed, the key output data corresponding to the respective key is set to "1". Please refer to the table below.

	KI1	KI2	KI3	KI4	KI5
KO1/SG41	KD1	KD2	KD3	KD4	KD5
KO2/SG42	KD6	KD7	KD8	KD9	KD10
KO3	KD11	KD12	KD13	KD14	KD15
KO4	KD16	KD17	KD18	KD19	KD20
KO5	KD21	KD22	KD23	KD24	KD25
KO6	KD26	KD27	KD28	KD29	KD30

When a key matrix (maximum of 20 keys) are constructed using the KO3 to KO6 and KI1 to KI5 lines and the KO1/SG41 and KO2/SG42 pins are used as Segment Output Pins via the control data bits -- K0 and K1--, the KD1 to KD10 key data bits are set to "0".

SLEEP ACKNOWLEDGE DATA BIT: SA

SA is sleep acknowledge data bit. SA is set to "1" during the Sleep Mode and "0" during the Normal Mode. When the key is pressed, the sleep acknowledge data bit will be set to the state.

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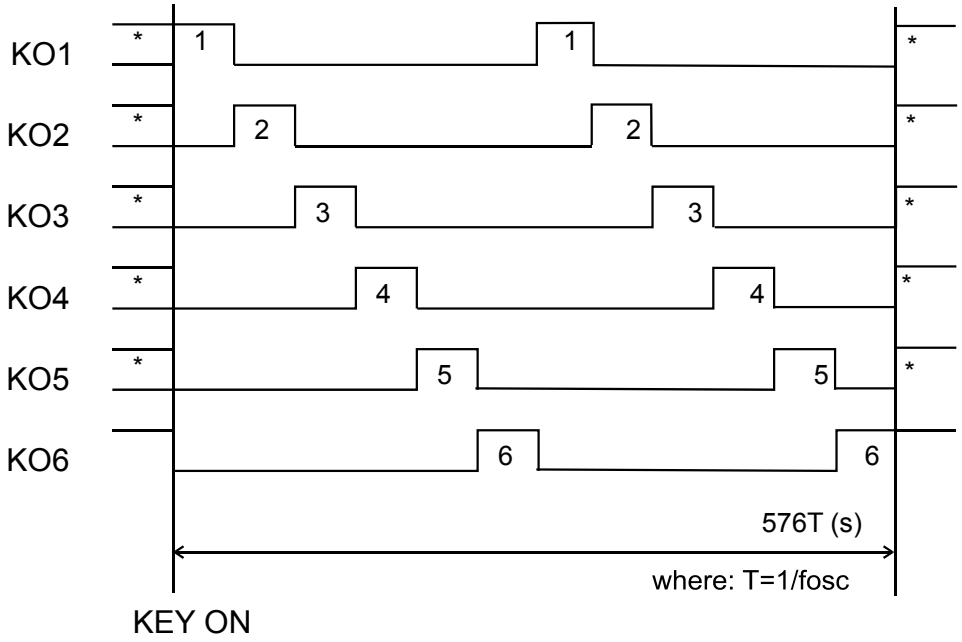
SLEEP MODE FUNCTION

The Sleep Mode is activated by setting S0 or S1 to "1". Both the segment and common outputs will be "LOW" and oscillation operation will stop reducing the power dissipation. However, oscillation operation will be activated again when a key is pressed. The Sleep Mode is deactivated when both S0 and S1 bits are set to "0". It should be noted that even in the Sleep Mode, the SG1/P1 to SG4/P4 pins can also be used as General Purpose Output Ports depending on the states of the P0 and P1 control data bits. Please refer to the control data section for details.

KEY SCAN OPERATION

KEY SCAN TIMING

The key scan period is 288T (s). The key is scanned twice and when the key data is in agreement with the key that has been pressed, then the key operation is valid. The key data read request (DO is set to "LOW") is outputted after starting a key scan operation. If the key data is not in agreement with the key that has been pressed, the PT6553 scans the key again. PT6553 can only detect a key press longer than or equal to 615T (s). Please refer to the diagram below.



Note:
* = During the Sleep Mode Condition, the States ("HIGH" or "LOW") of these pins are determined by the control data bits -- S0 and S1 bits. When these pins are set to "LOW" State the key scan output signals are not outputted.

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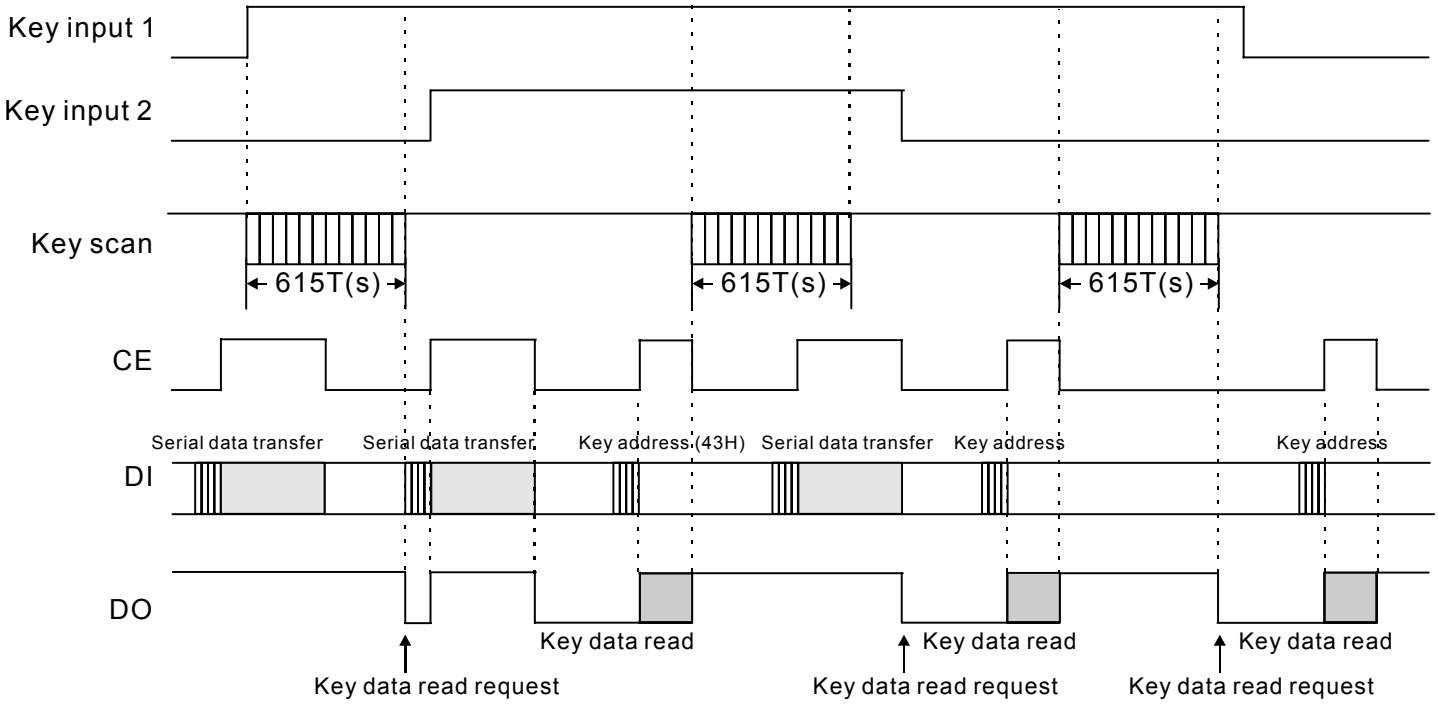
NORMAL MODE

Under the normal mode, the pins -- KO1 to KO6 -- are set to "HIGH". When a key is pressed, a key scan operation commences. The keys are scanned until all keys are released. Multiple key operation is recognized. When a key is pressed longer than 615T (s), PT6553 outputs a key data read request to the controller. Please take note that T= 1/[fosc] and during the key data read request, the DO is set to "LOW". The controller then acknowledges the key data request and reads the key data. However, if the CE is "HIGH" during the serial data transfer, DO will be set to "HIGH". After the key data reading operation is completed, the key data request is cleared (DO is set to "HIGH") and another key scan operation is performed. It must be noted that DO is an open-drain output and thus requires a 1K to 10K Ohms pull-up resistor. Please refer to the diagram below.



T = 1/fosc