

DESCRIPTION

The PT6522 is a general purpose LCD display driver which can be used for frequency display applications in microprocessor-controlled radio receivers and other display applications.

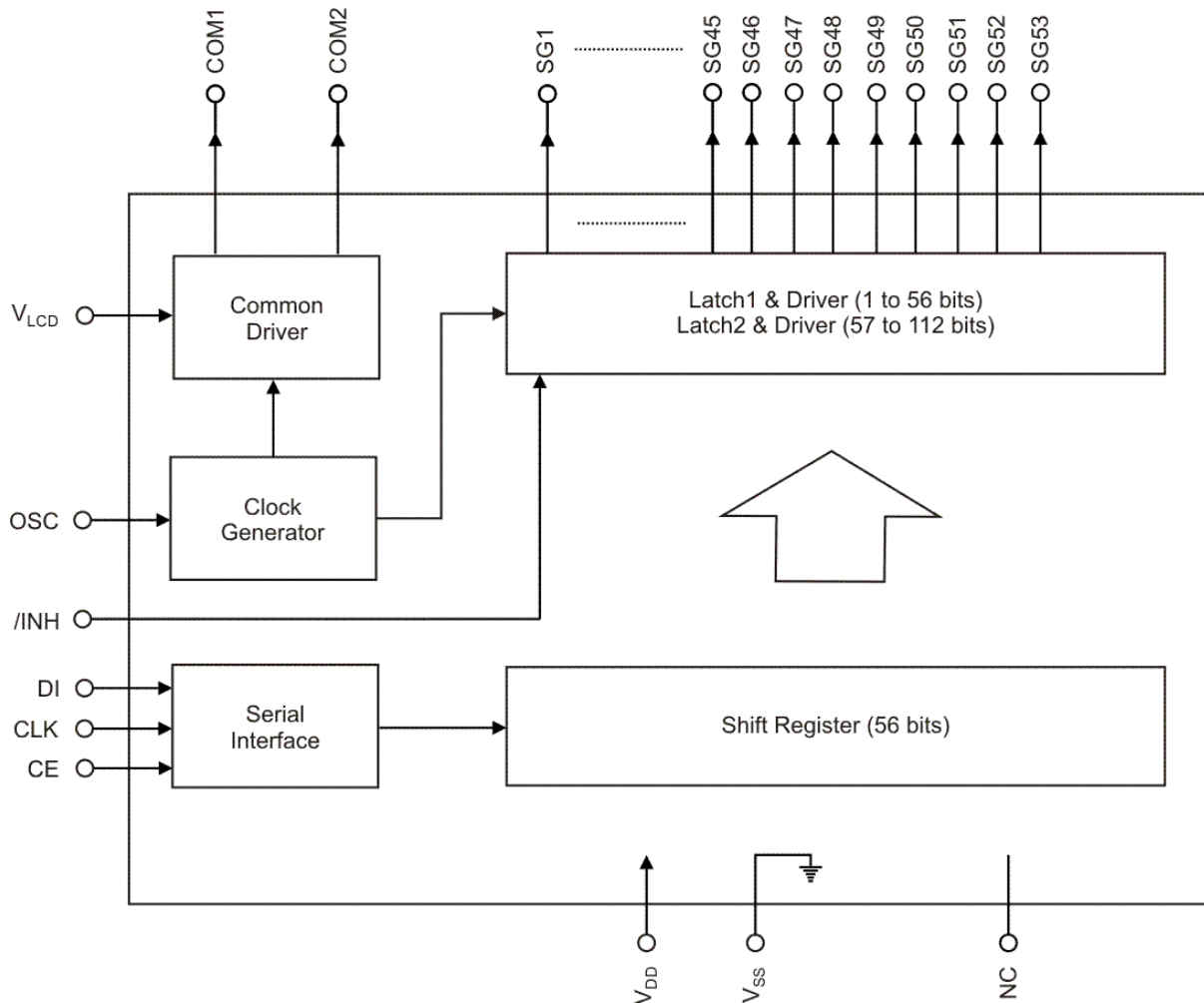
APPLICATIONS

- Electronic dictionary/calculator
- P.O.S. terminal
- Call ID device
- Pager
- Mini component system
- Electronic equipment with LCD display

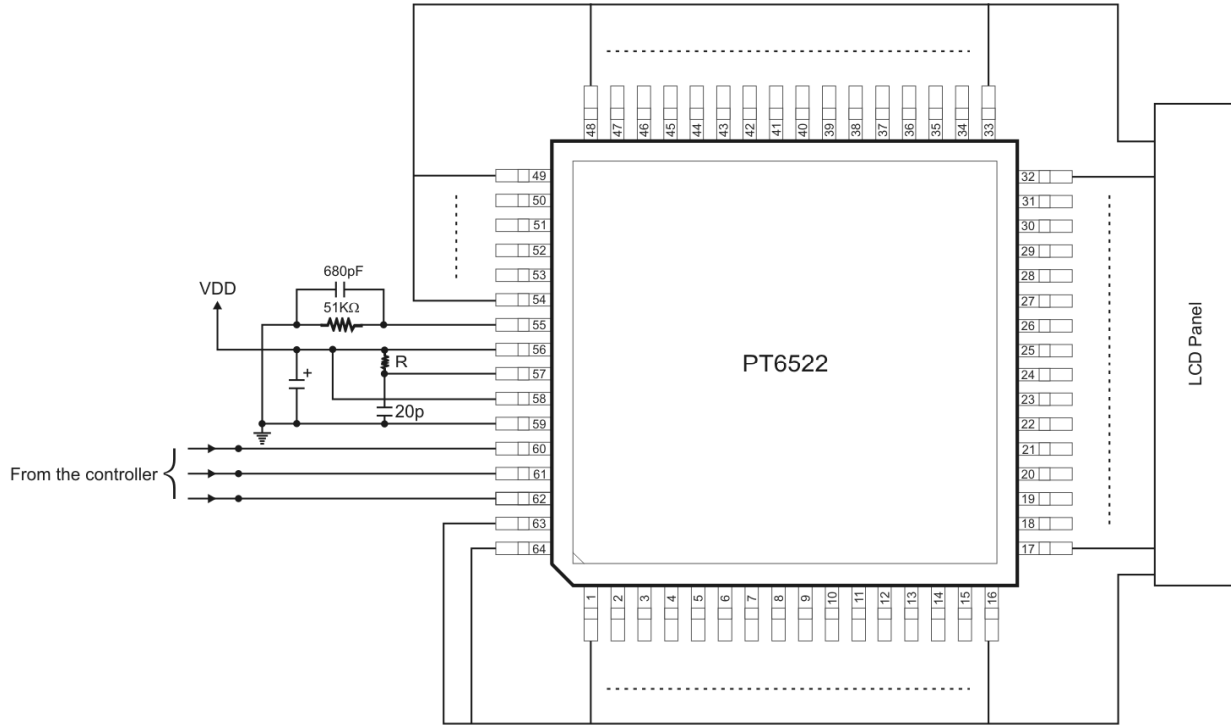
FEATURES

- 53 segment outputs
- Two drive types are possible: static (1/1) duty (53 segments) and 1/2 duty (104 segments)
- INH pin for turning off all display output
- RC oscillation circuit
- Power supply voltage: 3.0 to 6.5V
- Available in 64-pin QFP or LQFP package

BLOCK DIAGRAM

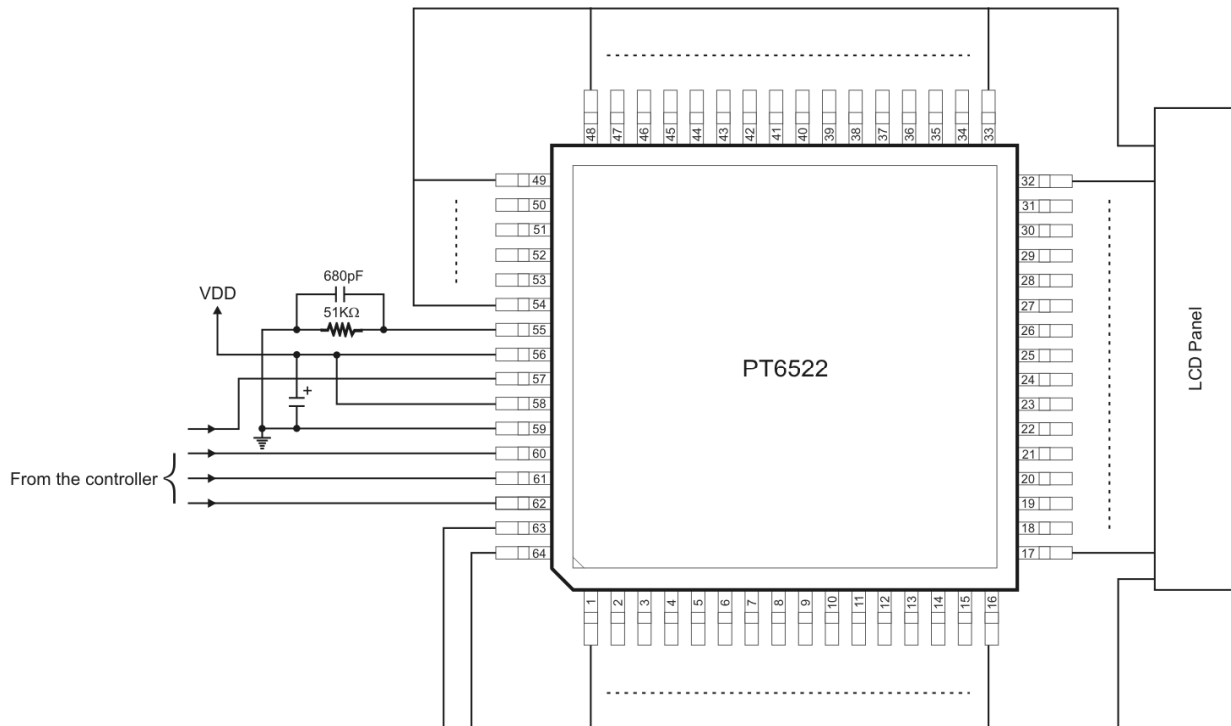


APPLICATION CIRCUIT 1



Note: $39K\Omega \geq R \geq 10K\Omega$

APPLICATION CIRCUIT 2



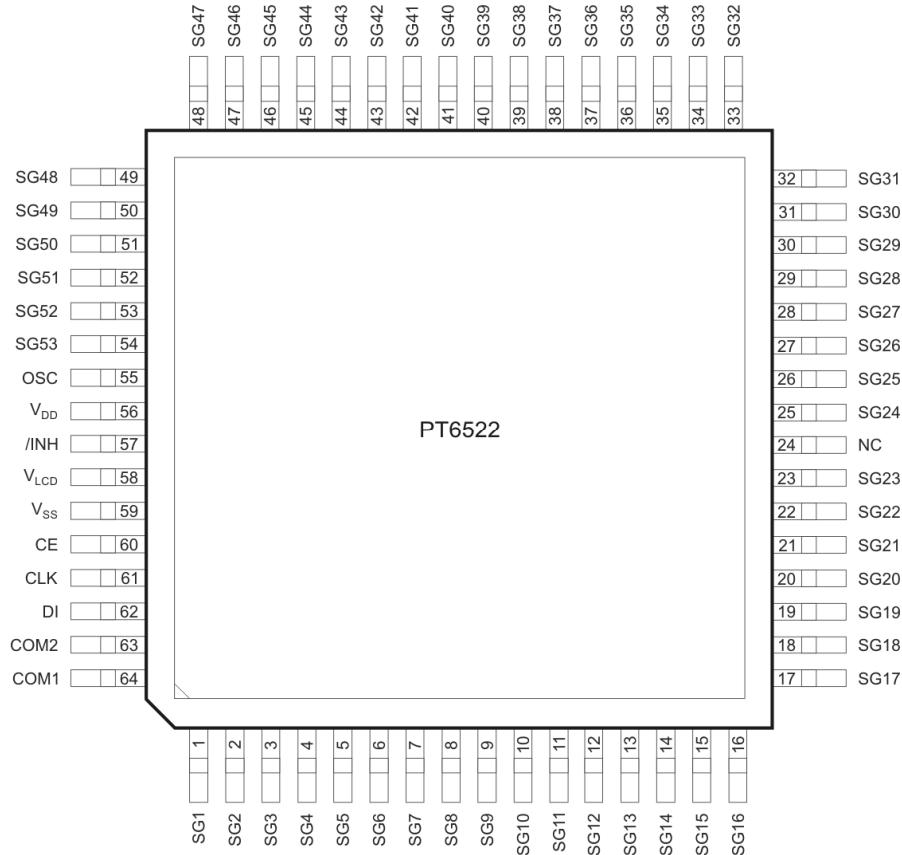
Note:

When power (V_{DD}) is first applied, the internal display data is undefined and a meaningless pattern will result if the display is turned on in this state. To avoid the display should be turned off by setting $/INH$ low and turned on only after display data has been sent from the controller.

ORDERING INFORMATION

Valid Part Number	Package Type	Top Code
PT6522-Q	64 pins, QFP	PT6522-Q
PT6522LQ	64 pins, LQFP	PT6522LQ

PIN CONFIGURATION



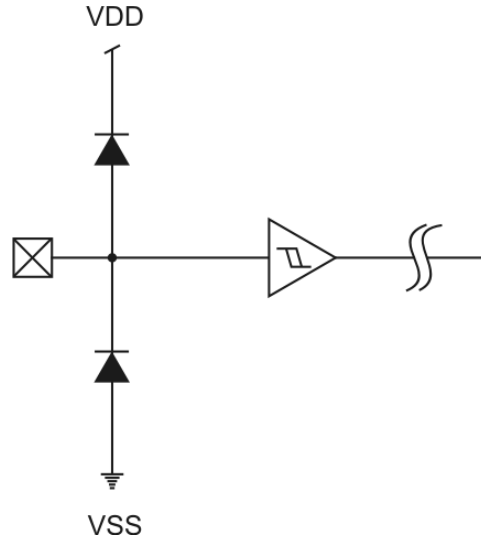
PIN DESCRIPTION

Pin Name	Description	Pin No.
SG1 to SG53	Segment output pins	1~23, 25~53
OSC	Oscillator connection	55
VSS, VDD	Power supply	59, 56
/INH	Display off control input /INH=low (VSS)=Display off (SG1 to SG53, COM1, COM2=low) /INH=high (VDD)=Display on Note that serial data transfers are allowed when display output is turned off using this pin.	57
VLCD	LCD bias voltage setting	58
CE, CLK, DI	Serial data transfer inputs	60, 61, 62
COM1, COM2	Common output pins (For static (1/1) drive only COM1 is used, COM2 must be left open)	64, 63
NC	No connection	24

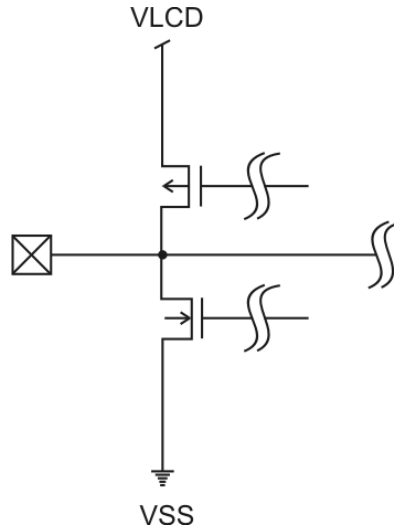
INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below:

INPUT PIN: CLK, CE, DI, /INH



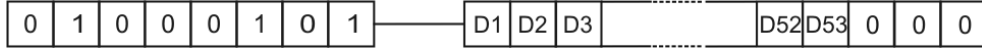
OUTPUT PIN: COM1 TO COM2, SG1 TO SG53



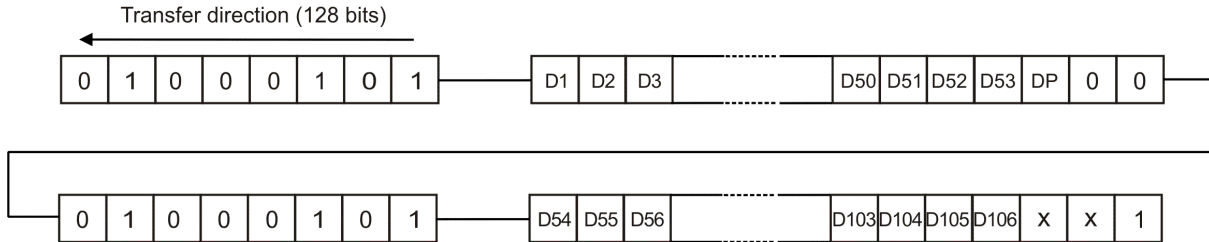
FUNCTION DESCRIPTION

DATA TRANSFER FORMAT

1. Static (1/1) duty



2. 1/2 duty (if there are no more than 52 display segments, only 64 bits need to be transferred. The transfer format is the same as the static duty case. It is not possible to alter the D54 to D106 data without specifying the D1 to D53 data.)



The values of bits D53 and D106 are ignored.
(don't care)

Address: A2_H

DP: Drive type selection bit

DP=0: 1/1 duty

DP=1: 1/2 duty

D1 to D106: Display data

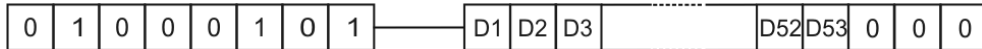
D_n (for n=1 to 106)=0: Segment off

D_n (for n=1 to 106)=1: Segment on

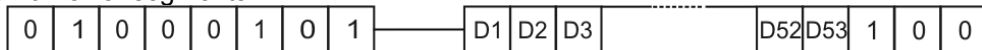
x: don't care

DATA TRANSFER EXAMPLES

1. Static duty



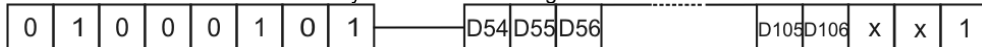
2. 1/2 duty with 52 or fewer segments



3. 1/2 duty with more than 52 segments

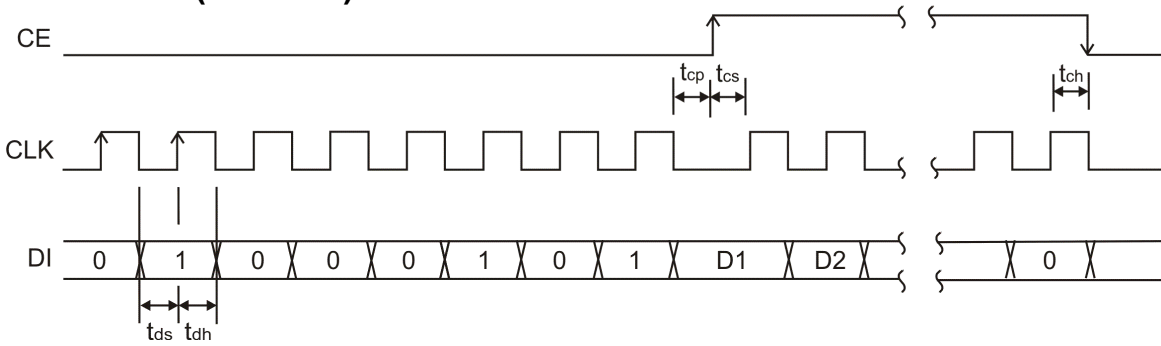


Note: the following transfer format is not allowed in 1/2 duty with 52 or fewer segments.

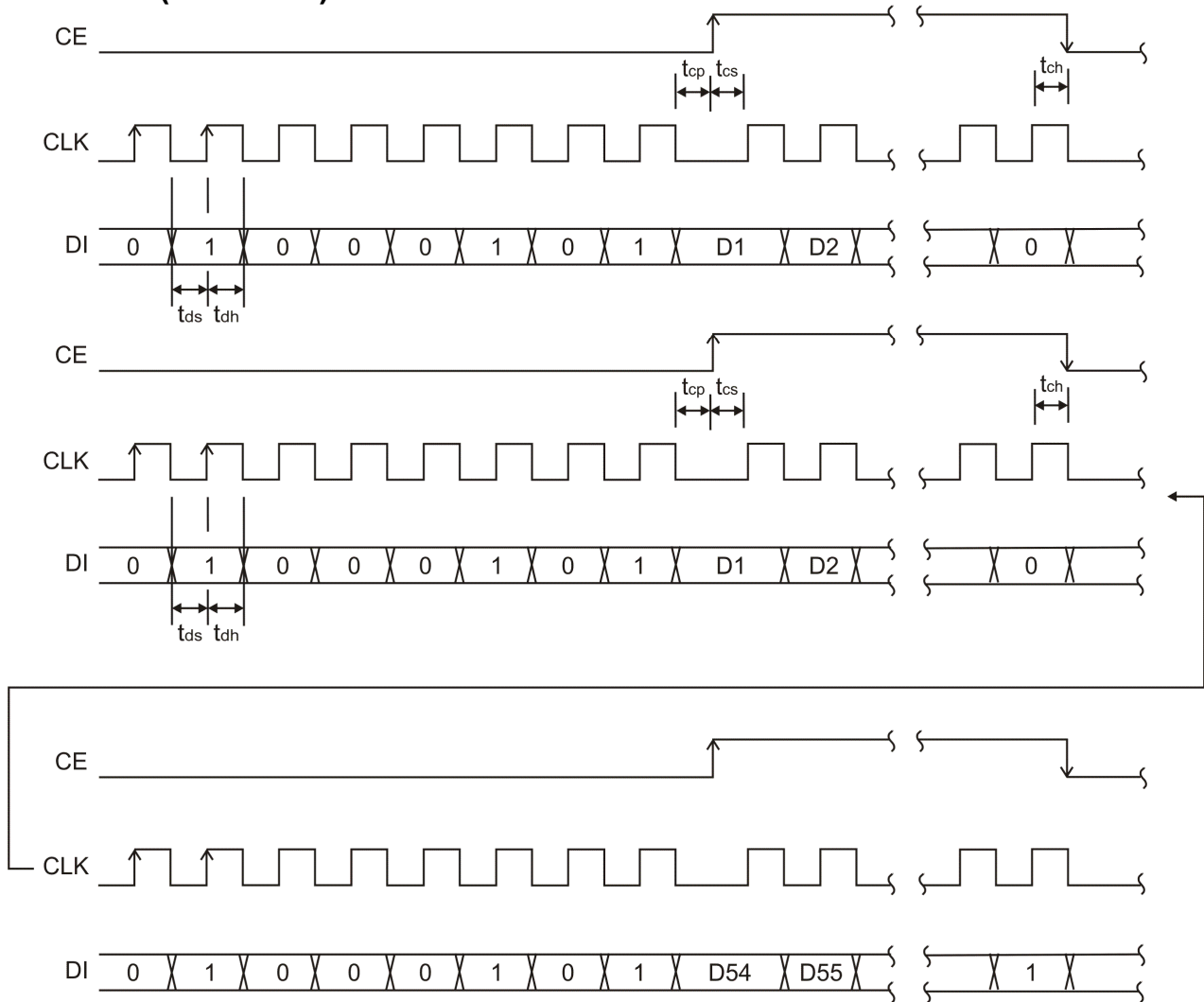


SERIAL DATA

1. STATIC DUTY (64 BITS)

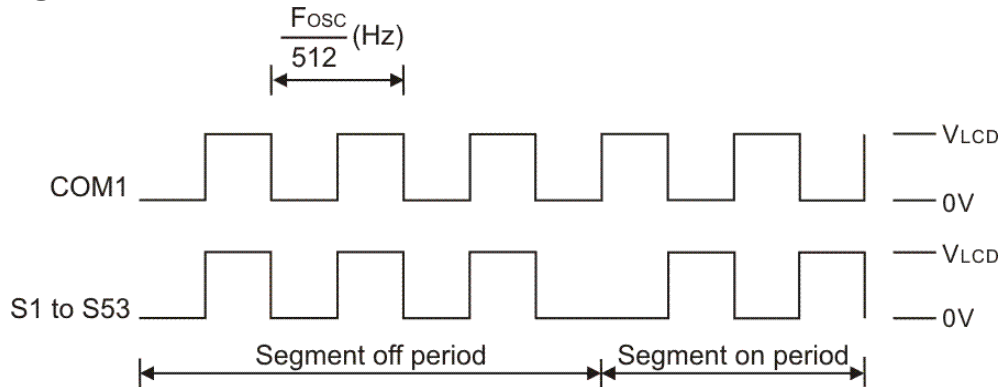


2. 1/2 DUTY (128 BITS)

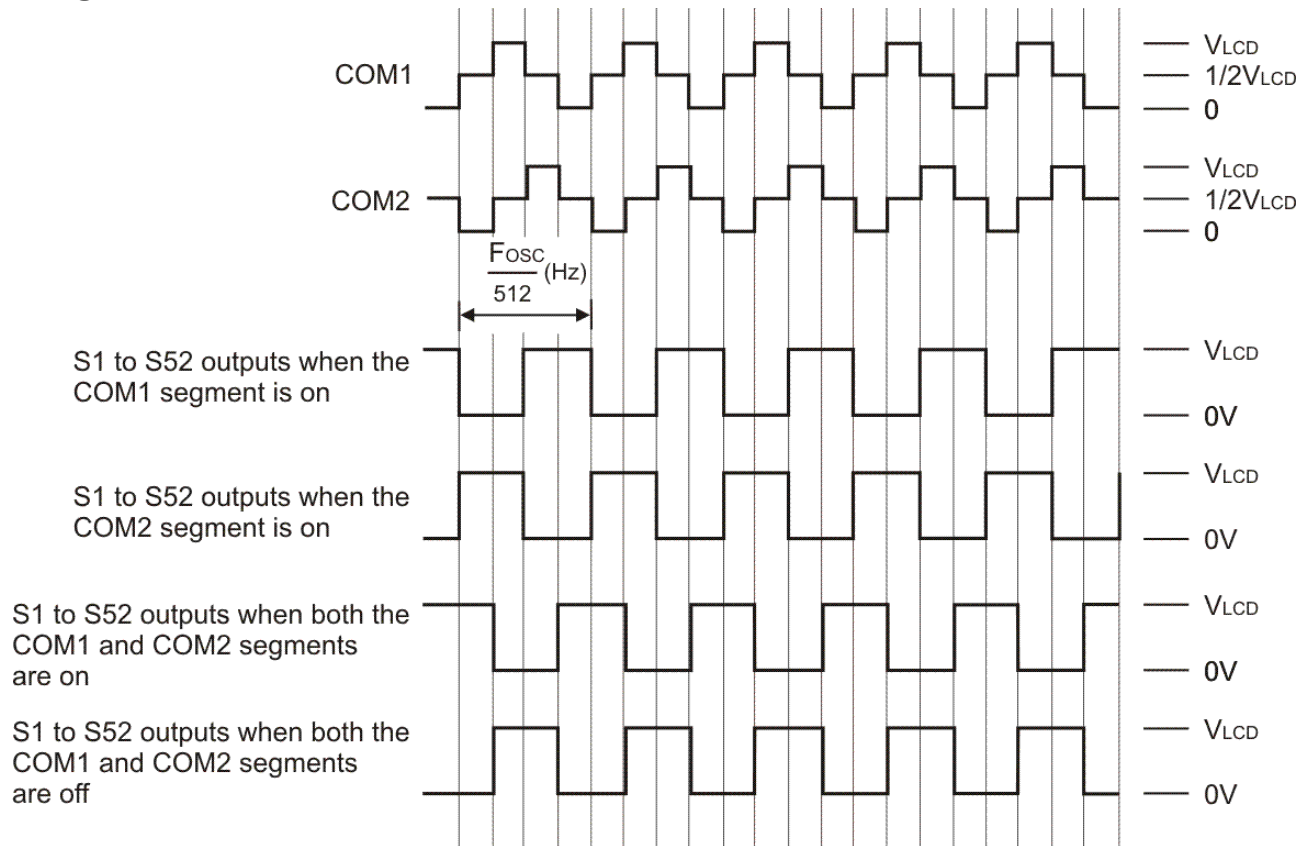


OUTPUT WAVEFORMS

1. STATIC DUTY



2. 1/2 DUTY



ABSOLUTE MAXIMUM RATINGS

 (Unless otherwise specified, $T_a=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VDDmax	VDD	-0.3 to +7.0	V
	VLCD	VLCD	-0.3 to VDD +0.3	V
Input voltage	VIN1	CE, CLK, DI, /INH	-0.3 to +7.0	V
	VIN2	OSC: output off	-0.3 to VDD +0.3	V
Output voltage	VOUT	OSC: output off	-0.3 to VDD +0.3	V
Output current	IOUT1	SG1 to SG53	100	μA
	IOUT2	COM1, COM2	1.0	mA
Allowable power dissipation	Pd max	$T_a=85^{\circ}\text{C}$	100	mW
Operating temperature	Topr	-	-40 to +85	$^{\circ}\text{C}$
Storage temperature	Tstg	-	-65 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS

 (Unless otherwise specified, $T_a=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$)

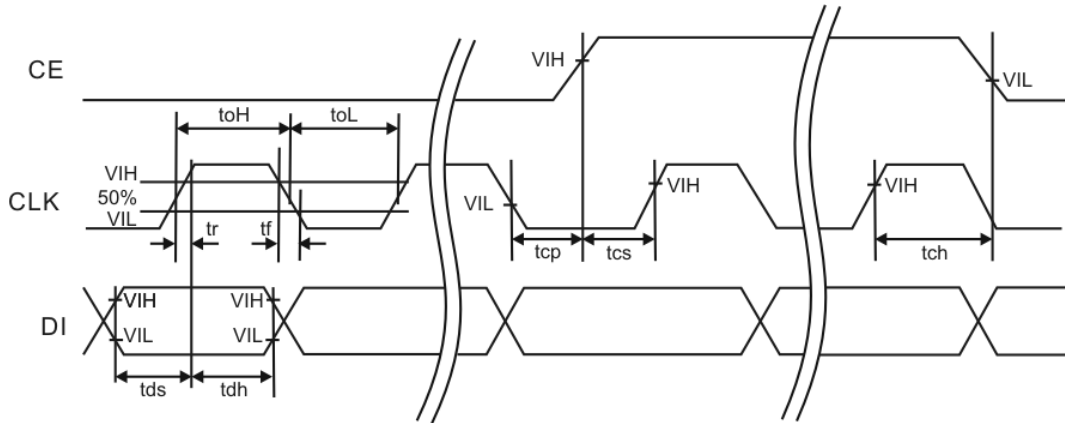
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level input current	I _{IH}	CE, CLK, DI, /INH: VDD	-	-	5	μA
Low-level input current	I _{IL}	CE, CLK, DI, /INH: VI=0V	-5	-	-	μA
High-level output voltage	VOH1	SG1 to SG53: IO=-10 μA	VLCD - 1.0	-	-	V
Low-level output voltage	VOL1	SG1 to SG53: IO=10 μA	-	-	1.0	V
High-level output voltage	VOH2	COM1, COM2: IO=-100 μA	VLCD - 0.6	-	-	V
Low-level output voltage	VOL2	COM1, COM2: IO=100 μA	-	-	0.6	V
Mid-level voltage	VMID1	COM1, COM2: VLCD=6.5V, IO= $\pm 100\mu\text{A}$	2.65	3.25	3.85	V
	VMID2	COM1, COM2: VLCD=3.0V, IO= $\pm 100\mu\text{A}$	0.9	1.5	2.1	V
Oscillator frequency	F _{OSC}	OSC: R=51K Ω , C=680pF	40	50	60	KHz
Hysteresis width	VH	CE, CLK, DI: VDD=5V	0.3	-	-	V
Supply current	IDD	VDD=5V, Output=open	-	-	0.5	mA
	ILCD	VLCD	-	-	2	mA

ALLOWABLE OPERATING RANGES

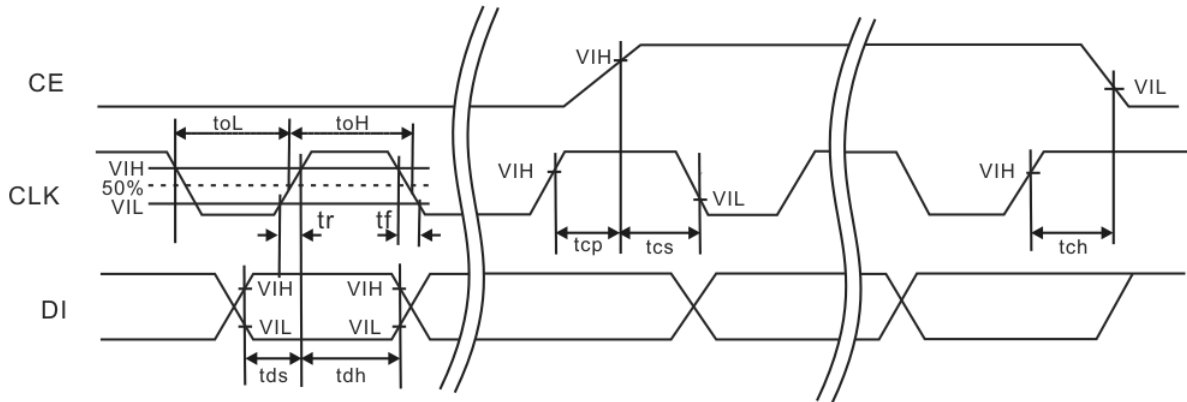
 (Unless otherwise specified, $T_a=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VDD	VDD	3.0	-	6.5	V
	VLCD	VLCD	3.0	-	VDD	V
High-level input voltage	VIH1	/INH	0.7 VDD	-	6.5	V
Low-level input voltage	VIL1	/INH	0	-	0.3 VDD	V
High-level input voltage	VIH2	CE, CLK, DI	0.8 VDD	-	6.5	V
Low-level input voltage	VIL2	CE, CLK, DI	0	-	0.2 VDD	V
Recommended external resistance	ROSC	OSC	-	51	-	K Ω
Recommended external capacitance	COSC	OSC	-	680	-	pF
Guaranteed oscillation range	F _{OSC}	OSC	25	50	100	KHz
Clock low-level pulse width (See figure)	toL	CLK	250	-	-	ns
Clock high-level pulse width (See figure)	toH	CLK	250	-	-	ns
Data setup time (See figure)	tds	CLK, DI	250	-	-	ns
Data hold time (See figure)	tdh	CLK, DI	250	-	-	ns
CE wait time (See figure)	tcp	CE, CLK	250	-	-	ns
CE setup time (See figure)	tcs	CE, CLK	250	-	-	ns
CE hold time (See figure)	tch	CE, CLK	250	-	-	ns

1. CLK IS TERMINATED AT “LOW” LEVEL



2. CLK IS TERMINATED AT “HIGH” LEVEL



Figure

TRANSFER (EXTERNAL INPUT) DATA/OUTPUT PIN CORRESPONDENCE

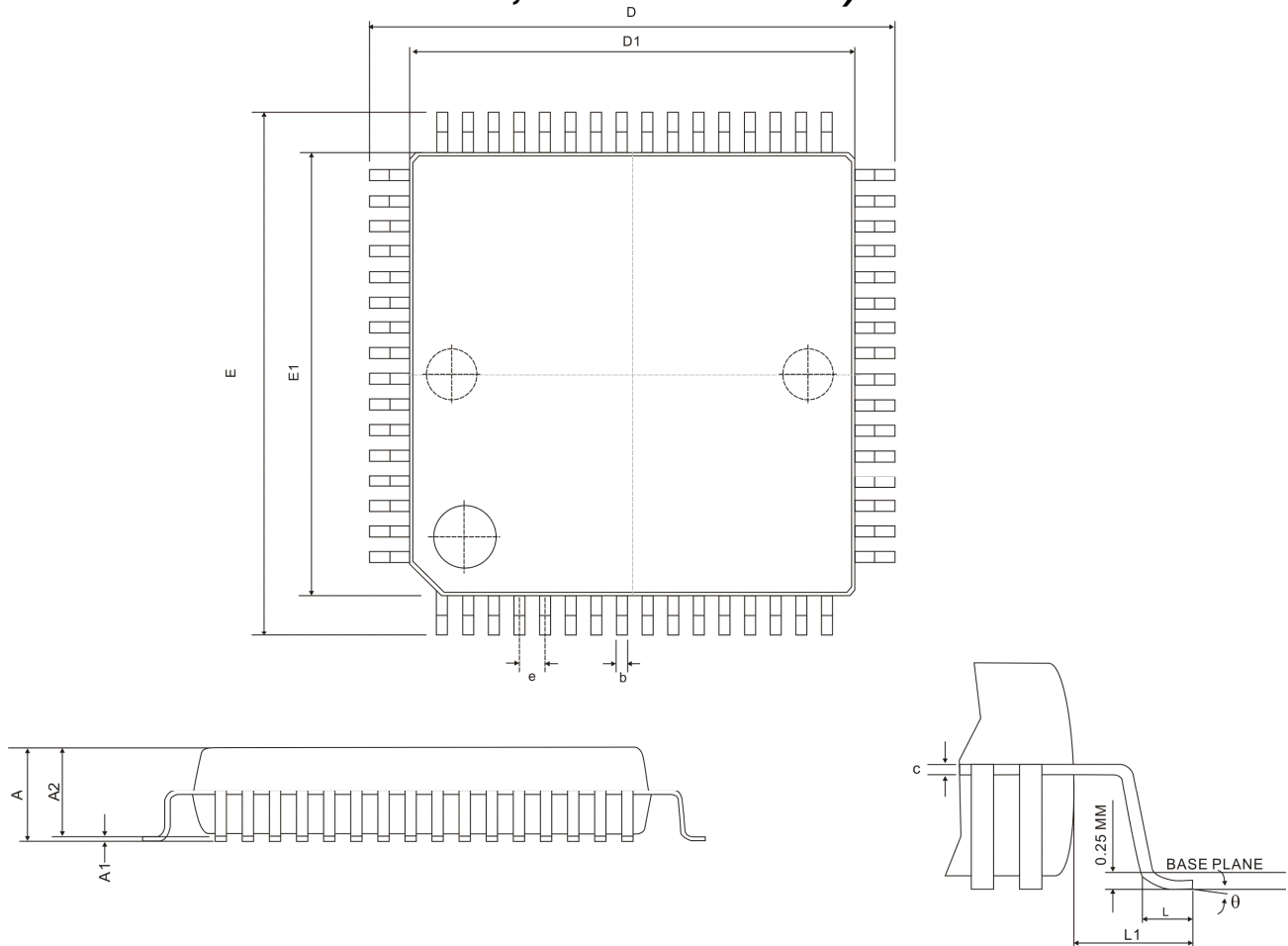
Note: Only COM1 is used in static (1/1 duty) drive.

Output Pin \ DP	0	1	COM1	COM2
	1/1 duty	1/2 duty		
SG1	D1	D1	○	
		D2		○
SG2	D2	D3	○	
		D4		○
SG3	D3	D5	○	
		D6		○
↓	↓	↓	↓	↓
SG26	D26	D51	○	
		D52		○
SG27	D27	D54	○	
		D55		○
SG28	D28	D56	○	
		D57		○
↓	↓	↓	↓	↓
SG43	D43	D86	○	
		D87		○
SG44	D44	D88	○	
		D89		○
SG45	D45	D90	○	
		D91		○
SG46	D46	D92	○	
		D93		○
SG47	D47	D94	○	
		D95		○
SG48	D48	D96	○	
		D97		○
SG49	D49	D98	○	
		D99		○
SG50	D50	D100	○	
		D101		○
SG51	D51	D102	○	
		D103		○
SG52	D52	D104	○	
		D105		○
SG53	D53	Always on	○	
		Always on		○

PACKAGE INFORMATION

64 PINS, QFP PACKAGE

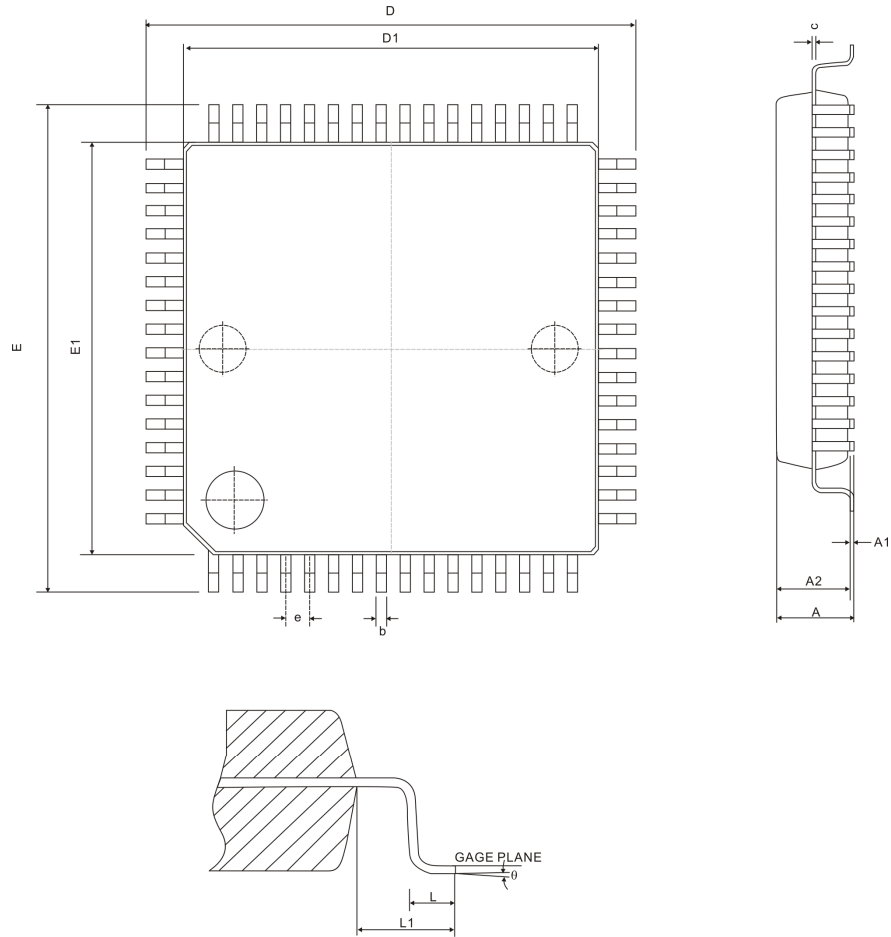
(BODY SIZE: 14mm x 14mm, PITCH: 0.80mm)



Symbol	Min.	Nom.	Max.
A	-	-	3.15
A1	0.00	-	0.25
A2	1.90	-	2.90
b	0.29	0.35	0.41
c	0.11	-	0.23
D	17.20 BSC		
D1	14.00 BSC		
E	17.20 BSC		
E1	14.00 BSC		
e	0.80 BSC		
L	0.65	-	1.05
L1	1.60 REF		
θ	0°	-	8°

Notes:
1. Refer to JEDEC MC-022BE
2. All dimensions are in millimeter.

64 PINS, LQFP PACKAGE
(BODY SIZE: 10mm x 10mm, THK BODY: 1.40mm)



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

- Notes:
1. All dimensions are in millimeter.
 2. Refer to JEDEC MS-026BCB

IMPORTANT NOTICE

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