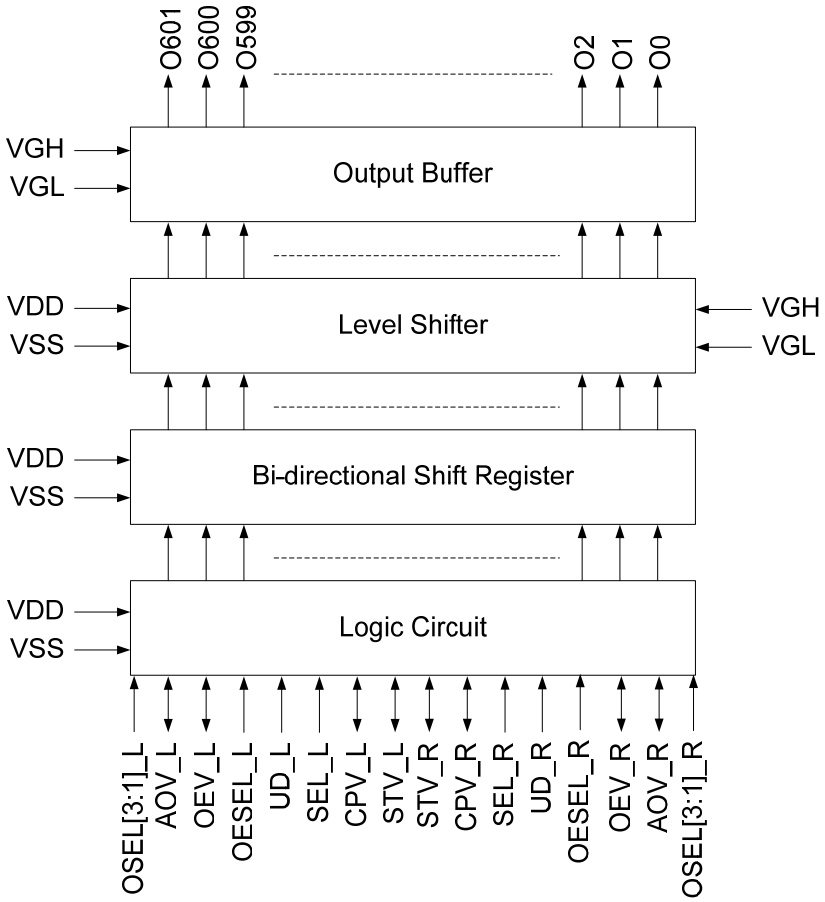
DESCRIPTION

The PT6003 is a CMOS silicon gate driver IC for active matrix TFT LCD panels. After a start pulse is triggered, this device will generate 2-level high voltage pulses on the outputs sequentially for driving the TFT LCD panel gate lines. It supports 600/576/540/525/512/480 channel selectable function, shift up/down selectable function, and cascade function for dot expansion.

FEATURES

- 2-level gate driver for active matrix TFT LCD panels
- Selectable 600/576/540/525/512/480 output ports
- Logic voltage power supply: 2.3V to 3.6V
- High voltage LCD gate line control signals at VGL + 40V maximum.
- Maximum operating frequency at 200KHz
- Bi-directional shift up/down function
- Power on reset function
- COF package

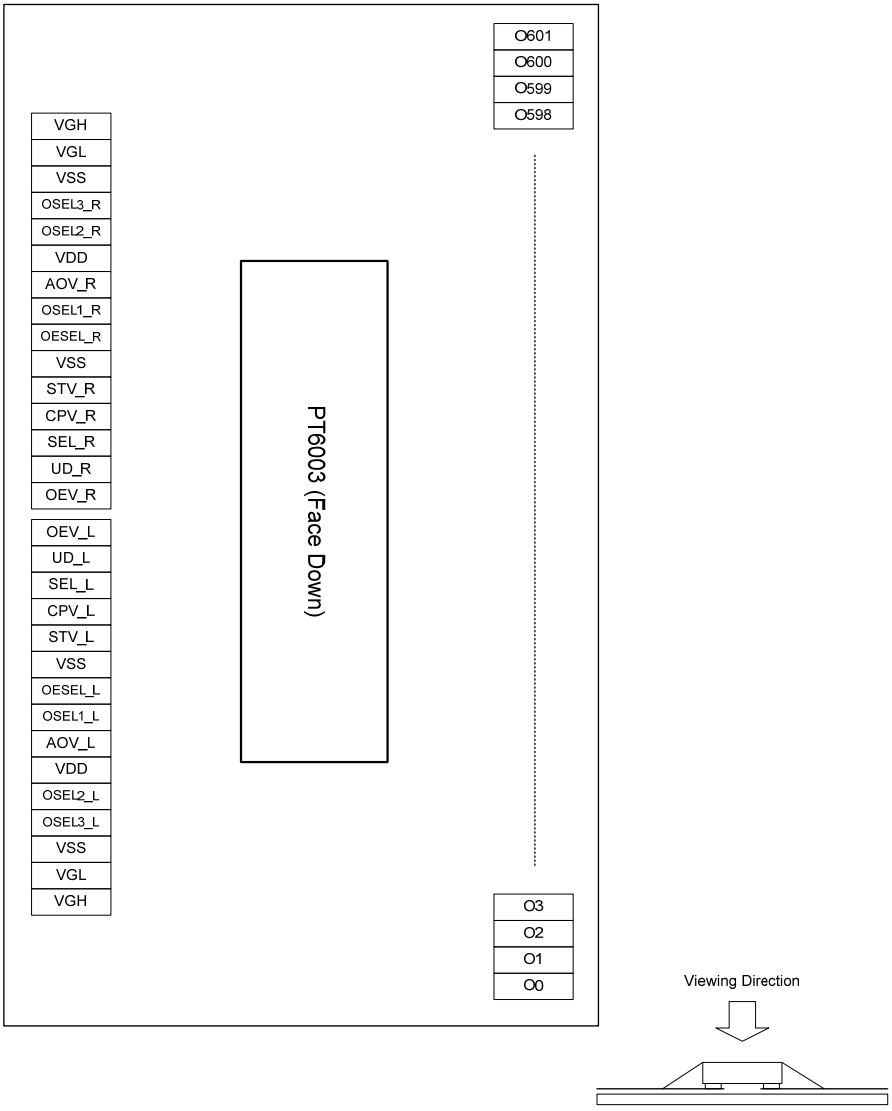
BLOCK DIAGRAM



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6003	COF	-

PIN CONFIGURATION



PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEL_R
SEL_L</td><td>I</td><td>SEL (SEL_R and SEL_L) determine the input/output direction of CPV, OEV and AOV (when left open, SEL=”H”).
<table>
<tr><th>SEL</th><th>Input</th><th>Output</th></tr>
<tr><td>H</td><td>CPV_L
OEV_L
AOV_L</td><td>CPV_R
OEV_R
AOV_R</td></tr>
<tr><td>L</td><td>CPV_R
OEV_R
AOV_R</td><td>CPV_L
OEV_L
AOV_L</td></tr>
</table></td></tr>
<tr><td>CPV_R
CPV_L</td><td>I/O</td><td>The shift register data is shifted on the rising edge of CPV (CPV_R and CPV_L).</td></tr>
<tr><td>STV_R
STV_L</td><td>I/O</td><td>When one of these terminals operates as input, the start pulse data is read at the rising edge of CPV.
When one of these terminals operates as output, the start pulse operates as the next chip’s start pulse input. The output pulse is generated at the falling edge of CPV.
Depending on UD, STV_R and STV_L become input or output.
<table>
<tr><th>UD</th><th>STV_L</th><th>STV_R</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>OSEL1_L
OSEL2_L
OSEL3_L
OSEL1_R
OSEL2_R
OSEL3_R</td><td>I</td><td>OSEL (OSEL1, OSEL2 and OSEL3) pins determine the number of output. (when left open, OSEL = ”H”)
<table>
<tr><th>OSEL1</th><th>OSEL2</th><th>OSEL3</th><th># of ch</th><th>Non-output Pin</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>600</td><td>No non-output pin</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>576</td><td>O289~O312 (Fixed to VGL)</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>540</td><td>O271~O330 (Fixed to VGL)</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>525</td><td>O263~O337 (Fixed to VGL)</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>512</td><td>O257~O344 (Fixed to VGL)</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>480</td><td>O241~O360 (Fixed to VGL)</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Reserved</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>UD_L
UD_R</td><td>I</td><td>Input with internal pull high to control the shift direction.
UD = ”H” (UD_L & UD_R): STV_L → O1 → … → O600 → STV_R
UD = ”L” (UD_L & UD_R): STV_R → O600 → … → O1 → STV_L</td></tr>
<tr><td>OEV_L
OEV_R</td><td>I/O</td><td>Output enable pin. These pins control O1 to O600 outputs to VGL state. OEV (OEV_R & OEV_L) is not synchronous to CPV.</td></tr>
<tr><td>OESEL_L
OESEL_R</td><td>I</td><td>Input pin to select the OEV (OEV_R and OEV_L) active state. Internal pull high.
OESEL = “L”: OEV is active high, i.e., when OEV is high then O1 to O600 output VGL.
OESEL = “H”: OEV is active low, i.e., when OEV is low then O1 to O600 output VGL.</td></tr>
<tr><td>AOV_L
AOV_R</td><td>I/O</td><td>When AOV=”L” (AOV_R & AOV_L), O1 to O600 are driven to VGH. AOV is not synchronous to CPV, and has higher priority over OEV. Internal pull high.</td></tr>
<tr><td>O1 ~ O600</td><td>O</td><td>The output for LCD drives data which are level-shifted from shift registers.</td></tr>
<tr><td>O0, O601</td><td>O</td><td>These pins output VGL level regardless of shift data.</td></tr>
<tr><td>VGH</td><td>P</td><td>Power supply for high voltage circuits and high level voltage supply for LCD control.</td></tr>
<tr><td>VGL</td><td>P</td><td>Ground for high voltage circuits and low level voltage supply for LCD control.</td></tr>
<tr><td>VDD</td><td>P</td><td>Power supply for logic circuits.</td></tr>
<tr><td>VSS</td><td>P</td><td>Ground for logic circuits.</td></tr>
</table>

IMPORTANT NOTICE

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