DESCRIPTION

The PT6001 is a CMOS silicon gate driver IC for active matrix TFT LCD panels. After a start pulse is triggered, this device will generate 2-level high voltage pulses on the outputs sequentially for driving the LCD panel gate lines. It supports 200/240/256/263/270 channel selectable function, shift up/down selectable function, and cascade function for dot expansion.

This device can be used to implement XGA/SXGA/WXGA/SXGA+/WXGA+ and other resolutions panels.

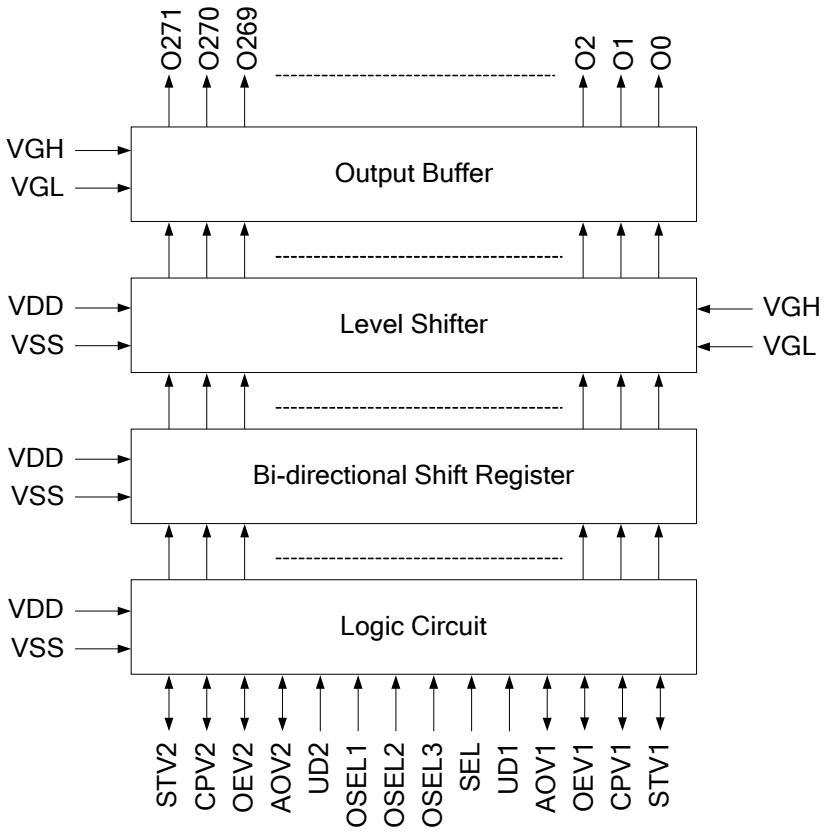
FEATURES

- 2-level gate driver for active matrix TFT LCD panels
- Selectable 200/240/256/263/270 output ports
- Logic voltage power supply: 2.3V to 4.2V
- High voltage LCD gate line control signals at VGL + 45V maximum.
- Maximum operating frequency at 200KHz
- Bi-directional shift up/down function
- Power on reset function
- AOV (All-On) function
- PCB-less applications
- COF package

APPLICATION

- Game console

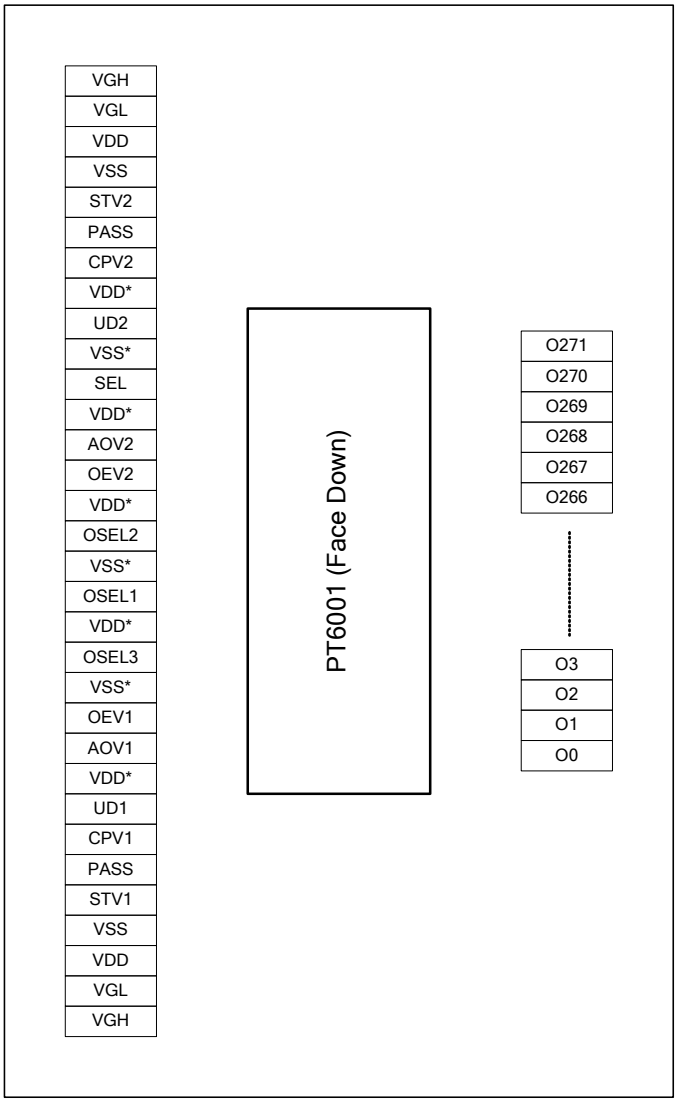
BLOCK DIAGRAM

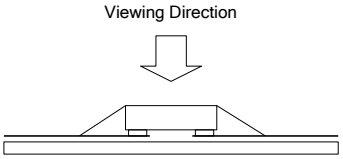


ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6001	COF	-

PIN ASSIGNMENT





PIN DESCRIPTION

<table>
<tr><th>Symbol</th><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEL</td><td>Input/Output selection</td><td>I</td><td>SEL determine the input/output direction of CPV, UD, OEV and AOV (when left open, SEL=”L”). Although SEL is internally pulled dwon, be sure to connect SEL to VSS when the input of this pin is fixed to “L”.
<table>
<tr><th>SEL</th><th>Input</th><th>Output</th></tr>
<tr><td>H</td><td>CPV1
UD1
OEV1
AOV1</td><td>CPV2
UD2
OEV2
AOV2</td></tr>
<tr><td>L</td><td>CPV2
UD2
OEV2
AOV2</td><td>CPV1
UD1
OEV1
AOV1</td></tr>
</table></td></tr>
<tr><td>CPV1
CPV2</td><td>Shift clock</td><td>I/O</td><td>The shift register data is shifted on the rising edge of CPV.</td></tr>
<tr><td>STV1
STV2</td><td>Shift data input/output</td><td>I/O</td><td>When one of these terminals operates as input, the start pulse data is read at the rising edge of CPV.
When one of these terminals operates as output, the start pulse operates as the next chip’s start pulse input. The output pulse is generated at the falling edge of CPV.
Depending on UD, STV1 and STV2 become input or output.
<table>
<tr><th>UD</th><th>STV1</th><th>STV2</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>OSEL1
OSEL2
OSEL3</td><td>Output channel selection</td><td>I</td><td>OSEL pins determine the number of output. (when left open, OSEL=”L”)
Although OSEL is internally pulled down, be sure to connect OSEL to VSS when the input of this pin is fixed to “L”.
<table>
<tr><th>OSEL1</th><th>OSEL2</th><th>OSEL3</th><th># of ch</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>200</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>240</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>256</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>263</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>270</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>Invalid</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>Invalid</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>Invalid</td></tr>
</table></td></tr>
<tr><td>UD1
UD2</td><td>Shift direction control</td><td>I/O</td><td>UD=”H”: STV1 → O1 → … → O270 → STV2
UD=”L”: STV2 → O270 → … → O1 → STV1
(when left open, UD=”L”) Although UD is internally pulled down, be sure to connect UD to VSS when the input of this pin is fixed to “L”.</td></tr>
<tr><td>OEV1
OEV2</td><td>Output enable</td><td>I/O</td><td>When OEV=”H”, O1 to O270 are driven to VGL. OEV is not synchronized to CPV.</td></tr>
<tr><td>AOV1
AOV2</td><td>All output-on</td><td>I/O</td><td>When AOV=”L”, O1 to O270 are driven to VGH. AOV is not synchronized to CPV, and has higher priority over OEV. (when left open, AOV=”H”) Although AOV is internally pulled up, be sure to connect AOV to VDD when the input of this pin is fixed to “H”.
This function shall be used when the power is turned off.</td></tr>
</table>

Symbol	Pin Name	I/O	Description
O1 ~ O270	LCD driving output	O	The output for LCD drives data which are level-shifted from shift registers.
O0, O271	LCD auxiliary driving output	O	These pins output VGL level regardless of shift data.
VGH	LCD power supply 1	P	Power supply for high voltage circuits and high level voltage supply for LCD control.
VGL	LCD power supply 2	P	Ground for high voltage circuits and low level voltage supply for LCD control.
VDD	Logic power supply 1	P	Power supply for logic circuits.
VSS	Logic power supply 2	P	Ground for logic circuits.
VDD*	VDD output	O	VDD output.
VSS*	VSS output	O	VSS output
PASS	Pass signal	-	Signal pass through the device.

IMPORTANT NOTICE

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