

DESCRIPTION

RS2259 combines a dedicated current mode PWM controller with a high voltage power MOSFET. It is optimized for high performance, low standby power, and cost effective off-line flyback converter applications in sub 27W range.

RS2259 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VDD over voltage clamp and under voltage lockout (UVLO). Excellent EMI performance is achieved with Orister proprietary frequency Jiggling technique together with soft switching control at the totem pole gate drive output. The tone energy at below 20KHz is minimized in the design and audio noise is eliminated during operation. RS2259 is offered in DIP-8 package.

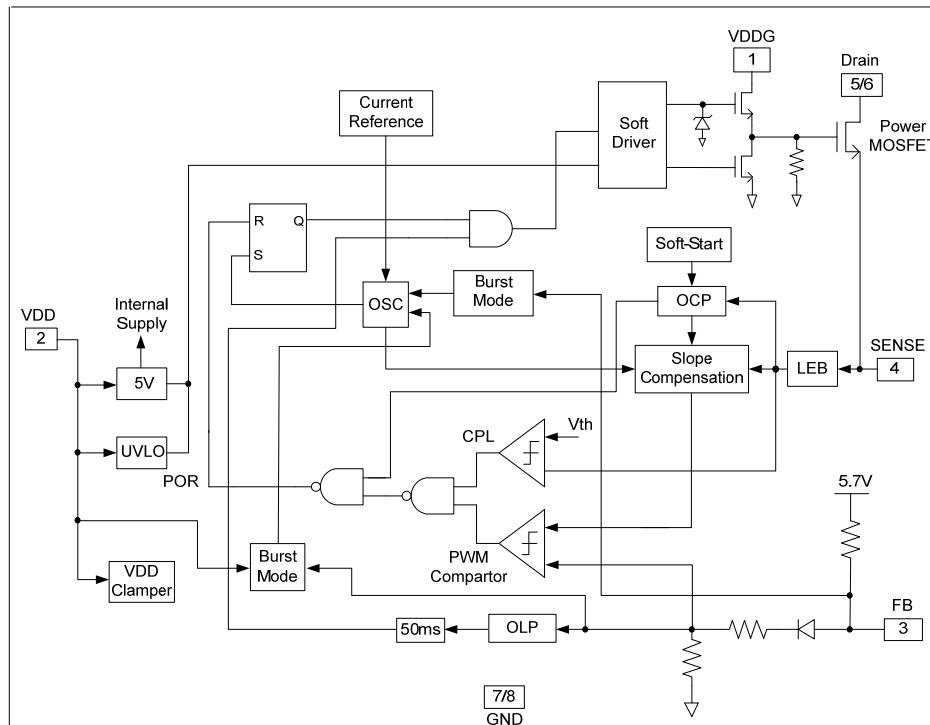
APPLICATIONS

- Battery Charger
- Digital Cameras and camcorder Adaptor
- PDA power supplies
- VCR, SVR, STB, DVD & DVCD Player SMPS
- Set-Top Box (STB) Power
- Auxiliary Power Supply for PC and Server
- Open-frame SMPS

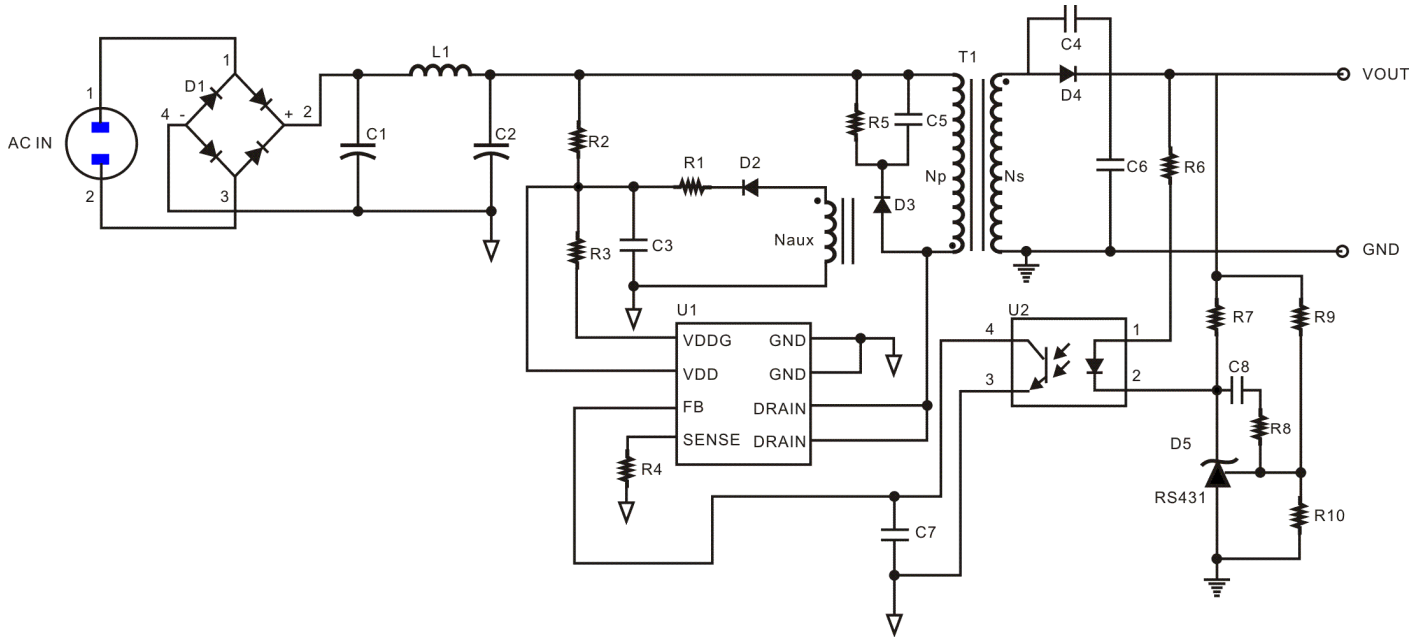
FEATURES

- Power on Soft Start Reducing MOSFET VDS Stress
- Frequency Jiggling to reduce EMI
- Burst Mode Control For Improved Efficiency and Minimum Standby power Design
- Audio Noise Free Operation
- Fixed 50KHz Switching Frequency
- Internal Synchronized Slope Compensation
- Low VDD Startup Current and Low Operating Current
- Leading Edge Blanking on Current Sense Input
- Good Protection Coverage With Auto Self-Recovery
 - VDD Over Voltage Clamp and Under Voltage Lockout with Hysteresis (UVLO)
 - Line Input Compensated Cycle-by-Cycle Over-current Threshold Setting For Constant Output Power Limiting Over Universal Input Voltage Range
 - Overload Protection (OLP)
 - Over Voltage Protection (OVP)
- DIP-8 Package
- RoHS Compliant and 100% Lead (Pb)-Free and Green (Halogen Free with Commercial Standard)

BLOCK DIAGRAM



APPLICATION CIRCUIT

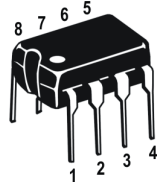


ORDER INFORMATION

Device	Device Code
RS2259 Y Z	<p>Y is package designator : P: DIP-8</p> <p>Z is Lead Free designator : P: Commercial Standard, Lead (Pb) Free and Phosphorous (P) Free Package G: Green (Halogen Free with Commercial Standard).</p>

PIN ASSIGNMENTS

DIP-8



PIN DESCRIPTION

Pin Name	Description	Pin No.
VDDG	Internal Gate Driver Power Supply Pin	1
VDD	DC Power Supply Input Pin	2
FB	Feedback input Pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 4	3
SENSE	Current Sense Input Pin	4
DRAIN	HV MOSFET Drain Pin. The Drain pin is connected to the primary lead of the transformer	5, 6
GND	Ground Pin	7, 8

FUNCTION DESCRIPTION

The RS2259 is a low power off-line SMPS Switcher optimized for off-line flyback converter applications in sub 10W power range. The burst mode control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

STARTUP CURRENT AND START UP CONTROL

Startup current of RS2259 is designed to be very low so that V_{DD} could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application. For AC/DC adaptor with universal input range design, a $2M\Omega$, 1/8W startup resistor could be used together with a V_{DD} capacitor to provide a fast startup and yet low power dissipation design solution.

OPERATION CURRENT

The Operation current of RS2259 is low at 2mA. Good efficient is achieved with RS2259 low operating current together with the 'Extended burst mode' control features.

SOFT START

RS2259 features an internal 4 ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as V_{DD} reaches UVLO(OFF), the peak current is gradually increased from nearly zero to the maximum level of 0.77V. Every restart up is followed by a soft start.

FREQUENCY JIGGLING MODE FOR EMI IMPROVEMENT

The frequency Jiggling Mode (switching frequency modulation) is implemented in RS2259. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

EXTENDED BURST MODE OPERATION

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below burst mode threshold level and device enters Burst Mode control. The Gate drive output switches only when V_{DD} voltage drops below a preset level and FB input is active to output an on state to minimize the switching loss and reduce the standby power consumption to the greatest extend.

The switching frequency control also eliminates the audio noise at any loading conditions.

OSCILLATOR OPERATION

The switching frequency of RS2259 is internally fixed at 50 KHz. No external frequency setting components are required for PCB design simplification.

CURRENT SENSING AND LEADING EDGE BLANKING

Cycle-by-Cycle current limiting is offered in RS2259 current mode PWM control. The switch current is detected by sense resistor into the sense pin. An internal leading edge blank circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of internal power MOSFET so that the external RC filtering on sense input is no longer needed. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

INTERNAL SYNCHRONIZED SLOPE COMPENSATION

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

DRIVE

The internal power MOSFET in RS2259 is driven by a dedicated gate driver for power switch control. Too weak the gate driving strength results in higher conduction and switch loss of MOSFET while too strong gate drive results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

In addition to the gate drive control scheme mentioned, the gate drive strength can also be adjusted externally by a resistor connected between V_{DD} and V_{DDG} , the falling edge of the Drain output can be well controlled. It provides great flexibility for system EMI design.

PROTECTION CONTROLS

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO).

With PTC, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition when FB input voltage exceeds power limit threshold value for more than T_{D_PL} , control circuit reacts to shut down the switcher. Switcher restarts when V_{DD} voltage drops below UVLO limit.

V_{DD} is supplied by transformer auxiliary winding output. It is clamped when V_{DD} is higher than 30V. The output of RS2259 is shut down when V_{DD} drops below UVLO(ON) limit and Switcher enters power on start-up sequence thereafter.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Range	Units
Drain Voltage (off state)	V_{DRAIN}	-0.3 to 650	V
VDD Voltage	V_{DD}	-0.3 to 30	V
VDDG Input Voltage	$V_{DDG IN}$	-03 to 30	V
VDD Clamp Continuous Current	$I_{VDD CLAMP}$	10	mA
FB Input Voltage	$V_{FB IN}$	-0.3 to 7	V
Sense Input Voltage	$V_{SENSE IN}$	-0.3 to 7	V
Operating Ambient Temperature	T_{OPR}	-40 to +85	°C
Storage Temperature	T_{STG}	-40 to +150	°C
Lead Temperature (soldering, 10sec)	-	+260	°C
ESD Voltage Protection, Human Body Model	-	2	KV
ESD Voltage Protection, Machine Model	-	200	V

Notes:

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and function operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. Caution: Stress above the listed absolute maximum rating may cause permanent damage to the device. * HBM B: 2000V to 3999V

OUTPUT POWER TABLE

DIP-8 Package	
230VAC ± 15%	85 to 265VAC
Open Frame ^(Note)	Open Frame ^(Note)
28W	24W

Note: Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sink, at 50°C ambient.

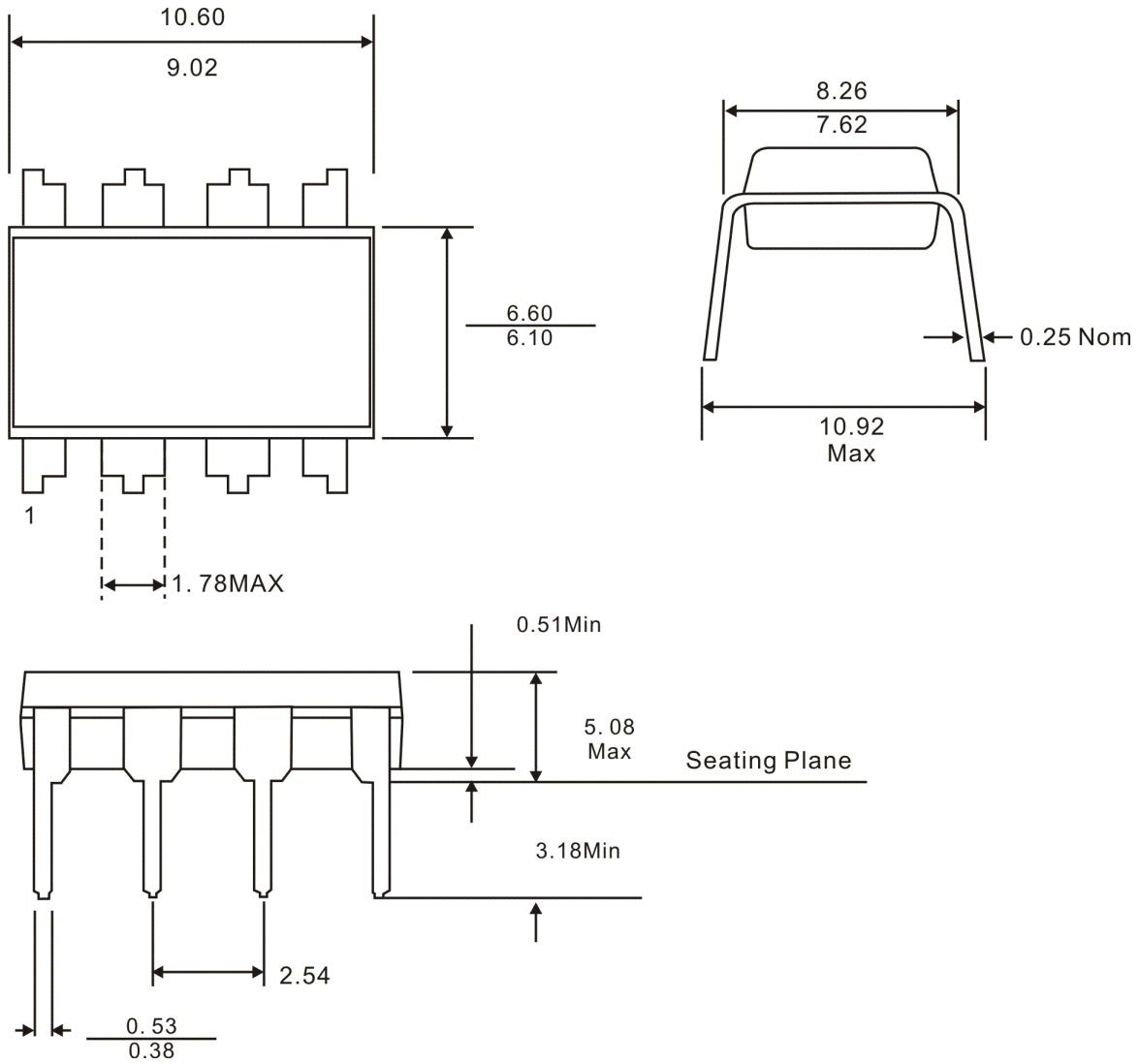
ELECTRICAL CHARACTERISTICS

 ($V_{DD}=16V$, $T_A=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD})						
V_{DD} Start up Current	$I_{startup}$	$V_{DD}=14.5V$, Measure Leakage current into V_{DD}	-	3	20	μA
Operation Current	I_{VDD}	$V_{FB}=3V$	-	2.0	-	mA
VDD Under Voltage Lockout Enter	UVLO(ON)	-	14.2	15.8	16.0	V
V_{DD} Under Voltage Lockout Exit (Recovery)	UVLO(OFF)	-	8.5	9.0	9.5	V
Over Voltage Protection Voltage	OVP(ON)	CS=0V, FB=3V Ramp up V_{DD} until gate clock is off	27.0	28.5	30.0	V
V_{DD} Zener Clamp Voltage	V_{DD_CLAMP}	$I_{DD}=10mA$	-	30	-	V
Feedback Input Section(FB pin)						
V_{FB} Open Loop Voltage	V_{FB_OPEN}	-	5.4	5.6	6.0	V
FB Pin Short Circuit Current	I_{FB_SHORT}	Short FB pin to GND and measure current	-	1.55	-	mA
Zero Duty Cycle FB Threshold Voltage	V_{TH_0D}	-	-	0.8	-	V
Power Limiting FB Threshold Voltage	V_{TH_PL}	-	-	3.7	-	V
Power Limiting Debounce Time	T_{D_PL}	-	-	50	-	ms
Input Impedance	Z_{FB_IN}	-	-	4	-	K Ω
Current Sense Input(Sense Pin)						
Soft Start Time	$T_{SOFTSTART}$	-	-	4	-	ms
Leading Edge Blanking Time	$T_{BLANKING}$	-	-	300	-	ns
Input Impedance	Z_{SENSE_IN}	-	-	40	-	K Ω
Over Current Detection and Control Delay	T_{D_OC}	From Over Current Occurs till the Gate drive output start to turn off	-	120	-	ns
Internal Current Limiting Threshold Voltage	V_{TH_OC}	FB=3.3V	0.76	0.8	0.82	V
Oscillator						
Normal Oscillation Frequency	F_{OSC}	-	45	50	55	KHz
Frequency Temperature Stability	ΔF_{TEMP}	-	-	5	-	%
Frequency Voltage Stability	ΔF_{VDD}	-	-	5	-	%
Maximum Duty Cycle	D_{MAX}	FB=3.3V, CS=0V	70	80	90	%
Burst Mode Base Frequency	F_{BURST}	-	-	22	-	KHz
Power MOSFET Section						
MOSFET Drain Source Breakdown Voltage	B_V_{DSS}	-	-	650	-	V
Static Drain to Source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V$, $I_{DS}=1A$	-	2.0	2.5	Ω
Frequency						
Frequency Modulation Range/Base Frequency	ΔF_{VDD}	-	-4	-	4	%

PACKAGE INFORMATION

8 PINS, DIP



Notes:

1. All dimensions are in millimeters.
2. Refer to JEDEC MS-001



IMPORTANT NOTICE

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