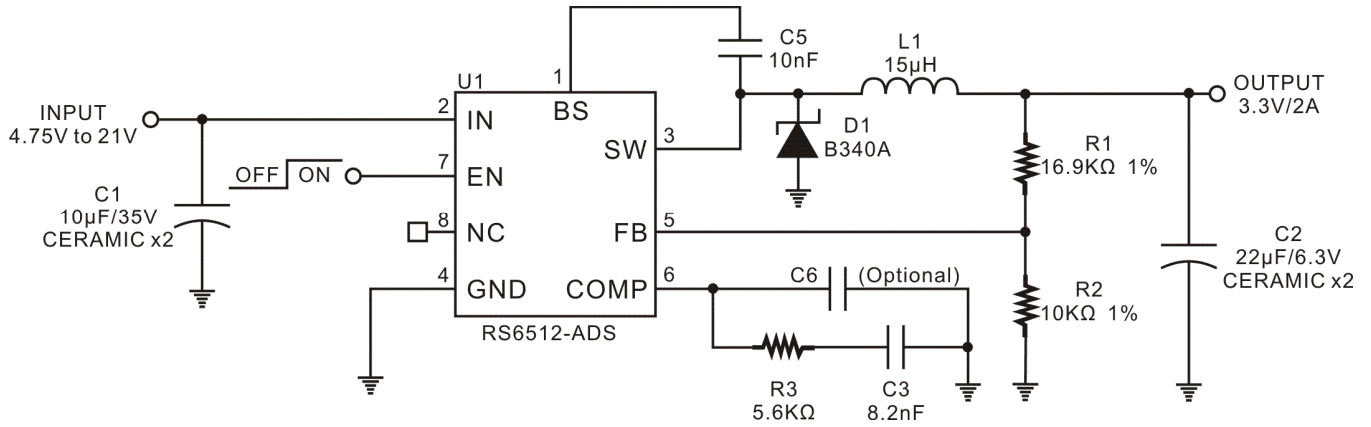


APPLICATION CIRCUIT

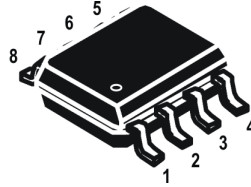


ORDER INFORMATION

Device	Device Code
RS6512-XX Y Z	<p>XX is nominal output voltage: AD: ADJ</p> <p>Y is package & Pin Assignments designator: S: SOP-8</p> <p>Z is Lead Free designator: P: Commercial Standard, Lead (Pb) Free and Phosphorous (P) Free Package G: Green (Halogen Free with Commercial Standard)</p>

PIN ASSIGNMENTS

SOP-8



PIN DESCRIPTION

Pin Name	Description	Pin No.
BS	Bootstrap. This capacitor (C5) is needed to drive the power switch's gate above the supply voltage. It is connected between the SW and BS pins to form a floating supply across the power switch driver. The voltage across C5 is about 5V and is supplied by the internal +5V supply when the SW pin voltage is low.	1
IN	Supply Voltage. The RS6512 operates from a 4.75V to 20V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.	2
SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.	3
GND	Ground.	4
FB	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider from the output voltage to ground. The feedback threshold is 1.23V. See Setting the Output Voltage.	5
COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required. See Compensation.	6
EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. For automatic startup, leave EN unconnected.	7
NC	No internal connection.	8

FUNCTION DESCRIPTION

The RS6512 is a synchronous high voltage buck converter that can support the input voltage range from 4.75V to 20V and the output current can be up to 2A.

OUTPUT VOLTAGE SETTING

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

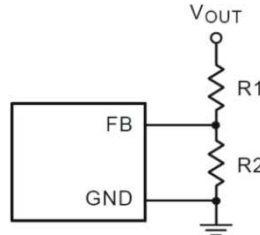


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{FB} \left(1 + \frac{R1}{R2} \right)$$

Where V_{FB} is the feedback reference voltage(1.23V typ.).

EXTERNAL BOOTSTRAP DIODE

Connect a 10nF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and the BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65%. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

INDUCTOR SELECTION

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L} \right] \times \left[1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.2375(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN} . To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_L(MAX)} \right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

INDUCTOR CORE SELECTION

The inductor type must be selected once the value for L is known. Generally speaking, high efficiency converters can not afford the core loss found in low cost powdered iron cores. So, the more expensive ferrite or mollypermalloy cores will be a better choice.

The selected inductance rather than the core size for a fixed inductor value is the key for actual core loss. As the inductance increases, core losses decrease. Unfortunately, increase of the inductance requires more turns of wire and therefore the copper losses will increase.

Ferrite designs are preferred at high switching frequency due to the characteristics of very low core losses. So, design goals can focus on the reduction of copper loss and the saturation prevention. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. The previous situation results in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate! Different core materials and shapes will change the size/current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate energy. However, they are usually more expensive than the similar powdered iron inductors. The rule for inductor choice mainly depends on the price vs. size requirement and any radiated field/EMI requirements.

C_{IN} AND C_{OUT} SELECTION

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN} = 2V_{OUT}, where I_{RMS} = I_{OUT}/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor, a 10μF x 2 low ESR ceramic capacitor is recommended. For the recommended capacitor, please refer to table 3 for more detail. The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta L \times \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since ΔL increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies.

Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for

ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN} . At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

OUTPUT RECTIFIER DIODE

The output rectifier diode supplies the current to the inductor when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, use a Schottky diode.

Choose a diode whose maximum reverse voltage rating is greater than the maximum input voltage, and whose current rating is greater than the maximum load current.

Choose a rectifier who's maximum reverse voltage rating is greater than the maximum input voltage, and who's current rating is greater than the maximum load current.

CHECKING TRANSIENT RESPONSE

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} (ESR)$ also begins to charge or discharge C_{OUT} generating a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Component Supplier	Series	Dimensions (mm)
MAGLAYERS	MSCDRI-124-150M	12 x 12 x 5.0
SUMIDA	CDRH104R	10.1 x 10 x 3.0
TOKO	D104C	10 x 10 x 4.3

Table 1. Suggested Inductors for Typical Application Circuit

Component Supplier	Part No.	Capacitance (μF)	Case Size
MURATA	GRM31CR61E106K	10	1206
TDK	C3225X5R1E106K	10	1206
MURATA	GRM32ER71C226M	22	1200
TDK	C3225X5R1C226M	22	1200

Table 2. Suggested Capacitors for C_{IN} and C_{OUT}

V_{IN} (Max.)	2A Load Current	
	Part No.	Vendor
20V	B320	Diodes, Inc. (www.diodes.com)
	SK33	Pan Jit International (www.panjit.com.tw)
	SS32	General Semiconductor (www.gensemi.com)

Table 3. Schottky Rectifier Selection Guide

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Range	Units
Supply Voltage	V_{IN}	-0.3 to +21	V
SW Pin Voltage	V_{SW}	-0.3 to $V_{IN} + 0.3$	V
Boot Strap Voltage	V_{BS}	$V_{SW} - 0.3$ to $V_{SW} + 6$	V
Feedback Voltage	V_{FB}	-0.3 to +6	V
Enable/UVLO Voltage	V_{EN}	-0.3 to +6	V
Comp Voltage	V_{COMP}	-0.3 to +6	V
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_{OPR}	-20 to +85	°C
Storage Temperature Range	T_{STG}	-40 to +150	°C
Lead Temperature	T_{LEAD}	260	°C

ELECTRICAL CHARACTERISTICS

($V_{IN} = 12V$, $T_A = 25^\circ C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}	-	4.75	-	20	V
Feedback Voltage	V_{FB}	$4.75V \leq V_{IN} \leq 20V$	1.19	1.23	1.26	V
Upper Switch On Resistance	$R_{DS(ON)1}$	-	-	0.22	-	Ω
Lower Switch On Resistance	$R_{DS(ON)2}$	-	-	10	-	Ω
Upper Switch Leakage	I_{SW}	$V_{EN} = 0V, V_{SW} = 0V$	-	-	10	μA
Current Limit ^(NOTE 1)	I_{LIM}	-	-	3.8	-	A
Current Sense Transconductance Output Current to Comp Pin Voltage	G_{CS}	-	-	1.95	-	A/V
Error Amplifier Voltage Gain	A_{VEA}	-	-	400	-	V/V
Error Amplifier Transconductance	G_{EA}	-	550	830	1150	$\mu A / V$
Oscillator Frequency	F_S	-	-	400	-	KHz
Short Circuit Frequency	F_{OSC1}	$V_{FB} = 0V$	-	240	-	KHz
Maximum Duty Cycle	D_{MAX}	$V_{FB} = 1.0V$	-	90	-	%
Minimum On Time	t_{ON}	-	-	100	-	ns
EN Shutdown Threshold	-	$I_{CC} > 100\mu A$	0.7	1.0	1.3	V
Enable Pull Up Current	-	$V_{EN} = 0V$	-	1.0	-	μA
EN UVLO Threshold Rising	-	V_{IN} Rising	2.35	2.50	2.65	V
EN UVLO Threshold Hysteresis	-	-	-	200	-	mV
Supply Current (Shutdown)	I_{SD}	$V_{IN} \leq 0.4V$	-	23	36	μA
Supply Current (Quiescent)	I_Q	$V_{EN} \geq 3V$	-	1.1	1.3	mA
Thermal Shutdown	T_{SD}	-	-	160	-	°C

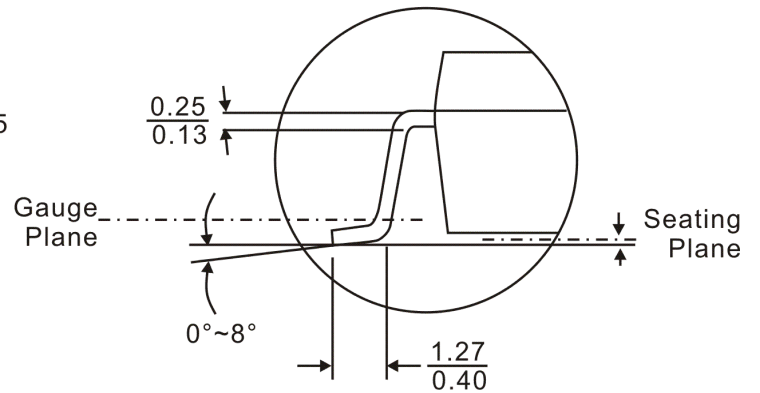
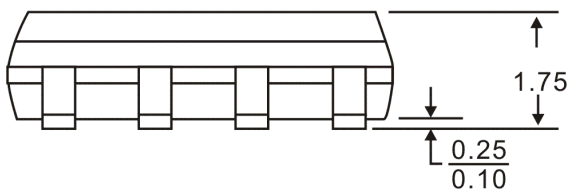
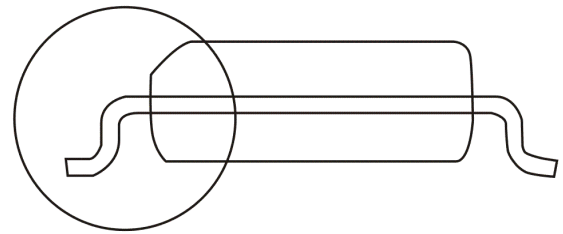
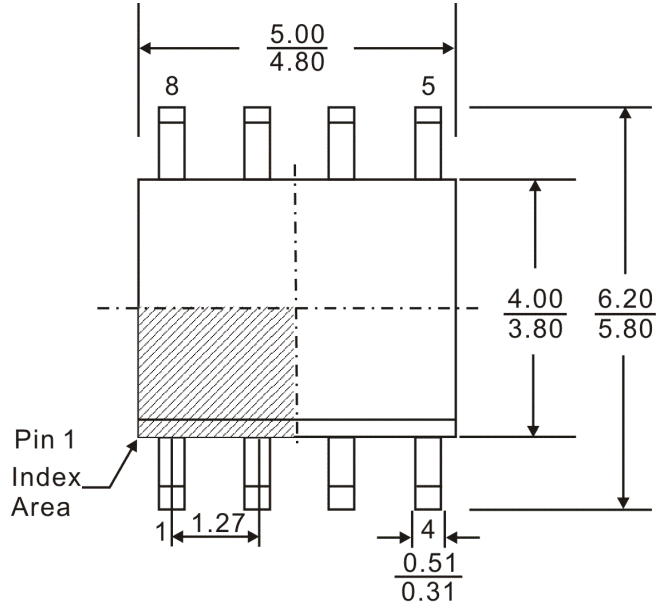
Notes:

- Slope compensation changes current limit above 40% duty cycle.
- Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
- Devices are ESD sensitive. Handling precaution is recommended.
- The device is not guaranteed to function outside its operating conditions.
- θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard.



PACKAGE INFORMATION

8-PIN, SOP



Notes:

1. All units are in millimeter
2. Refer to JEDEC MS-012 variation AA.



IMPORTANT NOTICE

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