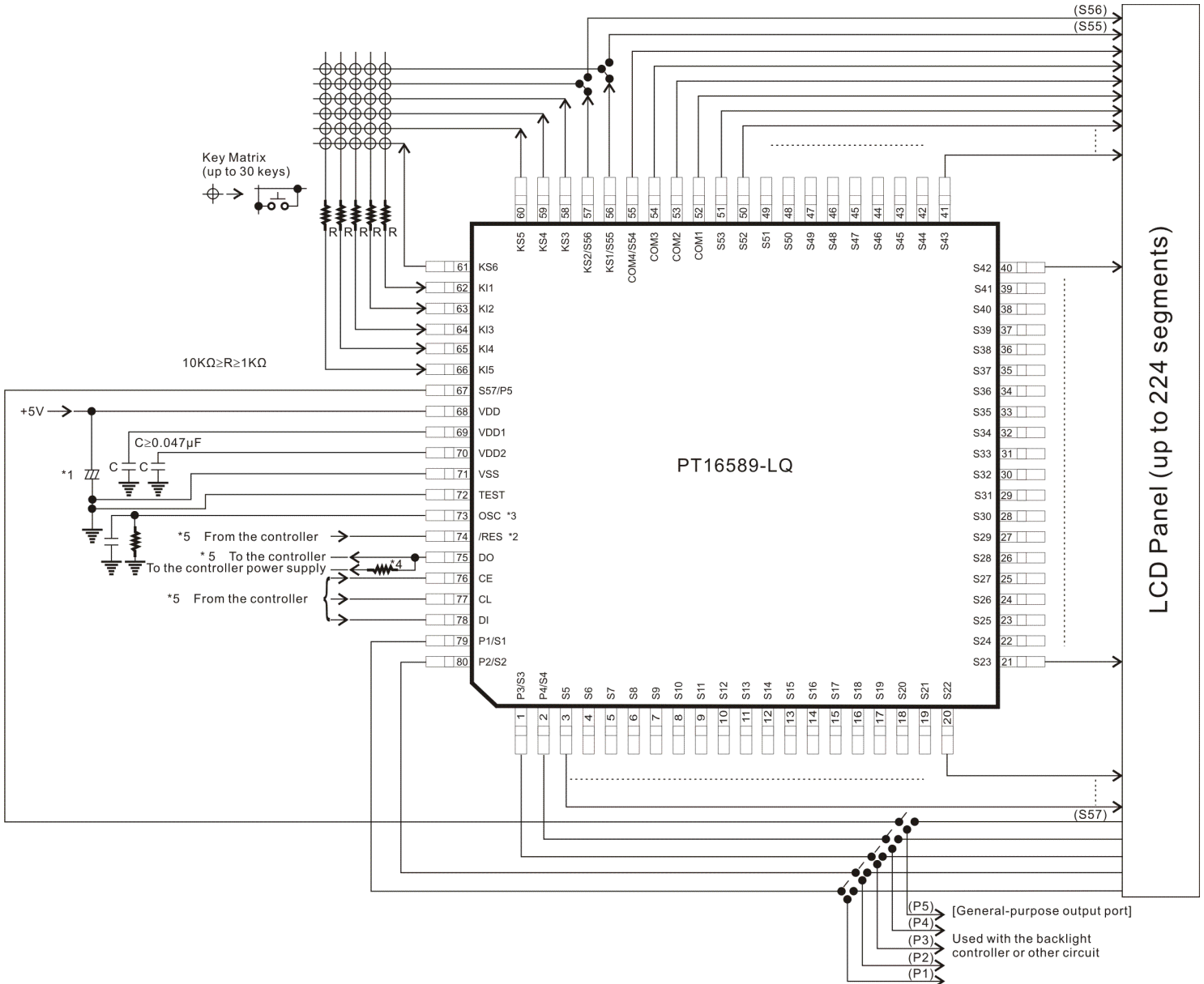


1. APPLICATION CIRCUITS

1.1 1/4 DUTY, 1/3 BIAS (FOR USE WITH NORMAL PANELS)

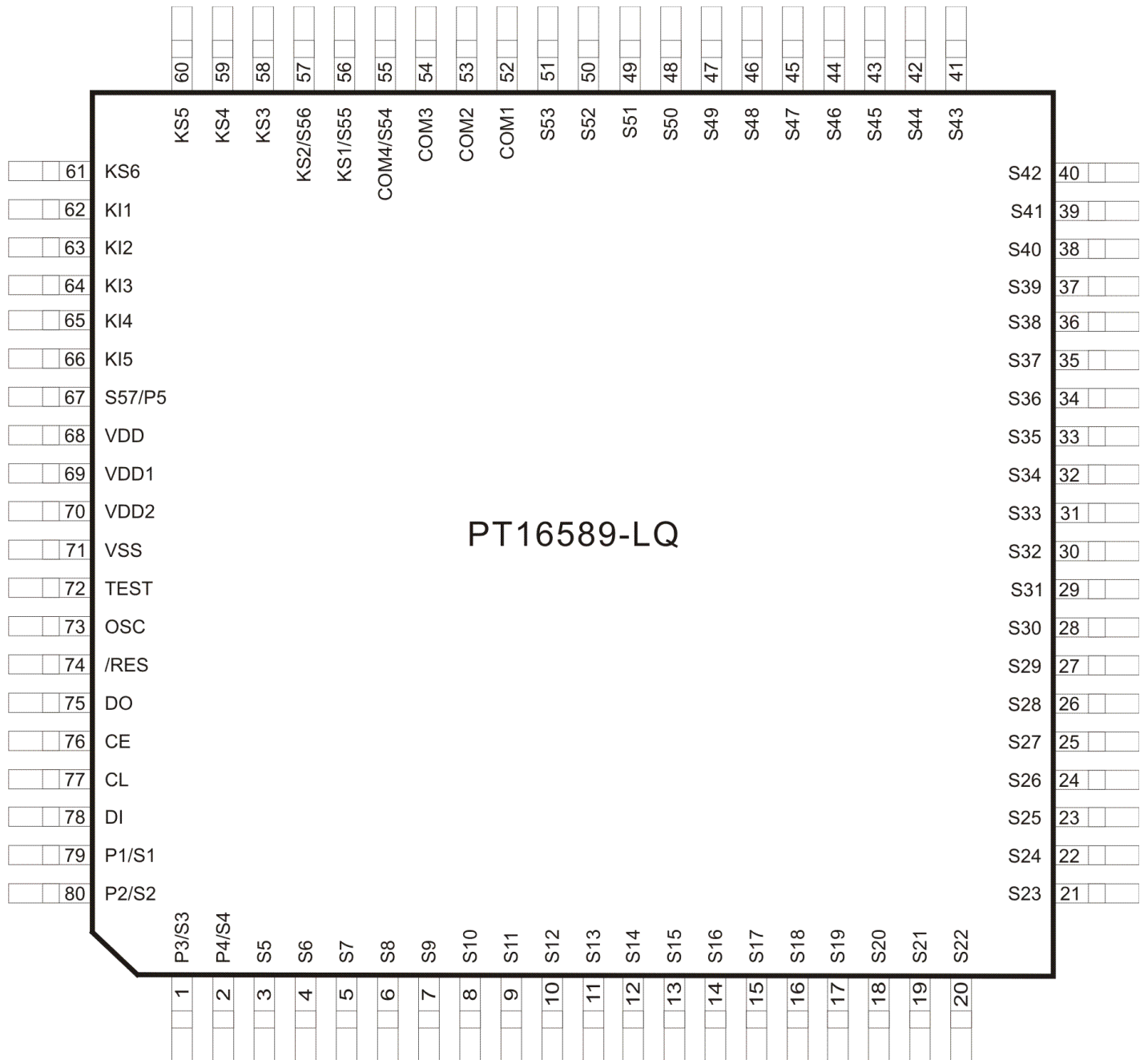


- Notes:
1. Add a capacitor to the power supply line so that the power supply voltage V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1ms, as the PT16589 is reset by the V_{DET} .
 2. If the /RES pin is not used for system reset, it must be connected to the power supply V_{DD} .
 3. When RC oscillator operating mode is used, the external resistor ROSC and the external capacitor COSC must be connected between the OSC pin and GND, and when external clock operating mode is selected the current protection resistor Rg (4.7 to 47KΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)
 4. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.
 5. The pins to be connected to the controller (CE, CL, DI, DO, /RES) can handle 3.3V or 5V.


2. ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT16589-LQ	80-Pin, LQFP	PT16589-LQ

3. PIN CONFIGURATION



4. PIN DESCRIPTION

Pin Name	I/O	Active	Handling when unused	Description	Pin No.
S1/P1 to S4/P4 S5 to S53	O	-	OPEN	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports under serial data control.	79,80,1,2 3 to 51
COM1 to COM3 COM4/S54	O	-	OPEN	Common driver outputs. The frame frequency is f_o [Hz]. The COM4/S54 pin can be used as a segment output in 1/3 duty.	52 to 54 55
KS1/S55 KS2/S56 KS3 to KS6	O	-	OPEN	Key scan outputs. Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S55 to KS2/S56 pins can be used as segment outputs when so specified by the control data.	56 57 58 to 61
KI1 to KI5	I	H	GND	Key scan inputs. These pins have built-in pull-down resistors.	62 to 66
S57/P5	O	-	OPEN	Logic block power supply connection. Provide a voltage of between 2.7 and 6.0V.	67
V_{DD}	-	-	-	Power supply connections. Provide a voltage of between 4.5 to 6.0V.	68
V_{DD1}	I	-	OPEN	Used for applying the LCD drive 2/3 bias voltage externally. Must be connected to V_{LCD2} when a 1/2 bias drive scheme is used.	69
V_{DD2}	I	-	OPEN	Used for applying the LCD drive 1/3 bias voltage externally. Must be connected to V_{LCD1} when a 1/2 bias drive scheme is used.	70
V_{SS}	-	-	-	Power supply connection. Connect to ground.	71
TEST	I	-	-	This pin must be connected to ground.	72
OSC	I/O	-	V_{DD}	The OSC pin can be used to form an oscillator circuit with an external resistor and an external capacitor. If external clock mode is selected with the control data, this pin is used to input an external clock signal.	73
/RES	I	L	V_{DD}	Reset signal input . /RES=Low Display off - S1/P1 to S4/P4, KS1/S55, KS2/S56=Low (These pins are forcibly set to the segment output port function and fixed at the low level.) - S5 to S53=Low - COM1 to COM3=Low - COM4/S54=Low (This pin is forcibly set to the common output function and fixed at the low level.) - S57/P5=Low (This pin is forcibly set to the general-purpose output port function and fixed at the low level.) - KS3 to KS6=Low - Key scanning disabled - All the key data is reset to low. - OSC="Z"(High impedance) - RC oscillation stopped - Inhibits external clock input . /RES=High Display on - General-purpose output port state setting is enabled - Key scanning is enabled. - RC oscillation enabled (RC oscillator operating mode) - Enables external clock input (external clock operating mode) However, serial data can be transferred when the RES pin is low	74
DO	O	-	OPEN	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. DO: Output data CE: Chip enable CL: Synchronization clock DI: Transfer data	75
CE	I	H	GND		76
CL	I				77
DI	I	-			78

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.

PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

Princeton Technology Corp.
2F, 233-1, Baociao Road,
Sindian Dist., New Taipei City 23145, Taiwan
Tel: 886-2-66296288
Fax: 886-2-29174598
<http://www.princeton.com.tw>