DESCRIPTION

PT6302 is a dot matrix VFD Driver/Controller IC utilizing CMOS Technology specially designed to display characters, numerals, and symbols. PT6302 provides 35 dot matrix, 2 additional segment drivers and 16 grid drivers. 248 types of character data (CGROM), 8 types of character data (CGRAM), 16 display digits x 2 bits symbol data, 16 display digits x 8 bits register for character data display and 2 general output bits for static operation are provided. Pin assignments and application circuit are optimized for easy PCB layout and cost saving advantages.

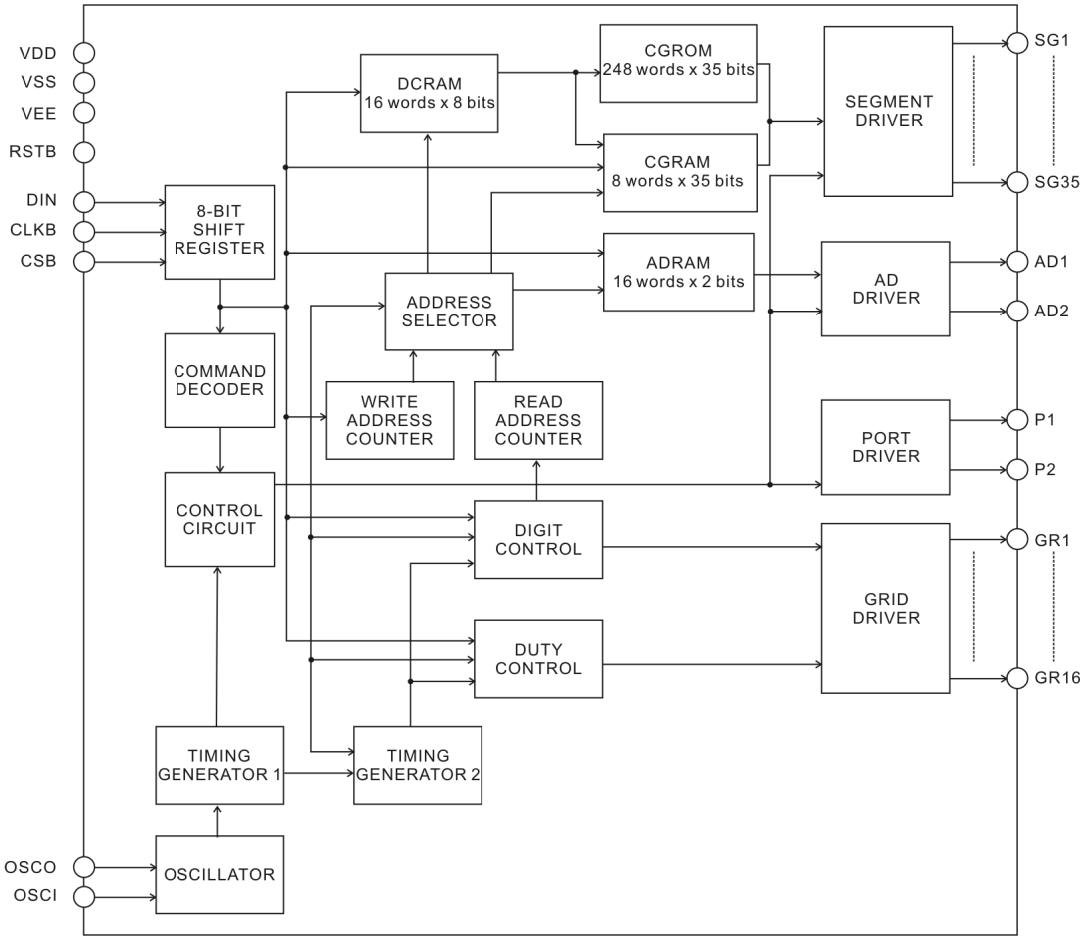
APPLICATIONS

- Microcontroller peripheral device
- Audio/Video equipment

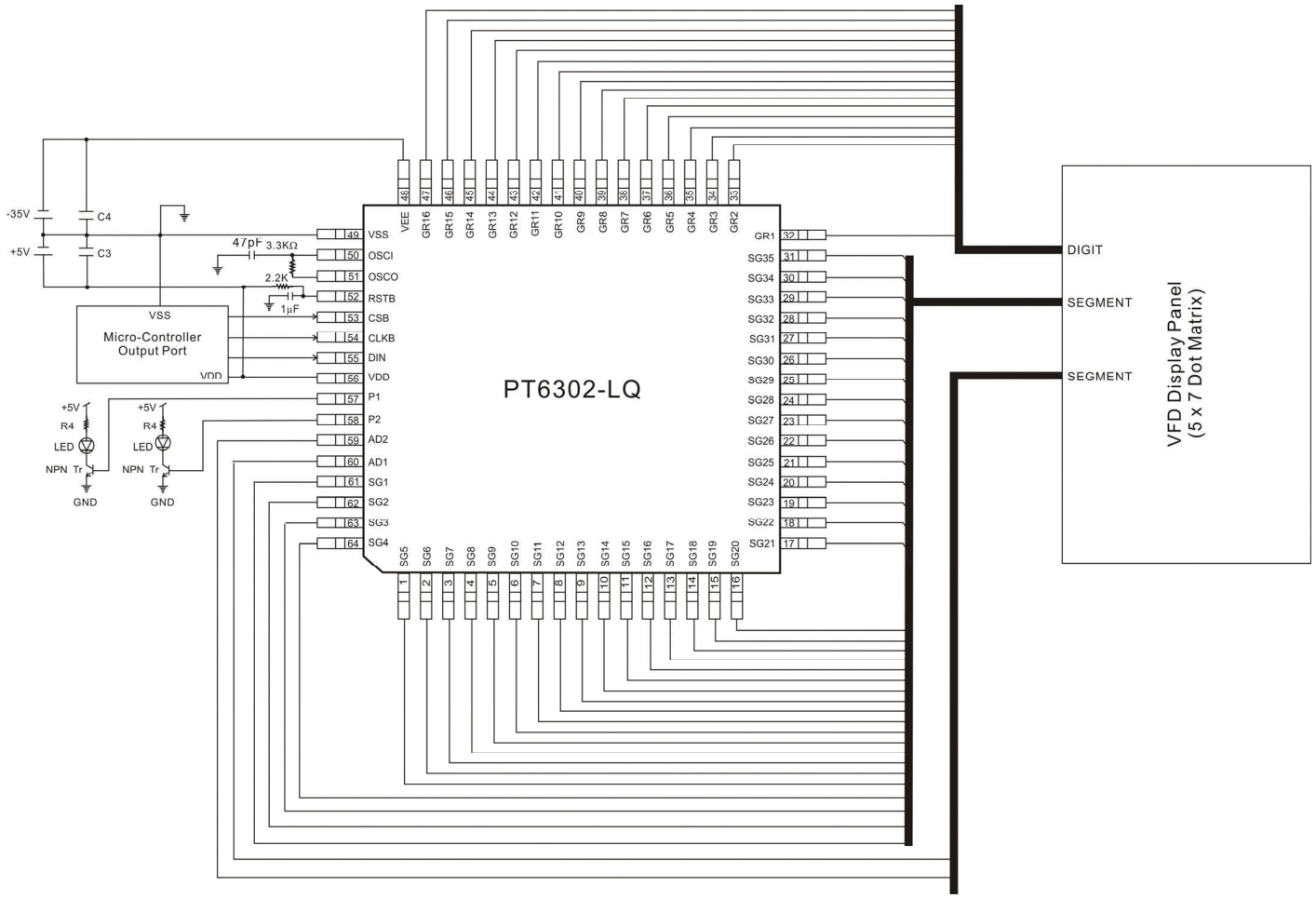
FEATURES

- CMOS technology
- Logic power supply: VDD=3.3V±10% or 5.0V±10%
- VFD drive power supply: VEE=-20V to -35V
- Built-in oscillation circuit (External RC)
- One-byte instruction execution (not including Data Write to RAM)
- Microcontroller interface
- Display contents:
  - Character generator ROM (CGROM): 5x7 Dots (248 Character data types)
  - Character generator RAM (CGRAM): 5x7 Dots (8 Character data types)
  - Additional data RAM (ADRAM): 16 Display digits x 2 Bits (Symbol data)
  - Data control RAM (DCRAM): 16 Display digits x 8 Bits (Character data display register)
  - General output port: 2 bits (Static operation)
- Display control function:
  - Display digits: 9 to 16 digits
  - Display duty (Contrast adjustment): 8 stages
  - All display lights: ON/OFF mode

BLOCK DIAGRAM



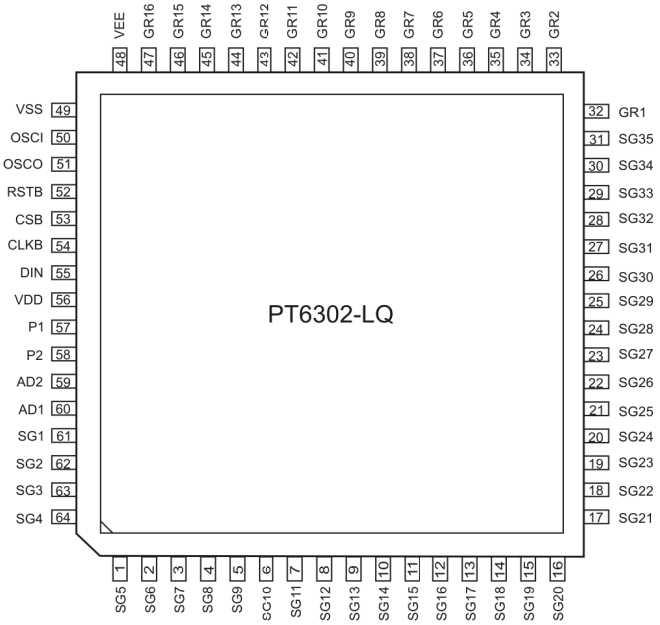
APPLICATION CIRCUIT



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6302LQ-001	64 pins, LQFP	PT6302LQ-001
PT6302LQ-003	64 pins, LQFP	PT6302LQ-003
PT6302LQ-005	64 pins, LQFP	PT6302LQ-005
PT6302LQ-007	64 pins, LQFP	PT6302LQ-007
PT6302-001-H	Bare Chip	-
PT6302-003-H	Bare Chip	-
PT6302-005-H	Bare Chip	-
PT6302-007-H	Bare Chip	-

PIN CONFIGURATION

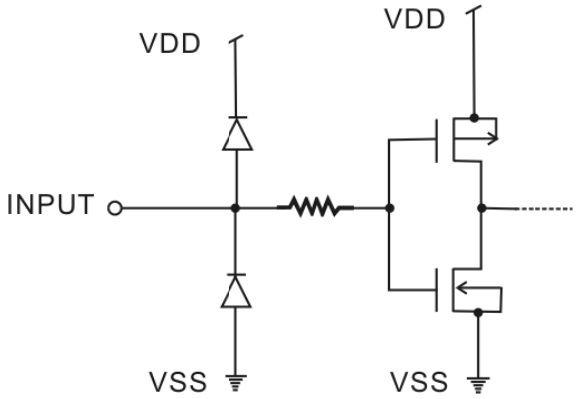


PIN DESCRIPTION

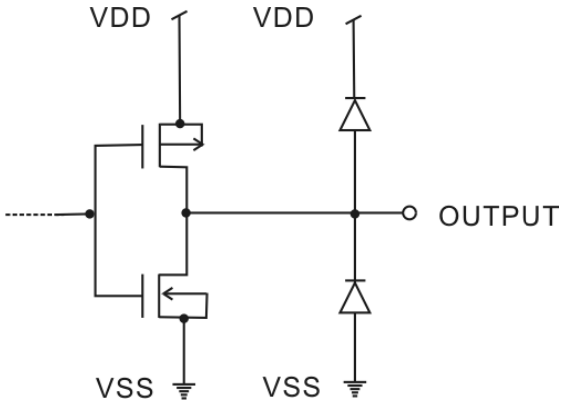
Pin Name	I/O	Description	Pin No.
SG5 to SG35 SG4 to SG1	O	Segment driver output pin	1 ~ 31 64 ~ 61
GR1 to GR16	O	Grid driver output pin	32 ~ 47
VEE	-	Power supply	48
VSS	-	Ground pin	49
OSCI	I	Oscillator input pin	50
OSCO	O	Oscillator output pin	51
RSTB	I	Reset input pin When this pin is set to "LOW", all functions are initialized.	52
CSB	I	Chip select input pin When this pin is set to "High" Level, the serial data transfer is disabled.	53
CLKB	I	Shift clock input pin The serial data is shifted at the rising edge of CLKB.	54
DIN	I	Serial data input pin	55
VDD	-	Positive power supply	56
P1 to P2	O	General purpose output pin	57 ~ 58
AD2 to AD1	O	Segment driver output pin	59 ~ 60

INPUT & OUTPUT CONFIGURATION

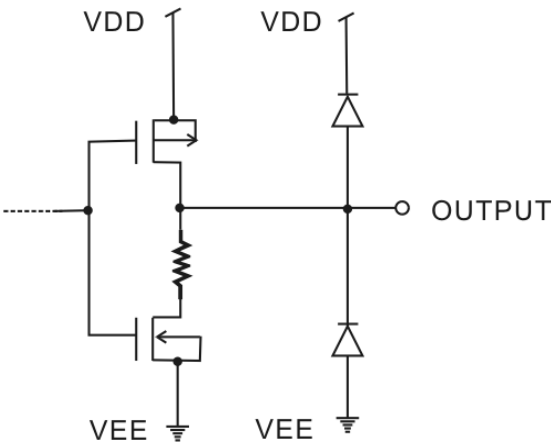
LOGIC INPUT PINS



LOGIC OUTPUT PINS



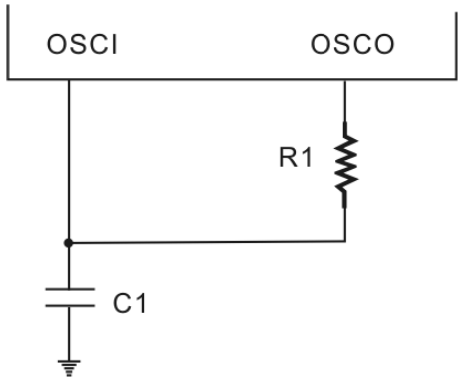
DRIVER OUTPUT PINS



FUNCTION DESCRIPTION

OSCILLATION CIRCUIT

An oscillation circuit may be constructed by connecting external Resistor (R1) and Capacitor (C1) between the oscillator pins -- OSCO and OSCI. The RC time constant depends on the value of VDD voltage used. The target oscillation frequency is 2MHz. Please refer to the diagram below.

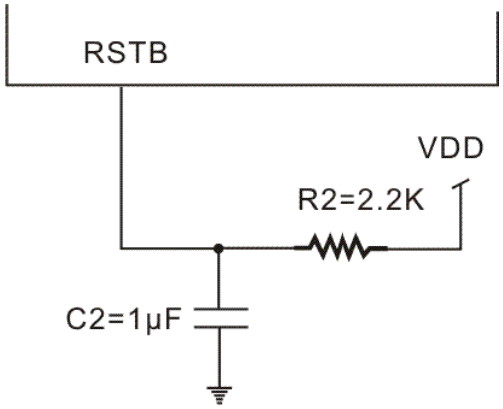


RESET FUNCTION

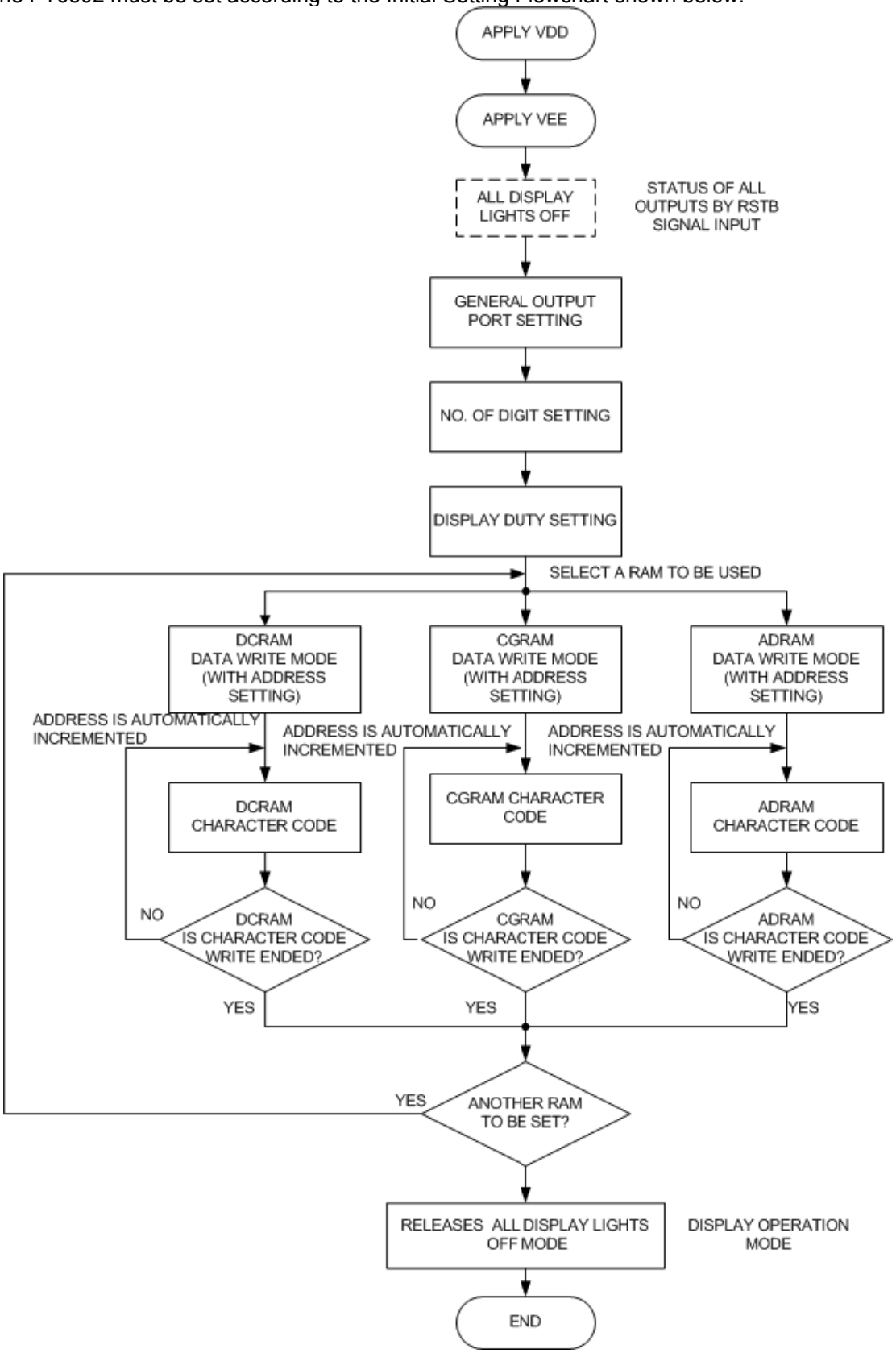
The Reset Function is enabled when the RSTB Pin is set to "Low" Level. All functions are initialized. The initial status of the various functions is given below:

1. Address of each RAM: Address "00"H
2. Data of each RAM: All contents are undefined.
3. General Output Ports: All General Output Ports are set to "LOW".
4. Display Digit: 16 Digits
5. Contrast Adjustment: 8/16
6. All Display Lights: OFF Mode
7. Segment Output: All Segment Outputs are set to "LOW".
8. AD Output: All AD Outputs are set to "LOW".

The RSTB Pin may be connected to either the microcontroller or an external Resistor and capacitor. For an external RC connection, please refer to the diagram below.

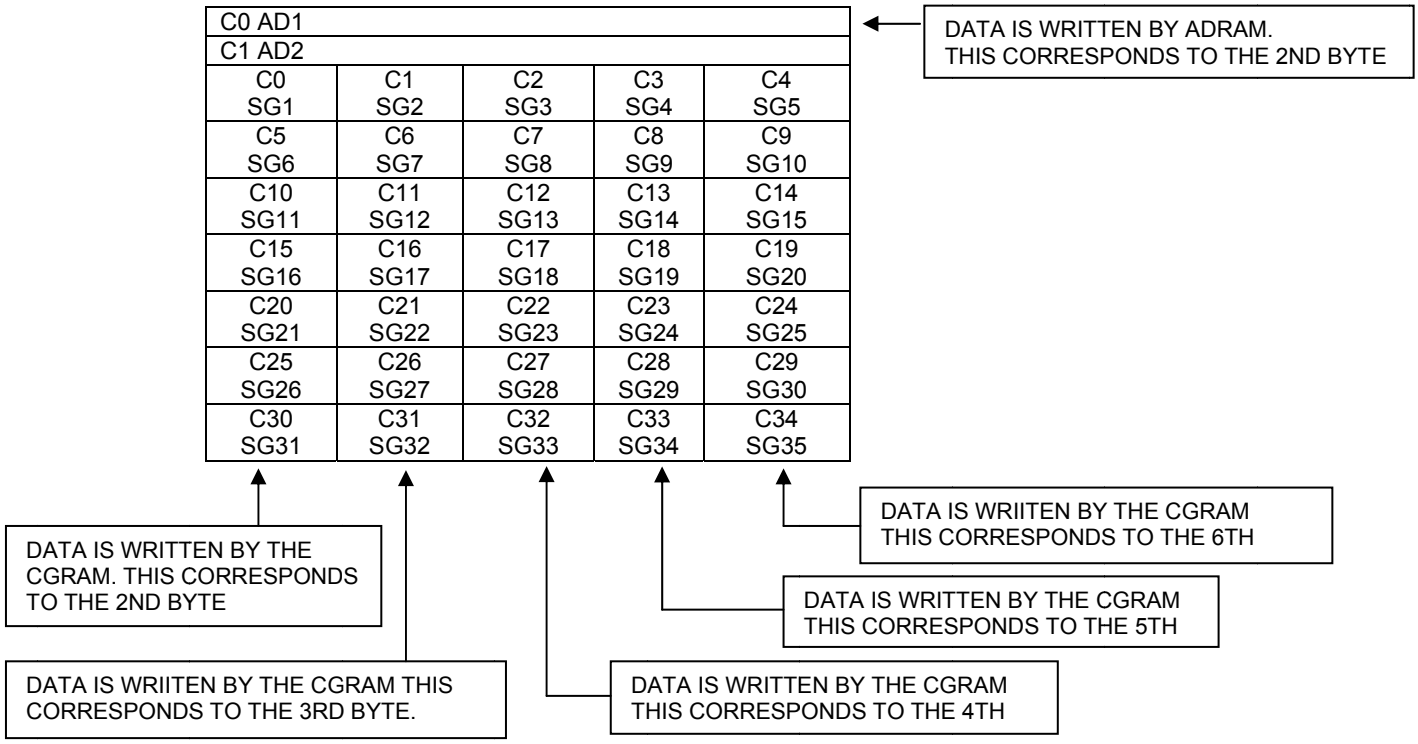


After reset, the PT6302 must be set according to the Initial Setting Flowchart shown below.



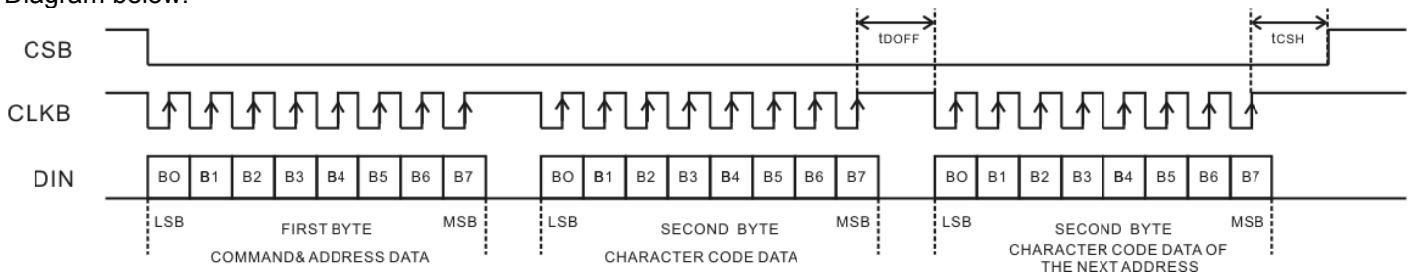
RELATIONSHIP BETWEEN SEGMENT DRIVERS SGN AND ADN (ONE DIGIT)

The following diagram best describes the relationship between the Segment Drivers -- SGn and ADn.



DATA TRANSFER

The Display Control Command and the data are written by an 8-bit serial data transfer. Please refer to the Write Timing Diagram below.



Note: When data is written into the RAM (DCRAM, ADRAM, CGRAM) in a continuous manner, the address are automatically incremented. Therefore it is not necessary to specify the first byte of the 2nd and later bytes when writing the RAM data.

When the CSB pin is set to "LOW" Level, data transfer operation is enabled. 8 bits of data are sequentially inputted into the DIN Pin (LSB first). The shift clock is inputted into CLKB pin and the shift register reads the data at rising edge of the shift clock. The internal load signals are automatically generated and the data is written to each register and RAM. Thus, it is not necessary to input load signals externally.

When the CSB Pin is set to "HIGH" Level, the data transfer operation is disabled. The data input when the CSB Pin changes from "HIGH" to "LOW" is recognized in 8-bit units.

COMMANDS

The following are the list of commands issued by PT6302. When data is written into the RAM (DCRAM, CGRAM, or ADRAM) in a continuous manner, the addresses are automatically incremented internally. It is therefore not necessary to specify the first byte.

NO.	COMMAND	LSB FIRST BYTE							MSB	LSB SECOND BYTE							MSB	
		B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
1	DCRAM DATA WRITE	X0	X1	X2	X3	1	0	0	0	C0	C1	C2	C3	C4	C5	C6	C7	
2	CGRAM DATA WRITE	X0	X1	X2	*	0	1	0	0	C0	C5	C10	C15	C20	C25	C30	*	2ND BYTE
										C1	C6	C11	C16	C21	C26	C31	*	3RD BYTE
										C2	C7	C12	C17	C22	C27	C32	*	4TH BYTE
										C3	C8	C13	C18	C23	C28	C33	*	5TH BYTE
										C4	C9	C14	C19	C24	C29	C34	*	6TH BYTE
3	ADRAM DATA WRITE	X0	X1	X2	X3	1	1	0	0	C0	C1	*	*	*	*	*	*	
4	GENERAL OUTPUT PORT SET	P1	P2	*	*	0	0	1	0									
5	DISPLAY DUTY SET	D0	D1	D2	*	1	0	1	0									
6	NO. OF DIGITS SET	K0	K1	K2	*	0	1	1	0									
7	ALL LIGHTS ON/OFF	L	H	*	*	1	1	1	0									
	TEST MODE	0	0	0	*	0	0	0	1									

Notes:
1. The Test Mode is not a user function, but an IC internal function
2. *=Not relevant
3. Xn=RAM address bit, n = 0 to 3
4. Cn=RAM character code bit, n=0 to 34
5. Pn=General output port status bit, n=1 to 2
6. Dn=Display duty bit, n=0 to 2
7. Kn=Number of digits bit, n=0 to 2
8. H=All lights on
9. L=All lights off

DATA CONTROL RAM (DCRAM) DATA WRITE COMMAND

The DCRAM Data Write Command is used to specify the address of the DCRAM and writes the character code of the CGROM and CGRAM. The DCRAM consists of 4 address bits which are used to store the CGRAM & CGROM character codes. The character codes specified by the DCRAM is converted to a 5 x 7 dot matrix character pattern via the CGROM and CGRAM. The DCRAM can store up to 16 characters. The DCRAM Data Write Command Format is shown below.

1st Byte (1st)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
X0	X1	X2	X3	1	0	0	0

DCRAM Data Write Mode is selected and the DCRAM Address is specified. (i.e. DCRAM Address = 0H)

2nd Byte (2nd)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	C2	C3	C4	C5	C6	C7

CGROM & CGRAM Character Codes are specified. (They are written into the DCRAM Address 0H)

During a continuous data write operation from one DCRAM Address to the next, it is not necessary to specify the DCRAM address since they are automatically incremented; however, the character code must be specified. Please refer to the information below.

2nd Byte (3rd)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	C2	C3	C4	C5	C6	C7

Character Code of CGRAM & CGROM are specified and written into the DCRAM Address 1H.

2nd Byte (4th)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	C2	C3	C4	C5	C6	C7

Character Code of CGRAM & CGROM are specified and written into the DCRAM Address 2H.

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2nd Byte (17th)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	C2	C3	C4	C5	C6	C7

Character Code of CGRAM & CGROM are specified and written into the DCRAM Address FH.

2nd Byte (18th)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	C2	C3	C4	C5	C6	C7

Character Code of CGRAM & CGROM are specified and rewritten into the DCRAM Address 0 H.

where:
1. X0 (LSB) to X3 (MSB): DCRAM Address Bits (16 Characters)
2. C0 (LSB) to C7 (MSB): CGROM & CGRAM Character Code Bits (256 Characters)

Please refer to the table below for the GRID position and DCRAM Address setting relationship.

Hex	X0	X1	X2	X3	GRID Position
0	0	0	0	0	GR1
1	1	0	0	0	GR2
2	0	1	0	0	GR3
3	1	1	0	0	GR4
4	0	0	1	0	GR5
5	1	0	1	0	GR6
6	0	1	1	0	GR7
7	1	1	1	0	GR8
8	0	0	0	1	GR9
9	1	0	0	1	GR10
A	0	1	0	1	GR11
B	1	1	0	1	GR12
C	0	0	1	1	GR13
D	1	0	1	1	GR14
E	0	1	1	1	GR15
F	1	1	1	1	GR16

CGRAM DATA WRITE COMMAND

The Character Generator RAM (CGRAM) Data Write Command is used to specify the CGRAM address (00H to 07H) and write the character pattern data. It consists of 3 address bits which is used to store the 5 x 7 dot matrix character patterns. The CGRAM can store up to 8 types of character patterns which may be displayed by specifying the Character Code (DCRAM Address). The CGRAM Data Write Command Format is given below.

1st Byte (1st)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
X0	X1	X2	*	0	1	0	0

CGRAM Data Write Mode is selected and the CGRAM Address is specified (i.e. CGRAM Address = 00H).

2nd Byte (2nd)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C0	C5	C10	C15	C20	C25	C30	*

1st Column Data is specified and rewritten into the CGRAM Address 00H.

3rd Byte (3rd)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C1	C6	C11	C16	C21	C26	C31	*

2nd Column Data is specified and rewritten into the CGRAM Address 00H.

4th Byte (4th)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C2	C7	C12	C17	C22	C27	C32	*

3rd Column Data is specified and rewritten into the CGRAM Address 00H.

5th Byte (5th)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C3	C8	C13	C18	C23	C28	C33	*

4th Column Data is specified and rewritten into the CGRAM Address 00H.

6th Byte (6th)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C4	C9	C14	C19	C24	C29	C34	*

5th Column Data is specified and rewritten into the CGRAM Address 00H.

During a continuous data write operation from one CGRAM Address to the next, it is not necessary to specify the CGRAM address since they are automatically incremented; however, the character pattern data must be specified. The 2nd to the 6th character pattern data byte are considered as one data item, therefore 300ns is sufficient value for parameter tDOFF between bytes. Please refer to the information below.

2nd Byte (7th)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C0	C5	C10	C15	C20	C25	C30	*

1st Column Data is specified and rewritten into the CGRAM Address 01H.

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6th Byte (11th)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C4	C9	C14	C19	C24	C29	C34	*

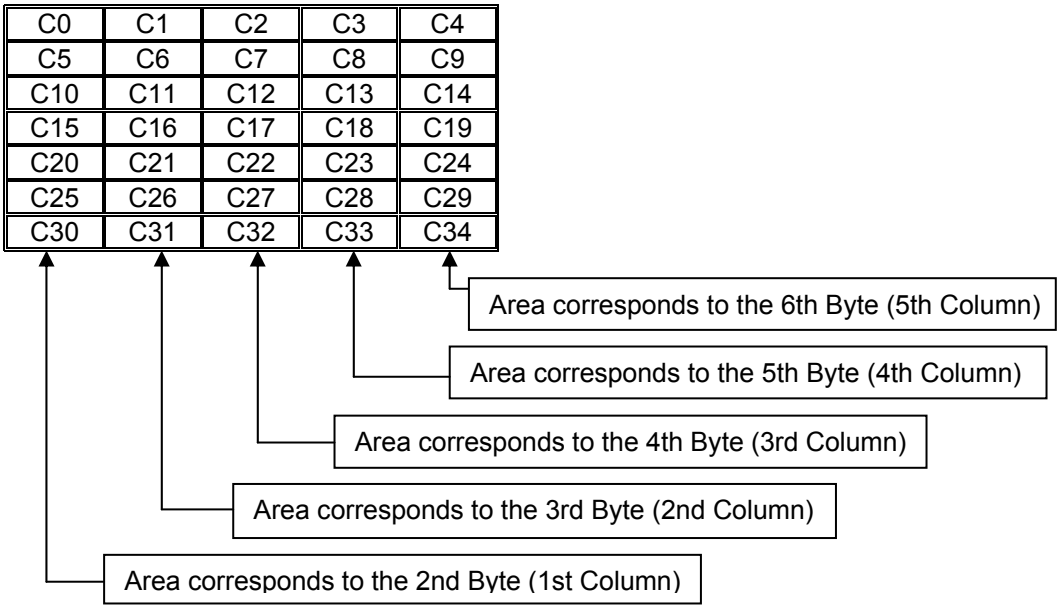
5th Column Data is specified and rewritten into the CGRAM Address 01H.

where:
1. X0 (LSB) to X2 (MSB): CGRAM Address Bits (8 Characters)
2. C0 (LSB) to C34 (MSB): Character Pattern Data Bits (35 outputs/digit)

Please refer below for the CGROM Address and CGRAM Address Setting relationship.

HEX	X0	X1	X2	CGROM Address
00	0	0	0	RAM00(00000000B)
01	1	0	0	RAM01(00000001B)
02	0	1	0	RAM02(00000010B)
03	1	1	0	RAM03(00000011B)
04	0	0	1	RAM04(00000100B)
05	1	0	1	RAM05(00000101B)
06	0	1	1	RAM06(00000110B)
07	1	1	1	RAM07(00000111B)

The CGROM and CGRAM output area placement is given in the table below.



Note: The Character Generator ROM (CGROM) consists of 8 CGROM Address bits generating 5 x 7 dot matrix character patterns. It can store up to a maximum of 248 types of character patterns.

ADRAM DATA WRITE COMMAND

The Additional Data RAM (ADRAM) consists of 4 address bits used to store the symbol data. It can store up to 2 types of symbol patterns per digit. The symbol data specified by the ADRAM is directly outputted. The terminals to which the ADRAM data are outputted may be used as a cursor. The ADRAM command format is given below.

1st Byte (1st)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
X0	X1	X2	X3	1	1	0	0

ADRAM Data Write Mode is selected and the ADRAM address is specified. (i.e. ADRAM Address = 0H)

2nd Byte (2nd)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	*	*	*	*	*	*

Symbol Data is specified and written into the ADRAM Address 0H.

During a continuous data write operation from one ADRAM Address to the next, it is not necessary to specify the ADRAM address since they are automatically incremented; however, the symbol data must be specified. Please refer to the information below.

2nd Byte (3rd)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	*	*	*	*	*	*

Symbol Data is specified and written into the ADRAM Address 1H.

2nd Byte (4th)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	*	*	*	*	*	*

Symbol Data is specified and written into the ADRAM Address 2H.

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:

2nd Byte (17th)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	*	*	*	*	*	*

Symbol Data is specified and written into the ADRAM Address FH.

2nd Byte (18th)

LSB							MSB
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	*	*	*	*	*	*

Symbol Data is specified and rewritten into the ADRAM Address 0H.

where:
1. X0 (LSB) to X3 (MSB): ADRAM address bits (16 Characters)
2. C0 (LSB) to C1 (MSB): Symbol data bits (2 symbol data per digit)

Please refer to the table below for the GRID and ADRAM Address relationship.

HEX	X0	X1	X2	X3	GRID Position
0	0	0	0	0	GR1
1	1	0	0	0	GR2
2	0	1	0	0	GR3
3	1	1	0	0	GR4
4	0	0	1	0	GR5
5	1	0	1	0	GR6
6	0	1	1	0	GR7
7	1	1	1	0	GR8
8	0	0	0	1	GR9
9	1	0	0	1	GR10
A	0	1	0	1	GR11
B	1	1	0	1	GR12
C	0	0	1	1	GR13
D	1	0	1	1	GR14
E	0	1	1	1	GR15
F	1	1	1	1	GR16

GENERAL OUTPUT PORT SET COMMAND

The General Output Port Set Command is used to specify the general output port status. The general output port is used to control other input/output devices as well as turn on the LED Display. When the general output port is set to "HIGH", the output is equivalent to the VDD voltage. When the general output port is set to "LOW" Level, the output becomes ground potential. The command format is given below.

	LSB							MSB	
1st Byte	B0	B1	B2	B3	B4	B5	B6	B7	A General Output Port is selected and the output status is specified.
	P1	P2	*	*	0	0	1	0	

where:
1. P1, P2: General output port
2. *=Not relevant

The following table shows the data setting in relation to the Status of the General Output Port

P1	P2	General Output Port Display Status
0	0	P1 ="LOW", P2="LOW" (see note 1)
1	0	P1="HIGH", P2="LOW"
0	1	P1="LOW", P2="HIGH"
1	1	P1="HIGH", P2="HIGH"

Note: The state when the power is applied or when the RSTB is inputted.

DISPLAY DUTY SET COMMAND

The Display Duty Set Command is used to write the display duty value to the duty cycle register. Using a 3-bit data, the display duty adjusts the contrast in 8 stages. When the power is turned ON or when the RSTB signal is inputted, the duty cycle register value is set to "0". It is advisable to always execute this command before turning on the display, after which the desired duty value may be set. The command format is given below.

	LSB							MSB	
1st Byte	B0	B1	B2	B3	B4	B5	B6	B7	Display Duty Set Mode is selected and the duty value is specified.
	D0	D1	D2	*	1	0	1	0	

where:
1. D0 (LSB) to D2 (MSB): Display duty data bits (8 stages)
2. *=Not relevant

The Relationship between the Setup Data and the Controlled GRID Duty is given in the table below.

HEX	D2	D1	D0	GRID Duty
0	0	0	0	8/16
1	0	0	1	9/16
2	0	1	0	10/16
3	0	1	1	11/16
4	1	0	0	12/16
5	1	0	1	13/16
6	1	1	0	14/16
7	1	1	1	15/16

The state when the Power is turned ON or when the RSTB signal is inputted

NUMBER OF DIGITS SET COMMAND

The Number of Digits Set Command is used to write the number of display digits into the display digit register. Using a 3-bit data, the Number of Digits Set Command can display 9 to 16 digits. When the power is turned ON or when the RSTB signal is inputted, the value is set to "0". It is advisable to always execute this command before the turning on the display. The command format is given below.

	LSB							MSB	
1st Byte	B0	B1	B2	B3	B4	B5	B6	B7	The Number of Digits Set Mode is selected and the number of digit value is specified.
	K0	K1	K2	*	0	1	1	0	

The table below shows the relationship between the setup data and the controlled GR.

HEX	K2	K1	K0	Number of Digits of GR
0	0	0	0	GR1 ~ GR16
1	0	0	1	GR1 ~ GR9
2	0	1	0	GR1 ~ GR10
3	0	1	1	GR1 ~ GR11
4	1	0	0	GR1 ~ GR 12
5	1	0	1	GR1~ GR13
6	1	1	0	GR1~ GR14
7	1	1	1	GR1~ GR15

The state when the Power is turned ON or when the RSTB signal is inputted.

DISPLAY LIGHT SET COMMAND

The Display Light Set Command is used to turn all display lights ON or OFF. All Display Lights ON Mode is primarily used for testing the display. The All Display Light OFF Mode is used for the blinking display and to prevent any malfunction when the power is turned ON. The general output port cannot be controlled by this command. The command format is given below.

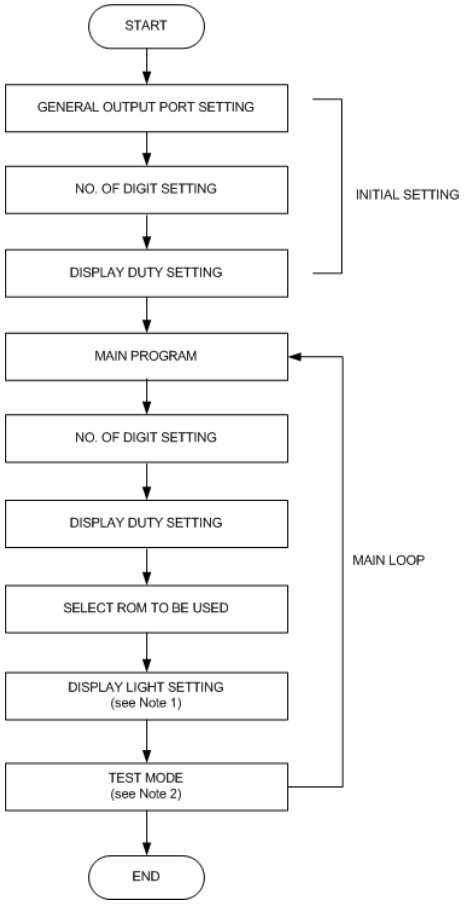
	LSB							MSB	
1st Byte	B0	B1	B2	B3	B4	B5	B6	B7	The Display Light Set Command is selected.
	L	H	*	*	1	1	1	0	

where:
1. L=All display lights are turned off
2. H=All display lights are turned on
3. *=Not relevant

The table below shows the SG and AD Display Status in relation to the Display Light Set Command data.

L	H	SG and AD Display State	
0	0	Normal Display Mode	The state when the power is applied or when the RSTB signal is inputted
1	0	All Outputs="LOW"	
0	1	All Outputs="HIGH"	
1	1	All Outputs="HIGH"	All Display Light ON Mode has the first priority.

RECOMMENDED SOFTWARE FLOWCHART



Notes:
1. Display light active mode (ex. 0111XX00B)
2. Test mode off (ex. 1000X000B)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply voltage 1	V_{DD}	-	-0.3 to 6.5	V
Supply voltage 2	V_{EE}	-	-35 to V_{DD}+0.3	V
Input voltage	V_{IN}	-	-0.3 to V_{DD}+0.3	V
Power dissipation	P_D	Ta ≤ 25℃	541	mW
Output current 1	I_{O1}	GR1 to GR16	-40 to 0	mA
Output current 2	I_{O2}	AD1 to AD2	-20 to 0	mA
Output current 3	I_{O3}	SG1 to SG35	-10 to 0	mA
Output current 4	I_{O4}	P1 to P2	-4.0 to 4.0	mA
Operating temperature	Topr	-	-40 to +85	℃
Storage temperature	Tstg	-	-65 to +150	℃

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage 1	V_{DD}		4.5	5.0	5.5	V
			3.0	3.3	3.6	V
Supply voltage 2	V_{EE}	Power supply voltage=5V	-35	-	-20	V
		Power supply voltage=3.3V	-35	-	-20	V
High level input voltage	V_{IH}	Power supply voltage=5V All input pins except OSCI.	0.7V_{DD}	-	-	V
		Power supply voltage=3.3V All input pins except OSCI.	0.8V_{DD}	-	-	V
Low level input voltage	V_{IL}	Power supply voltage=5V All input pins except OSCI.	-	-	0.3V_{DD}	V
		Power supply voltage=3.3V All input pins except OSCI.	-	-	0.2V_{DD}	V
CLKB frequency	fc	Power supply voltage=5V	-	-	1.0	MHz
		Power supply voltage=3.3V	-	-	1.0	MHz
Oscillation frequency	fosc	Power supply voltage=5V R1=3.3KΩ, C1=47pF	1.5	2.0	2.5	MHz
		Power supply voltage=3.3V R1=3.3KΩ, C1=39pF	1.5	2.0	2.5	MHz
Frame frequency	f_{FR}	Power supply voltage=5V DIGIT=1 to 16, R1=3.3KΩ, C1=47pF	183	244	305	Hz
		Power supply voltage=3.3V DIGIT=1 to 16, R1=3.3KΩ, C1=39pF	183	244	305	Hz
RSTB input time	t_{RSON}	Power supply voltage=5V	200	-	-	μs
		Power supply voltage=3.3V	200	-	-	
Operating temperature	T_{opr}	Power supply voltage=5V	-40	-	85	℃
		Power supply voltage=3.3V	-40	-	85	℃

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{EE}=-35V, Ta=-40 to +85℃)

Parameter	Symbol	Condition	Min.	Max.	Unit
High level input voltage	V_{IH}	V_{DD}=5.0±10% CSB, CLKB, DIN, RSTB	0.7V_{DD}	-	V
		V_{DD}=3.3±10% CSB, CLKB, DIN, RSTB	0.8V_{DD}	-	V
Low level input voltage	V_{IL}	V_{DD}=5.0±10% CSB, CLKB, DIN, RSTB	-	0.3V_{DD}	V
		V_{DD}=3.3±10% CSB, CLKB, DIN, RSTB	-	0.2V_{DD}	V
High level input current	I_{IH}	V_{DD}=5.0±10% CSB, CLKB, DIN, RSTB; V_{IH}=V_{DD}	-1.0	1.0	μA
		V_{DD}=3.3±10% CSB, CLKB, DIN, RSTB; V_{IH}=V_{DD}	-1.0	1.0	μA
Low level input current	I_{IL}	V_{DD}=5.0±10% CSB, CLKB, DIN, RSTB; V_{IL}=0V	-1.0	1.0	μA
		V_{DD}=3.3±10% CSB, CLKB, DIN, RSTB; V_{IL}=0V	-1.0	1.0	μA
High level output voltage 1	V_{OH1}	V_{DD}=5.0±10% GR1 to GR16; I_{OH}=-30mA	V_{DD}-1.5	-	V
		V_{DD}=3.3±10% GR1 to GR16; I_{OH}=-30mA	V_{DD}-1.5	-	V
High level output voltage 2	V_{OH2}	V_{DD}=5.0±10% AD1 to AD2, I_{OH}=-15mA	V_{DD}-1.5	-	V
		V_{DD}=3.3±10% AD1 to AD2, I_{OH}=-15mA	V_{DD}-1.5	-	V
High level output voltage 3	V_{OH3}	V_{DD}=5.0±10% SG1 to SG35, I_{OH}=-6mA	V_{DD}-1.5	-	V
		V_{DD}=3.3±10% SG1 to SG35, I_{OH}=-6mA	V_{DD}-1.5	-	V
High level output voltage 4	V_{OH4}	V_{DD}=5.0±10% P1 to P2, I_{OH}=-5mA	V_{DD}-1.0	-	V
		V_{DD}=3.3±10% P1 to P2, I_{OH}=-2.5mA	V_{DD}-1.0	-	V
Low level output voltage 1	V_{OL1}	V_{DD}=5.0±10% GR1 to GR16, AD1 to AD2,SG1 to SG35	-	V_{EE}+1.0	V
		V_{DD}=3.3±10% GR1 to GR16, AD1 to AD2; SG1 to SG35		V_{EE}+1.0	V
Low level output voltage	V_{OL2}	V_{DD}=5.0±10% P1, P2, I_{OL}=15mA	-	1.0	V
		V_{DD}=3.3±10% P1, P2, I_{OL}=7.5mA	-	1.0	V
Current consumption 1	I_{DD1}	V_{DD}=5.0±10% V_{DD}, fosc=2MHz, No Load Duty 15/16, DIGIT 1 to 16; All outputs lights ON	-	4	mA
		V_{DD}=3.3±10% V_{DD}, fosc=2MHz, No Load Duty 15/16, DIGIT 1 to 16; All outputs lights ON	-	3	mA
Current consumption 2	I_{DD2}	V_{DD}=5.0±10% V_{DD}, fosc=2MHz, No Load Duty 8/16, DIGIT 1 to 9; All outputs lights OFF	-	3	mA
		V_{DD}=3.3±10% V_{DD}, fosc=2MHz, No Load Duty 8/16, DIGIT 1 to 9; All outputs lights OFF	-	2	mA

AC CHARACTERISTICS

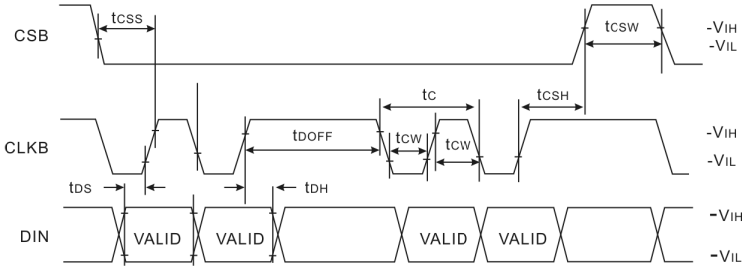
(Unless otherwise specified, V_{EE}=-35V, Ta=-40 to +85℃)

Parameter	Symbol	Condition	Min.	Max.	Unit
CLKB cycle time	fc	V_{DD}=5.0V+10%	1.0	-	μs
		V_{DD}=3.3V+10%	1.0	-	μs
CLKB pulse width	t_{CW}	V_{DD}=5.0V+10%	300	-	ns
		V_{DD}=3.3V+10%	300	-	ns
DIN setup time	t_{DS}	V_{DD}=5.0V+10%	300	-	ns
		V_{DD}=3.3V+10%	300	-	ns
DIN hold time	t_{DH}	V_{DD}=5.0V+10%	300	-	ns
		V_{DD}=3.3V+10%	300	-	ns
CSB setup time	t_{CSS}	V_{DD}=5.0V+10%	300	-	ns
		V_{DD}=3.3V+10%	300	-	ns
CSB hold time	t_{CSH}	V_{DD}=5.0V+10% R1=3.3KΩ, C1=47pF	16	-	μs
		V_{DD}=3.3V+10% R1=3.3KΩ, C1=39pF	16	-	μs
CSB wait time	t_{CSW}	V_{DD}=5.0V+10%	300	-	ns
		V_{DD}=3.3V+10%	300	-	ns
Data processing time	t_{DOFF}	V_{DD}=5.0V+10% R1=3.3KΩ, C1=47pF	8	-	μs
		V_{DD}=3.3V+10% R1=3.3KΩ, C1=39pF	8	-	μs
RSTB pulse width	t_{WRSTB}	V_{DD}=5.0V+10% When the RSTB signal is externally inputted from the microcontroller.	300	-	ns
		V_{DD}=3.3V+10% When the RSTB signal is externally inputted from the microcontroller.	300	-	ns
DIN wait time	t_{RSOFF}	V_{DD}=5.0V+10%	300	-	ns
		V_{DD}=3.3V+10%	300	-	ns
All outputs slew rate	t_R	V_{DD}=5.0V+10% Ci=100pF, tR=20% to 80%	-	4.0	μs
		V_{DD}=3.3V+10% Ci=100pF, tR=20% to 80%	-	4.0	μs
	t_F	V_{DD}=5.0V+10% Ci=100pF, tF=80% to 20%	-	4.0	μs
		V_{DD}=3.3V+10% Ci=100pF, tF=80% to 20%	-	4.0	μs
VDD rise time	t_{PRZ}	V_{DD}=5.0V+10% Mounted in the Unit	100	-	μs
		V_{DD}=3.3V+10% Mounted in the Unit	100	-	
VDD off time	t_{POF}	V_{DD}=0V Mounted in the Unit	5.0	-	ms

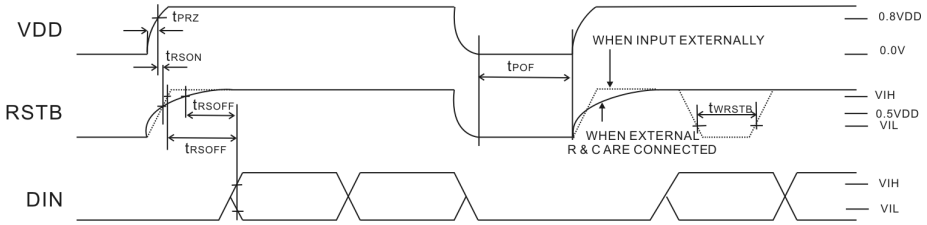
TIMING CHARACTERISTICS

Parameter	Symbol	VDD=3.3V±10%	VDD=5.0±10%
High level input voltage	V_{IH}	$0.8V_{DD}$	$0.7V_{DD}$
Low level input voltage	V_{IL}	$0.2V_{DD}$	$0.3V_{DD}$

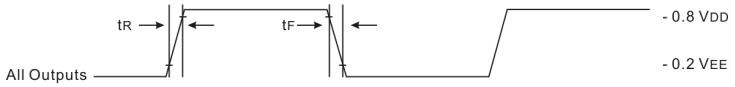
DATA TIMING



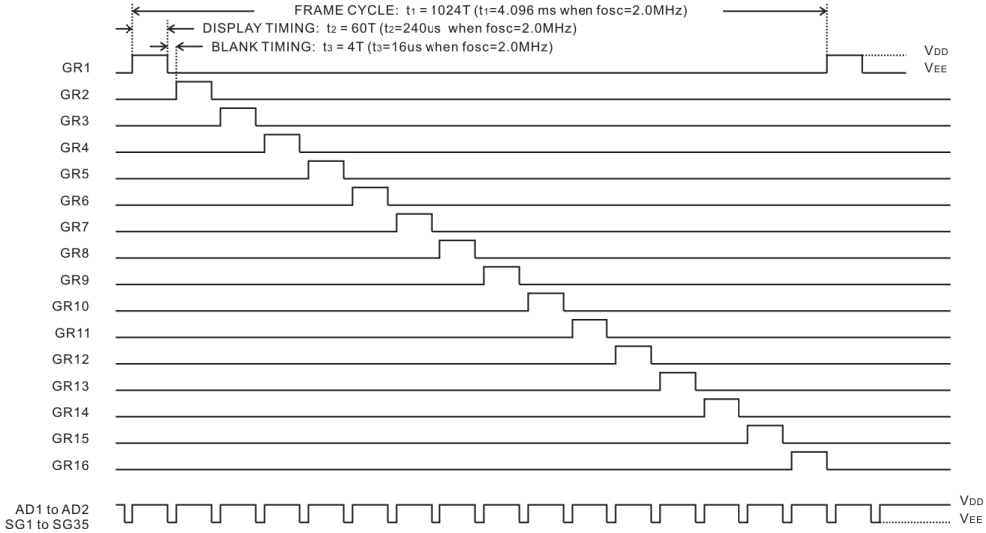
RESET (RSTB) TIMING



OUTPUT TIMING



DIGIT OUTPUT TIMING (16-DIGIT DISPLAY, DUTY= 15/16)

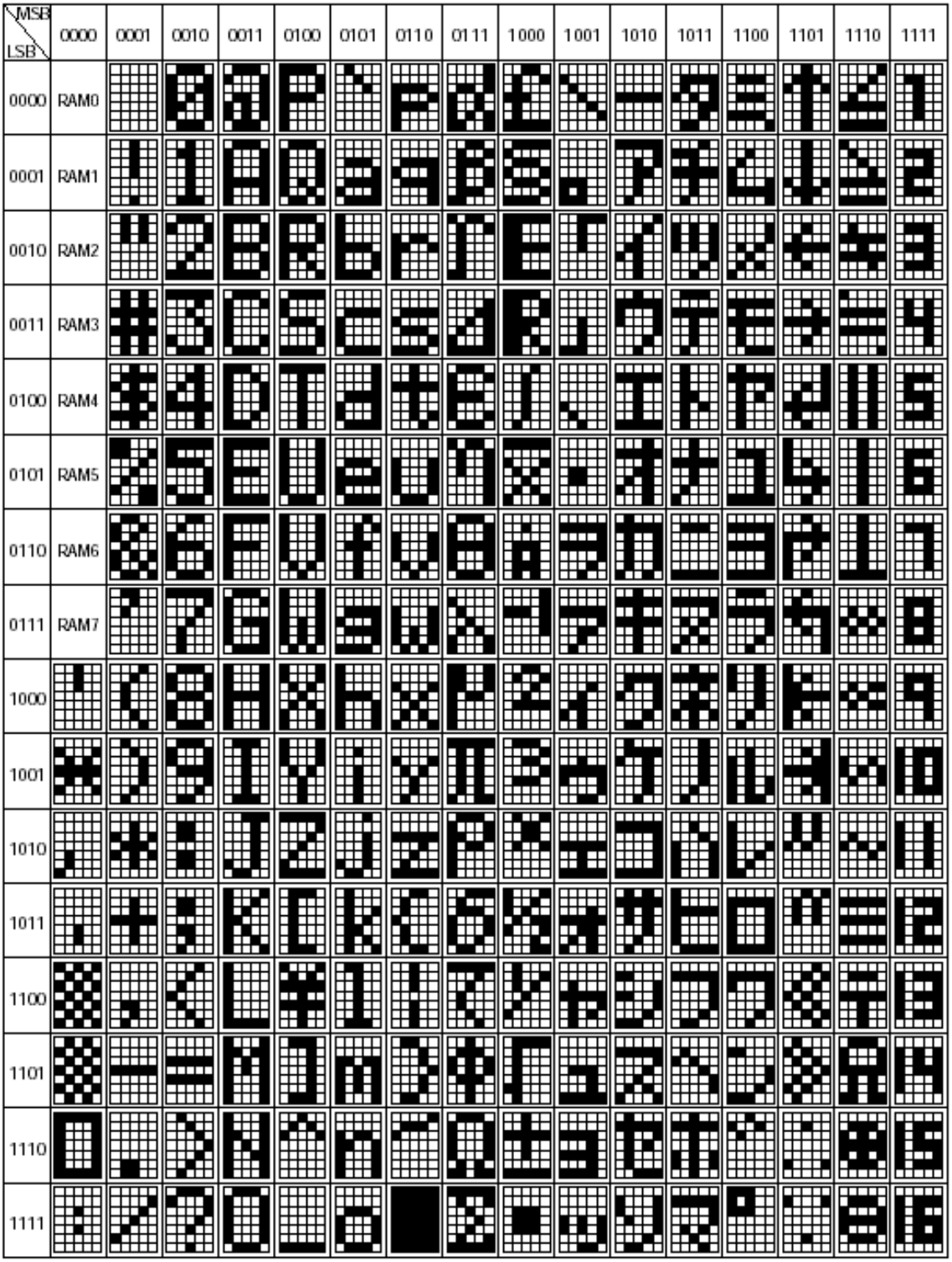


where: T=8/fosc

PT6302-001 CHARACTER FONT TABLE

MSB / LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	RAM0															
1	RAM1															
2	RAM2															
3	RAM3															
4	RAM4															
5	RAM5															
6	RAM6															
7	RAM7															
8																
9																
A																
B																
C																
D																
E																
F																

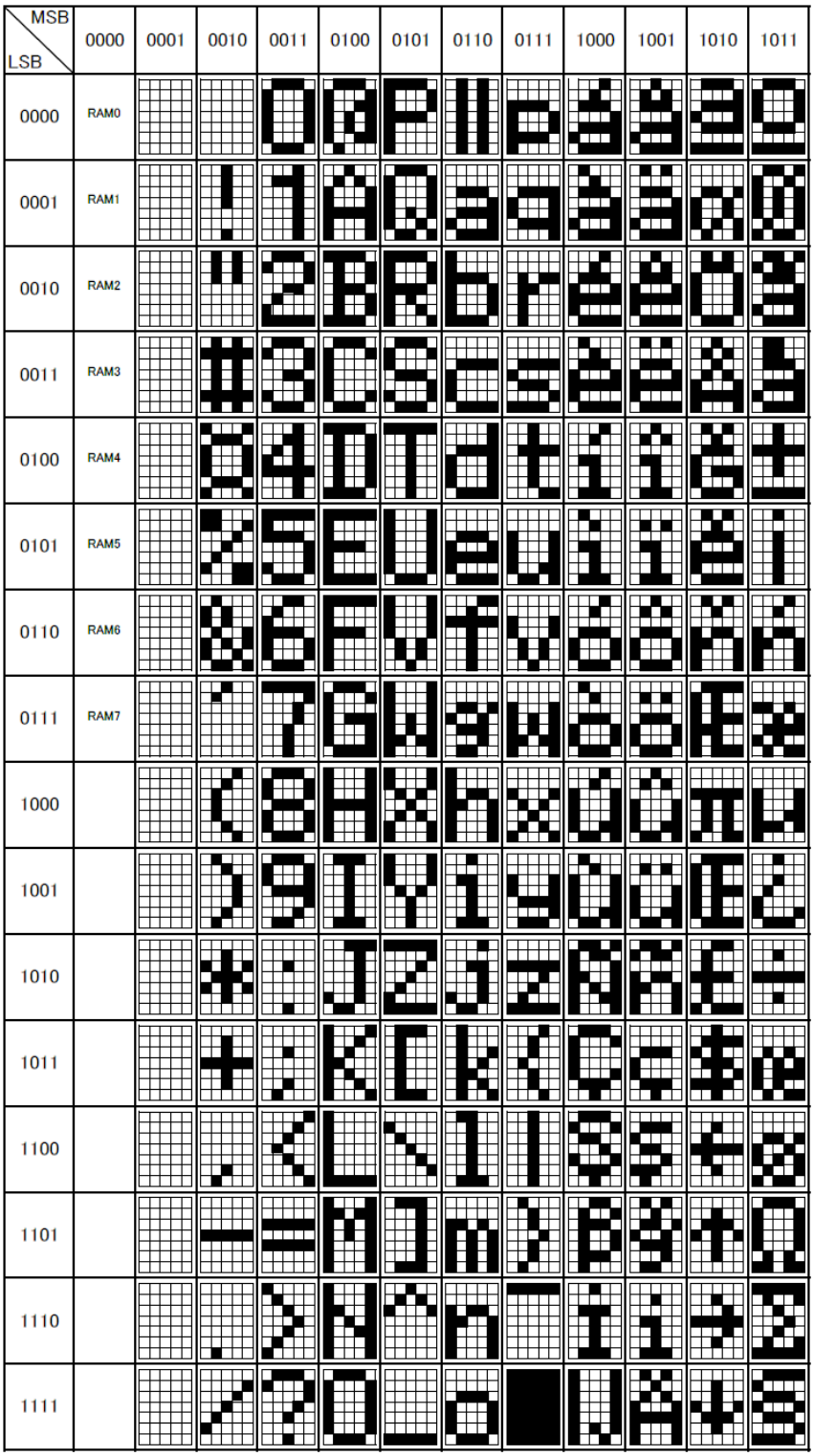
PT6302-003 CHARACTER FONT TABLE



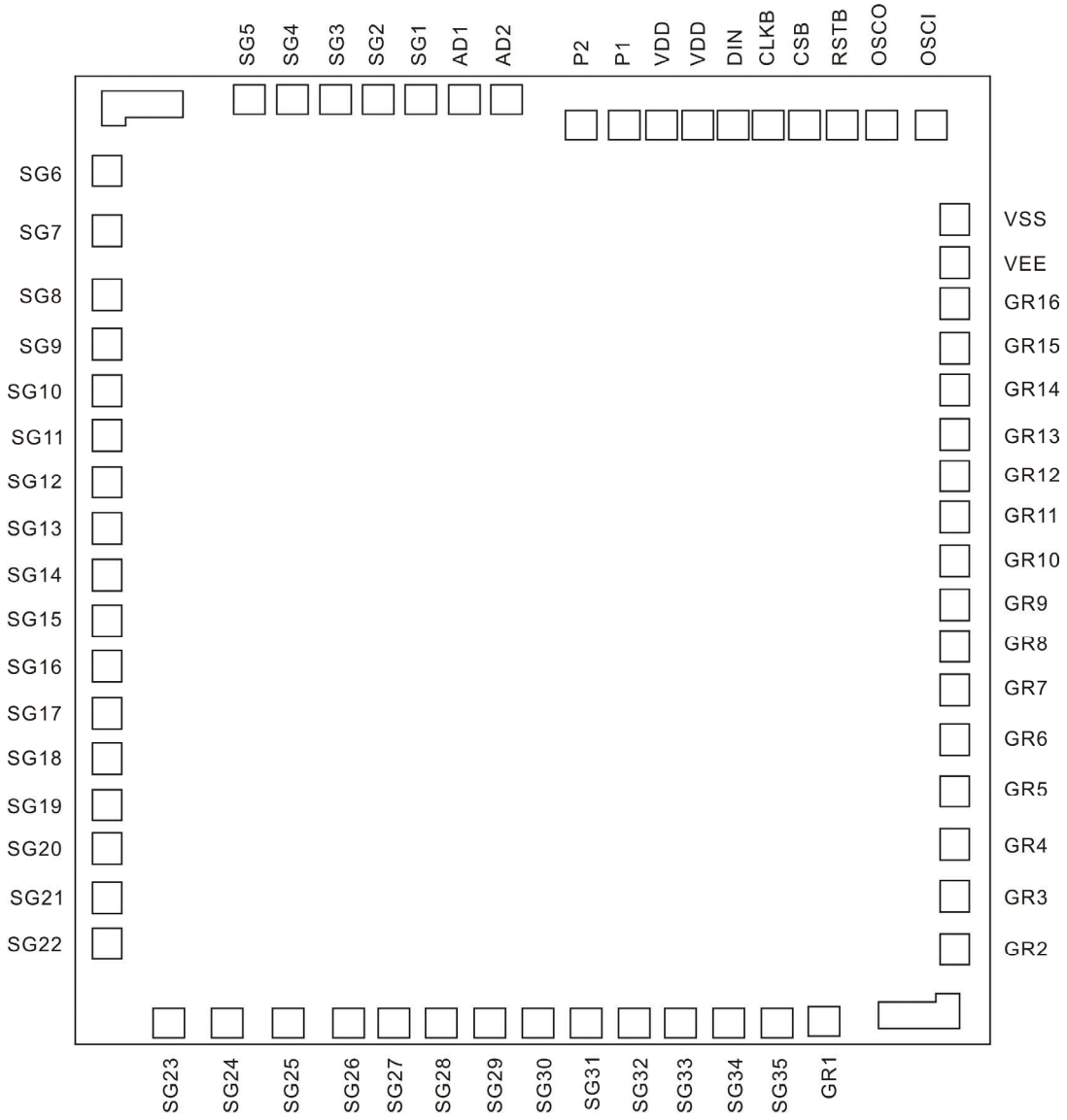
PT6302-005 CHARACTER FONT TABLE

Upper / Lower Nibble		D7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		D6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		D5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		D4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
D3	D2 D1 D0		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0 0 0	0	CG-RAM (#0)																
0	0 0 1	1	CG-RAM (#1)																
0	0 1 0	2	CG-RAM (#2)																
0	0 1 1	3	CG-RAM (#3)																
0	1 0 0	4	CG-RAM (#4)																
0	1 0 1	5	CG-RAM (#5)																
0	1 1 0	6	CG-RAM (#6)																
0	1 1 1	7	CG-RAM (#7)																
1	0 0 0	8																	
1	0 0 1	9																	
1	0 1 0	A																	
1	0 1 1	B																	
1	1 0 0	C																	
1	1 0 1	D																	
1	1 1 0	E																	
1	1 1 1	F																	

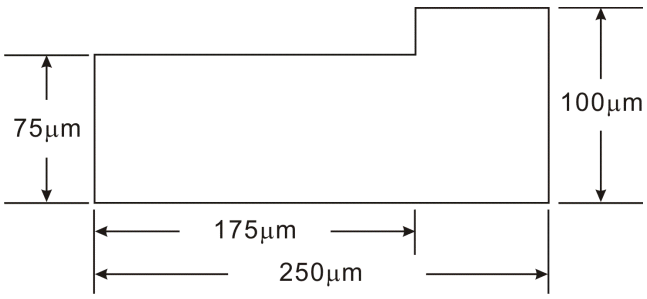
PT6302-007 CHARACTER FONT TABLE



PAD CONFIGURATION



ALIGNMENT MARK DIMENSION



Die Size:	X=2870μm Y=3140μm (Extended Buffer)
Chip Thickness:	300μm
PAD Size:	X=90μm Y=90μm
PAD Pitch:	110μm

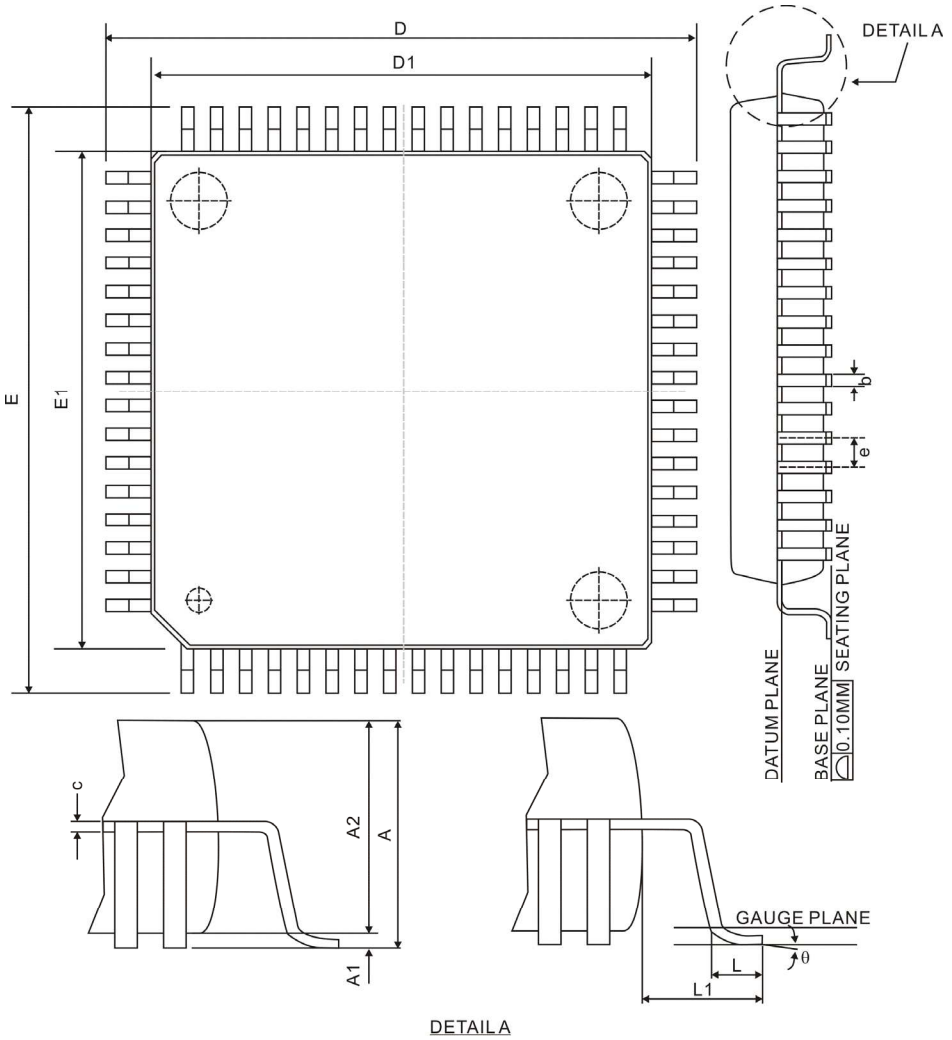
PAD LOCATION

Pad No.	Pad Name	Location
1	SG5	[478.600, 2852.100]
2	SG6	[50.000, 2637.500]
3	SG7	[50.000, 2447.500]
4	SG8	[50.000, 2257.500]
5	SG9	[50.000, 2107.500]
6	SG10	[50.000, 1967.500]
7	SG11	[50.000, 1827.500]
8	SG12	[50.000, 1687.500]
9	SG13	[50.000, 1547.500]
10	SG14	[50.000, 1407.500]
11	SG15	[50.000, 1267.500]
12	SG16	[50.000, 1127.500]
13	SG17	[50.000, 987.500]
14	SG18	[50.000, 847.500]
15	SG19	[50.000, 707.500]
16	SG20	[50.000, 567.500]
17	SG21	[50.000, 427.500]
18	SG22	[50.000, 287.500]
19	SG23	[233.800, 50.000]
20	SG24	[413.800, 50.000]
21	SG25	[593.800, 50.000]
22	SG26	[773.800, 50.000]
23	SG27	[918.800, 50.000]
24	SG28	[1063.800, 50.000]
25	SG29	[1208.800, 50.000]
26	SG30	[1353.800, 50.000]
27	SG31	[1498.800, 50.000]
28	SG32	[1643.800, 50.000]
29	SG33	[1788.800, 50.000]
30	SG34	[1933.800, 50.000]
31	SG35	[2078.800, 50.000]
32	GR1	[2223.800, 50.000]
33	GR2	[2615.800, 267.200]
34	GR3	[2615.800, 427.200]
35	GR4	[2615.800, 587.200]
36	GR5	[2615.800, 747.200]
37	GR6	[2615.800, 907.200]
38	GR7	[2615.800, 1057.200]
39	GR8	[2615.800, 1187.200]
40	GR9	[2615.800, 1317.200]
41	GR10	[2615.800, 1447.200]
42	GR11	[2615.800, 1577.200]

Pad No.	Pad Name	Location
43	GR12	[2615.800, 1707.200]
44	GR13	[2615.800, 1837.200]
45	GR14	[2615.800, 1967.200]
46	GR15	[2615.800, 2097.200]
47	GR16	[2615.800, 2227.200]
48	VEE	[2615.800, 2357.200]
49	VSS	[2615.800, 2487.200]
50	OSCI	[2543.700, 2772.300]
51	OSCO	[2395.900, 2772.300]
52	RSTB	[2277.900, 2772.300]
53	CSB	[2167.900, 2772.300]
54	CLKB	[2057.900, 2772.300]
55	DIN	[1947.900, 2772.300]
56	VDD	[1837.900, 2772.300]
56	VDD	[1727.900, 2772.300]
57	P1	[1615.300, 2772.300]
58	P2	[1490.100, 2772.300]
59	AD2	[1258.600, 2852.100]
60	AD1	[1128.600, 2852.100]
61	SG1	[998.600, 2852.100]
62	SG2	[868.600, 2852.100]
63	SG3	[738.600, 2852.100]
64	SG4	[608.600, 2852.100]

PACKAGE INFORMATION

64 PINS, LQFP



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.35	0.40
c	0.09	-	0.16
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.80 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Notes:
1. All dimensions are in millimeter
2. Refer to JEDEC MS-022 BE

IMPORTANT NOTICE

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