

NHD-320240WG-BxTGH-VZ#-3VR

Graphic Liquid Crystal Display Module

NHD-	Newhaven Display
320240-	320 x 240 Pixels
WG-	Display Type: Graphic
Bx-	Model
T-	White LED Backlight
G-	STN - Gray
H-	Transflective, 6:00 Optimal View, Wide Temperature
VZ#-	Built-in Negative Voltage
3VR-	3.3V Vdd, Frame Ground
	RoHS Compliant

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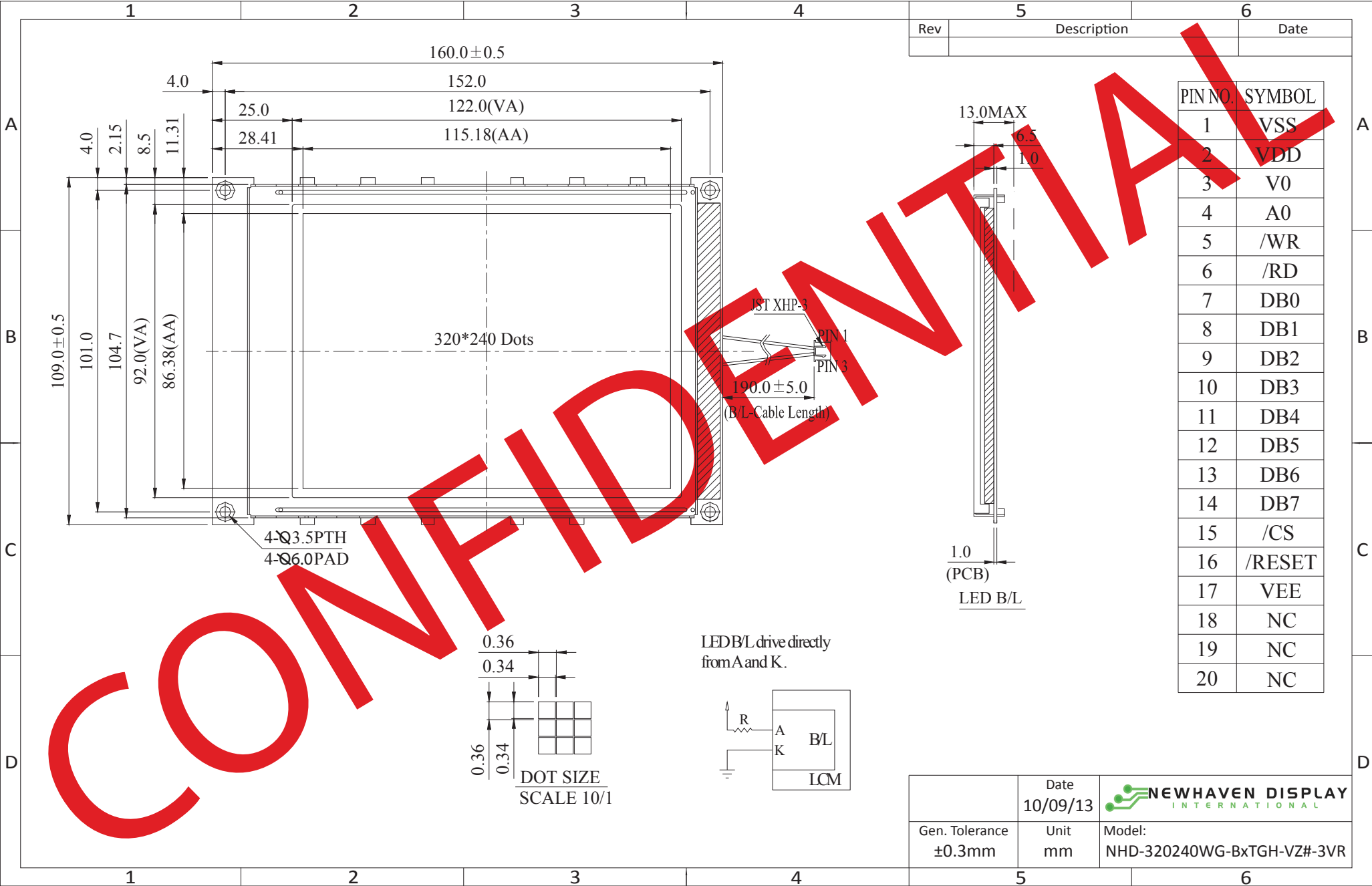
Document Revision History

Revision	Date	Description	Changed by
0	6/7/2007	Initial Release	-
1	3/16/2010	User guide reformat	MC
2	9/2/2010	Mechanical drawing update	MP
3	10/9/2013	Mechanical Drawing, Pin Description, Electrical Characteristics, Timing Characteristics updated Added Jumper Selection	ML

Functions and Features

- 320 x 240 pixels
- Built-in S1D13700 Controller
- +3.3V power supply
- RoHS Compliant

Mechanical Drawing



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Pin Description

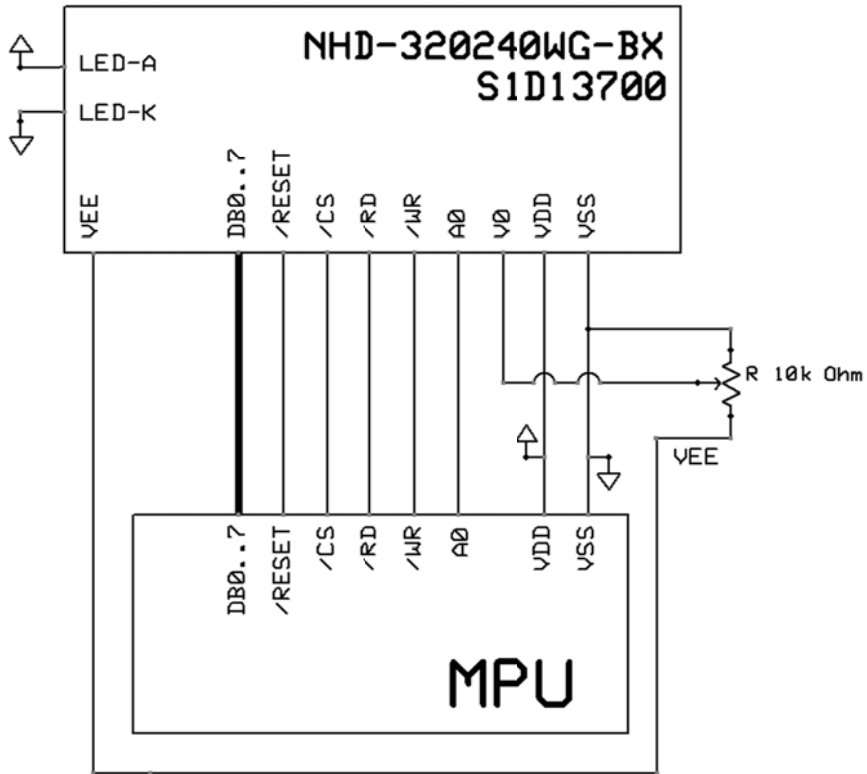
Pin No.	Symbol	External Connection	Function Description
1	VSS	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage (+3.3V)
3	V0	Adj Power Supply	Adj. Power Supply for contrast (approx. -18.8V)
4	A0	MPU	Register Select signal. A0=0: Command, A0=1: Data
5	/WR R/W	MPU	8080: Active LOW Write signal 6800: Read/Write select signal, R/W=1: Read R/W=0: Write
6	/RD E	MPU	8080: Active LOW Read signal 6800: Operation Enable signal. Falling edge triggered.
7-14	DB0-DB7	MPU	8-bit bi-directional data bus
15	/CS	MPU	Active LOW Chip Select signal
16	/RESET	MPU	Active LOW Reset signal
17	VEE	Power Supply	Negative voltage output (-25V)
18	NC	-	No Connect
19	NC	-	No Connect
20	NC	-	No Connect

Recommended LCD connector: 1.0mm pitch, 20-pos FFC connector

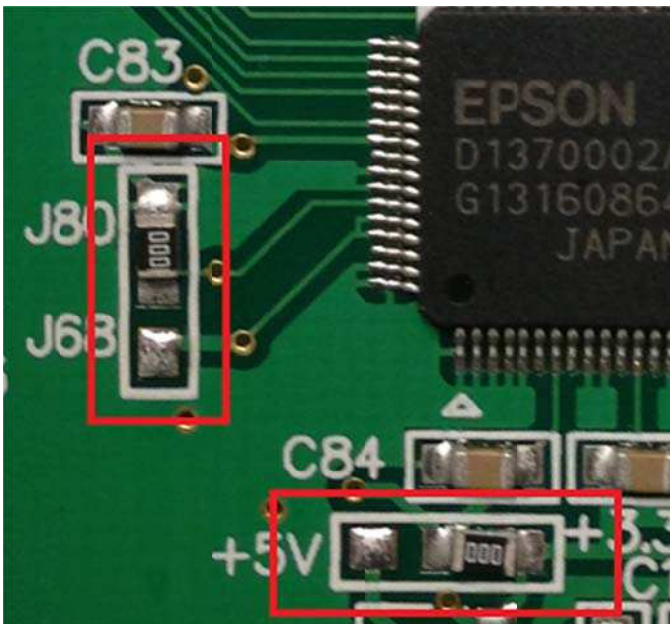
Backlight connector: JST p/n: XHP-3

Mates with: JST p/n: B 3B-XH-A

Wiring Diagram



Jumper Selection



Note: This display is pre-configured for 3.3V and 8080 mode.

Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	Top	Absolute Max	-20	-	+70	°C
Storage Temperature Range	Tst	Absolute Max	-30	-	+80	°C
Supply Voltage	VDD	-	3.0	3.3	3.5	V
Supply Current	IDD	Ta=25°C, VDD=5.0V	65.0	75.0	85.0	mA
Supply for LCD (contrast)	VDD-VLCD	Ta=25°C	20.0	21.8	24.1	V
"H" Level input	VIH	-	0.5*VDD	-	VDD	V
"L" Level input	VIL	-	VSS	-	0.2*VDD	V
"H" Level output	VOH	-	VDD-0.4	-	VDD	V
"L" Level output	VOL	-	VSS	-	0.4	V
Backlight Supply Voltage	VLED	-	3.4	3.5	3.6	V
Backlight Supply Current	ILED	VLED=3.5V	120	160	180	mA

Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing Angle - Top	-	Cr ≥ 3	-	20	-	°
Viewing Angle - Bottom	-		-	40	-	°
Viewing Angle - Left	-		-	30	-	°
Viewing Angle - Right	-		-	30	-	°
Contrast Ratio	Cr	-	-	3	-	-
Response Time (rise)	Tr	-	-	200	300	ms
Response Time (fall)	Tf	-	-	150	200	ms

Controller Information

Built-in S1D13700 controller.

Please download specification at http://www.newhavendisplay.com/app_notes/S1D13700.pdf

Table of Commands

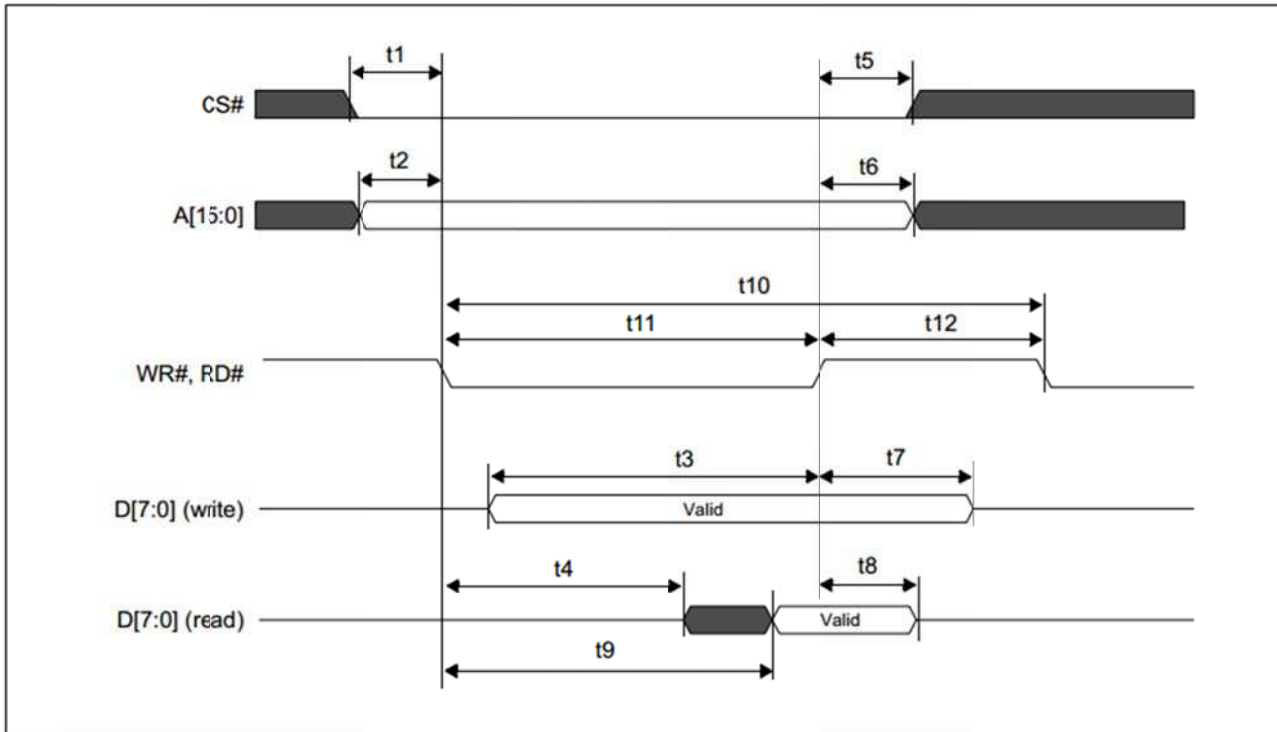
REG[01h] Horizontal Character Size Register																							
Address = 8001h Default = 00h																							
Read/Write																							
<table><tr><td colspan="2">MOD</td><td colspan="2">n/a</td><td colspan="4">Horizontal Character Size bits 3-0</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								MOD		n/a		Horizontal Character Size bits 3-0				7	6	5	4	3	2	1	0
MOD		n/a		Horizontal Character Size bits 3-0																			
7	6	5	4	3	2	1	0																
REG[02h] Vertical Character Size Register																							
Address = 8002h Default = 00h																							
Read/Write																							
<table><tr><td colspan="4">n/a</td><td colspan="4">Vertical Character Size bits 3-0</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								n/a				Vertical Character Size bits 3-0				7	6	5	4	3	2	1	0
n/a				Vertical Character Size bits 3-0																			
7	6	5	4	3	2	1	0																
REG[03h] Character Bytes Per Row Register																							
Address = 8003h Default = 00h																							
Read/Write																							
<table><tr><td colspan="8">Character Bytes Per Row bits 7-0</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								Character Bytes Per Row bits 7-0								7	6	5	4	3	2	1	0
Character Bytes Per Row bits 7-0																							
7	6	5	4	3	2	1	0																
REG[04h] Total Character Bytes Per Row Register																							
Address = 8004h Default = 00h																							
Read/Write																							
<table><tr><td colspan="8">Total Character Bytes Per Row bits 7-0</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								Total Character Bytes Per Row bits 7-0								7	6	5	4	3	2	1	0
Total Character Bytes Per Row bits 7-0																							
7	6	5	4	3	2	1	0																
REG[05h] Frame Height Register																							
Address = 8005h Default = 00h																							
Read/Write																							
<table><tr><td colspan="8">Frame Height bits 7-0</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								Frame Height bits 7-0								7	6	5	4	3	2	1	0
Frame Height bits 7-0																							
7	6	5	4	3	2	1	0																
REG[06h] Horizontal Address Range Register 0																							
Address = 8006h Default = 00h																							
Read/Write																							
<table><tr><td colspan="8">Horizontal Address Range bits 7-0</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								Horizontal Address Range bits 7-0								7	6	5	4	3	2	1	0
Horizontal Address Range bits 7-0																							
7	6	5	4	3	2	1	0																
REG[07h] Horizontal Address Range Register 1																							
Address = 8007h Default = 00h																							
Read/Write																							
<table><tr><td colspan="8">Horizontal Address Range bits 15-8</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								Horizontal Address Range bits 15-8								7	6	5	4	3	2	1	0
Horizontal Address Range bits 15-8																							
7	6	5	4	3	2	1	0																
REG[08h] Power Save Mode Register																							
Address = 8008h Default = 01h																							
Read/Write																							
<table><tr><td colspan="7">n/a</td><td>Power Save Mode Enable</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								n/a							Power Save Mode Enable	7	6	5	4	3	2	1	0
n/a							Power Save Mode Enable																
7	6	5	4	3	2	1	0																
REG[09h] Display Enable Register																							
Address = 8009h Default = 00h																							
Read/Write																							
<table><tr><td colspan="7">n/a</td><td>Display Enable</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								n/a							Display Enable	7	6	5	4	3	2	1	0
n/a							Display Enable																
7	6	5	4	3	2	1	0																
REG[0Ah] Display Attribute Register																							
Address = 800Ah Default = 00h																							
Read/Write																							
<table><tr><td colspan="2">SAD3 Attribute bits 1-0</td><td colspan="2">SAD2 Attribute bits 1-0</td><td colspan="2">SAD1 Attribute bits 1-0</td><td colspan="2">Cursor Attribute bits 1-0</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								SAD3 Attribute bits 1-0		SAD2 Attribute bits 1-0		SAD1 Attribute bits 1-0		Cursor Attribute bits 1-0		7	6	5	4	3	2	1	0
SAD3 Attribute bits 1-0		SAD2 Attribute bits 1-0		SAD1 Attribute bits 1-0		Cursor Attribute bits 1-0																	
7	6	5	4	3	2	1	0																
REG[0Bh] Screen Block 1 Start Address Register 0																							
Address = 800Bh Default = 00h																							
Read/Write																							
<table><tr><td colspan="8">Screen Block 1 Start Address bits 7-0 (LSB)</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								Screen Block 1 Start Address bits 7-0 (LSB)								7	6	5	4	3	2	1	0
Screen Block 1 Start Address bits 7-0 (LSB)																							
7	6	5	4	3	2	1	0																
REG[0Ch] Screen Block 1 Start Address Register 1																							
Address = 800Ch Default = 00h																							
Read/Write																							
<table><tr><td colspan="8">Screen Block 1 Start Address bits 15-8 (MSB)</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								Screen Block 1 Start Address bits 15-8 (MSB)								7	6	5	4	3	2	1	0
Screen Block 1 Start Address bits 15-8 (MSB)																							
7	6	5	4	3	2	1	0																
REG[0Dh] Screen Block 1 Size Register																							
Address = 800Dh Default = 00h																							
Read/Write																							
<table><tr><td colspan="8">Screen Block 1 Size bits 7-0</td></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>								Screen Block 1 Size bits 7-0								7	6	5	4	3	2	1	0
Screen Block 1 Size bits 7-0																							
7	6	5	4	3	2	1	0																

REG[0Eh] Screen Block 2 Start Address Register 0							
Address = 800Eh Default = 00h							
Read/Write							
Screen Block 2 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0
REG[0Fh] Screen Block 2 Start Address Register 1							
Address = 800Fh Default = 00h							
Read/Write							
Screen Block 2 Start Address bits 15-8 (MSB)							
7	6	5	4	3	2	1	0
REG[10h] Screen Block 2 Size Register							
Address = 8010h Default = 00h							
Read/Write							
Screen Block 2 Size bits 7-0							
7	6	5	4	3	2	1	0
REG[11h] Screen Block 3 Start Address Register 0							
Address = 8011h Default = 00h							
Read/Write							
Screen Block 3 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0
REG[12h] Screen Block 3 Start Address Register 1							
Address = 8012h Default = 00h							
Read/Write							
Screen Block 3 Start Address bits 15-8 (MSB)							
7	6	5	4	3	2	1	0
REG[13h] Screen Block 4 Start Address Register 0							
Address = 8013h Default = 00h							
Read/Write							
Screen Block 4 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0
REG[14h] Screen Block 4 Start Address Register 1							
Address = 8014h Default = 00h							
Read/Write							
Screen Block 4 Start Address bits 15-8 (MSB)							
7	6	5	4	3	2	1	0
REG[15h] Cursor Width Register							
Address = 8015h Default = 00h							
Read/Write							
n/a				Cursor Width bits 3-0			
7	6	5	4	3	2	1	0
REG[16h] Cursor Height Register							
Address = 8016h Default = 00h							
Read/Write							
Cursor Mode	n/a			Cursor Height bits 3-0			
7	6	5	4	3	2	1	0
REG[17h] Cursor Shift Direction Register							
Address = 8017h Default = 00h							
Read/Write							
n/a				Cursor Shift Direction bits 1-0			
7	6	5	4	3	2	1	0
REG[18h] Overlay Register							
Address = 8018h Default = 00h							
Read/Write							
n/a			3 Layer Overlay Select	Screen Block 3 Display Mode	Screen Block 1 Display Mode	Layer Composition Method bits 1-0	
7	6	5	4	3	2	1	0
REG[19h] Character Generator RAM Start Address Register 0							
Address = 8019h Default = 00h							
Read/Write							
CGRAM Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0
REG[1Ah] Character Generator RAM Start Address Register 1							
Address = 801Ah Default = 00h							
Read/Write							
CGRAM Start Address bits 15-8 (MSB)							
7	6	5	4	3	2	1	0
REG[1Bh] Horizontal Pixel Scroll Register							
Address = 801Bh Default = 00h							
Read/Write							
n/a				Horizontal Pixel Scroll bits 2-0			
7	6	5	4	3	2	1	0

REG[1Ch] Cursor Write Register 0							
Address = 801Ch Default = 00h							
Write Only							
Cursor Write bits 7-0 (LSB)							
7	6	5	4	3	2	1	0
REG[1Dh] Cursor Write Register 1							
Address = 801Dh Default = 00h							
Write Only							
Cursor Write bits 15-8 (MSB)							
7	6	5	4	3	2	1	0
REG[1Eh] Cursor Read Register 0							
Address = 801Eh Default = 00h							
Read Only							
Cursor Read bits 7-0 (LSB)							
7	6	5	4	3	2	1	0
REG[1Fh] Cursor Read Register 1							
Address = 801Fh Default = 00h							
Read Only							
Cursor Read bits 15-8 (MSB)							
7	6	5	4	3	2	1	0
REG[20h] Bit-Per-Pixel Select Register							
Address = 8020h Default = 00h							
Read/Write							
n/a						Bit-Per-Pixel Select bits 1-0	
7	6	5	4	3	2	1	0

Timing Characteristics

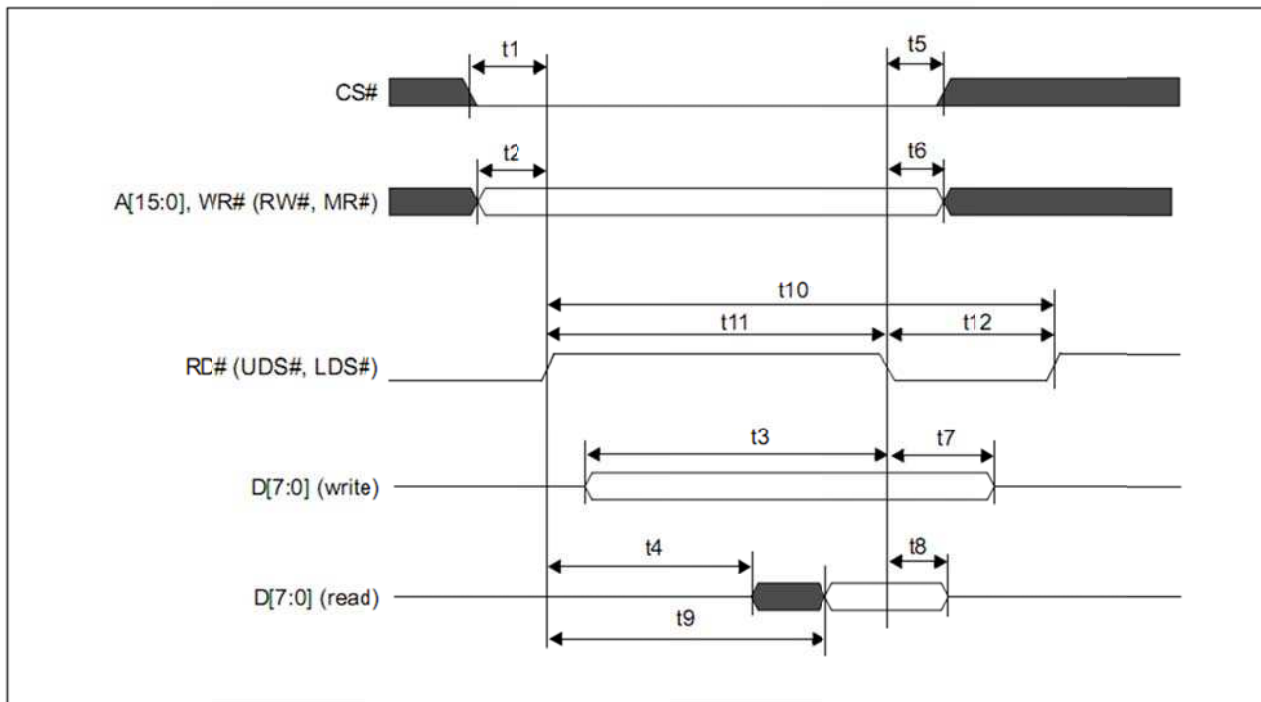
8080 Family Bus Interface Timing



Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	D[7:0] setup time to WR# rising edge (write cycle)	Note 2	—	Note 2	—	ns
t4	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t5	CS# hold time	7	—	7	—	ns
t6	A[15:0] hold time	7	—	7	—	ns
t7	D[7:0] hold time from WR# rising edge (write cycle)	5	—	5	—	ns
t8	D[7:0] hold time from RD# rising edge (read cycle)	3	14	3	14	ns
t9	RD# falling edge to valid Data (read cycle)	—	Note 3	—	Note 3	ns
t10	RD#, WR# cycle time	Note 4	—	Note 4	—	ns
t11	RD#, WR# pulse active time	5	—	5	—	Ts
t12	RD#, WR# pulse inactive time	Note 5	—	Note 5	—	ns

1. Ts = System clock period
2. t3min = 2Ts + 5
3. t9max = 4Ts + 18 (for 3.3V)
= 4Ts + 20 (for 5.0V)
4. t10min = 6Ts (for a read cycle followed by a read or write cycle)
= 7Ts + 2 (for a write cycle followed by a write cycle)
= 10Ts + 2 (for a write cycle followed by a read cycle)
5. t12min = 1Ts (for a read cycle followed by a read or write cycle)
= 2Ts + 2 (for a write cycle followed by a write cycle)
= 5Ts + 2 (for a write cycle followed by a read cycle)

6800 Family Bus Interface Timing



Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	D[7:0] setup time to RD# falling edge (write cycle)	Note 2	—	Note 2	—	ns
t4	RD# rising edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t5	CS# hold time	7	—	7	—	ns
t6	A[15:0] hold time	7	—	7	—	ns
t7	D[7:0] hold time from RD# falling edge (write cycle)	5	—	5	—	ns
t8	D[7:0] hold time from RD# falling edge (read cycle)	2	55	2	55	ns
t9	RD# rising edge to valid Data	—	Note 3	—	Note 3	ns
t10	RD# cycle time	Note 4	—	Note 4	—	ns
t11	RD# pulse active time	5	—	5	—	Ts
t12	RD# pulse inactive time	Note 5	—	Note 5	—	ns

1. Ts = System clock period
2. t3min = 2Ts + 5
3. t9max = 4Ts + 18 (for 3.3V)
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4. t10min = 6Ts (for a read cycle followed by a read or write cycle)
= 7Ts + 2 (for a write cycle followed by a write cycle)
= 10Ts + 2 (for a write cycle followed by a read cycle)
5. t12min = 1Ts (for a read cycle followed by a read or write cycle)
= 2Ts + 2 (for a write cycle followed by a write cycle)
= 5Ts + 2 (for a write cycle followed by a read cycle)

Example Initialization Code

```
//-----

Sub Writecom
  Reset P3.0
  P1 = A
  Reset P3.1
  Reset P3.7
  Set P3.4
  Reset P3.4
  Set P3.7
  Set P3.1
End Sub

Sub Writedata
  Set P3.0
  P1 = A
  Reset P3.1
  Reset P3.7
  Set P3.4
  Reset P3.4
  Set P3.7
  Set P3.1
End Sub

//-----

Sub Init
  Set P3.2
  Reset P3.6
  Waitms 10
  Set P3.6
  Waitms 100

  A = &H40
  Call Writecom
  A = &H30
  Call Writedata
  A = &H87
  Call Writedata
  A = &H07
  Call Writedata
  A = &H27
  Call Writedata
  A = &H50
  Call Writedata
  A = &HEF
  Call Writedata
  A = &H28
  Call Writedata
  A = &H00
  Call Writedata
  A = &H44
  Call Writecom
  A = &H00
  Call Writedata
  A = &H00
  Call Writedata
  A = &HEF
  Call Writedata
  A = &HB0
  Call Writedata
  A = &H04
  Call Writedata

  'A0 = L = Write command
  'move data to P1
  'chip select
  'R/W
  'E
  'E
  'R/W
  'CS

  'A0 = H = Write data

  'SEL=1 = Motorola 6800 interface
  'RESET
  'wait
  'RESET done
  'wait

  'system set command
  'set parameters
  'horizontal character size=8
  'vertical character size=8
  'display addresses per line
  'total address range per line
  '240 display lines
  'virtual address1
  'virtual address2
  'scroll
  'start address1
  'start address2
  '240 lines
  '2nd screen start1
  '2nd screen start2
```

A = &HEF	'2nd screen 240 lines
Call Writedata	
A = &H00	'3rd screen address1
Call Writedata	
A = &H00	'3rd screen address2
Call Writedata	
A = &H00	'4th screen address1
Call Writedata	
A = &H00	'4th screen address2
Call Writedata	
A = &H5A	'hdot scr
Call Writecom	
A = &H00	'horizontal pixel shift=0
Call Writedata	
A = &H5B	'overlay
Call Writecom	
A = &H00	'OR
Call Writedata	
A = &H5D	'cursor form
Call Writecom	
A = &H04	'5 pixels
Call Writedata	
A = &H86	'by 7 pixels
Call Writedata	
A = &H4C	'cursor direction = right
Call Writecom	
Call Clr	'clear the screen
A = &H59	'disp on/off
Call Writecom	
A = &H14	'on
Call Writedata	
End Sub	
//-----	

Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+80°C , 96hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C , 96hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time.	+70°C, 96hrs	2
Low Temperature Operation	Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time.	-20°C , 96hrs	1,2
High Temperature / Humidity Operation	Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time.	+60°C , 90% RH , 96hrs	1,2
Thermal Shock resistance	Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress.	-20°C,30min -> 25°C,5min -> 70°C,30min = 1 cycle 10 cycles	
Vibration test	Endurance test applying vibration to simulate transportation and use.	10-55Hz , 15mm amplitude. 60 sec in each of 3 directions X,Y,Z For 15 minutes	3
Static electricity test	Endurance test applying electric static discharge.	VS=800V, RS=1.5kΩ, CS=100pF One time	

Note 1: No condensation to be observed.

Note 2: Conducted after 4 hours of storage at 25°C, 0%RH.

Note 3: Test performed on product itself, not inside a container.

Precautions for using LCDs/LCMs

See Precautions at www.newhavendisplay.com/specs/precautions.pdf

Warranty Information

See Terms & Conditions at http://www.newhavendisplay.com/index.php?main_page=terms