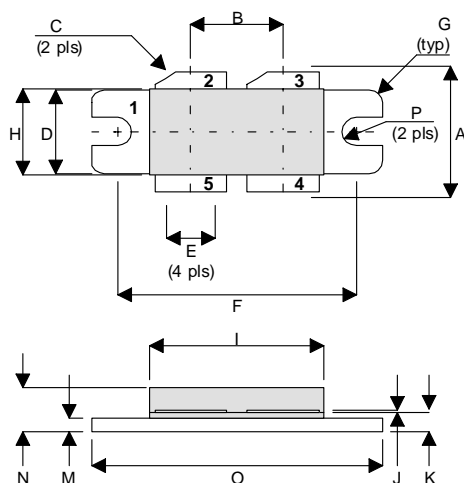


**MECHANICAL DATA**



**D1**

PIN 1	SOURCE (COMMON)	PIN 2	DRAIN 1
PIN 3	DRAIN 2	PIN 4	GATE 2
PIN 5	GATE 1		

DIM	Millimetres	Tol.	Inches	Tol.
A	15.24	0.50	0.600	0.020
B	10.80	0.13	0.425	0.005
C	45°	5°	45°	5°
D	9.78	0.13	0.385	0.005
E	8.38	0.13	0.330	0.005
F	27.94	0.13	1.100	0.005
G	1.52R	0.13	0.060R	0.005
H	10.16	0.15	0.400	0.006
I	21.84	0.23	0.860	0.009
J	0.10	0.02	0.004	0.001
K	1.96	0.13	0.077	0.005
M	1.02	0.13	0.040	0.005
N	4.45	0.38	0.175	0.015
O	34.04	0.13	1.340	0.005
P	1.63R	0.13	0.064R	0.005

**GOLD METALLISED**  
**MULTI-PURPOSE SILICON**  
**DMOS RF FET**  
**125W – 28V – 500MHz**  
**PUSH-PULL**

**FEATURES**

- SUITABLE FOR BROAD BAND APPLICATIONS
- SIMPLE BIAS CIRCUITS
- ULTRA-LOW THERMAL RESISTANCE
- BeO FREE
- LOW Crss
- HIGH GAIN – 13 dB MINIMUM

**APPLICATIONS**

- VHF/UHF COMMUNICATIONS  
from 1 MHz to 500 MHz

$P_D$	Power Dissipation	648W (389W -A Version)
$BV_{DSS}$	Drain – Source Breakdown Voltage *	70V
$BV_{GSS}$	Gate – Source Breakdown Voltage*	±20V
$I_{D(sat)}$	Drain Current*	20A
$T_{stg}$	Storage Temperature	-65 to 150°C
$T_j$	Maximum Operating Junction Temperature	200°C

\* Per Side

Semelab Plc reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.

### ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25°C unless otherwise stated)

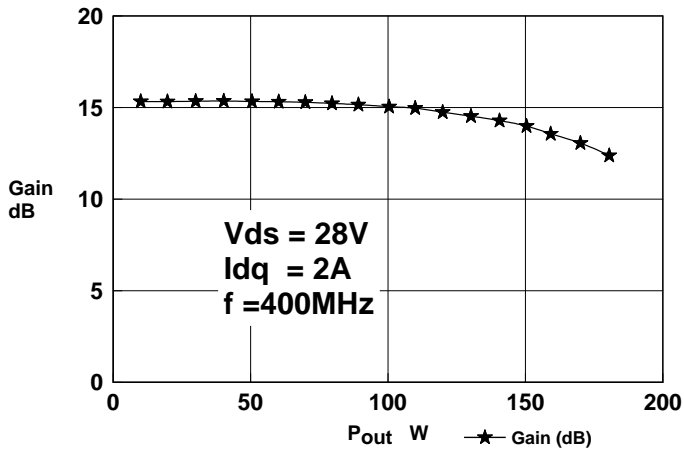
Parameter		Test Conditions		Min.	Typ.	Max.	Unit
<b>PER SIDE</b>							
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0	I <sub>D</sub> = 100mA	70			V
I <sub>D</sub> DSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 28V	V <sub>GS</sub> = 0			4	mA
I <sub>G</sub> DSS	Gate Leakage Current	V <sub>GS</sub> = 20V	V <sub>DS</sub> = 0			1	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage*	I <sub>D</sub> = 10mA	V <sub>DS</sub> = V <sub>GS</sub>	1		7	V
g <sub>fs</sub>	Forward Transconductance*	V <sub>DS</sub> = 10V	I <sub>D</sub> = 4A	3.2			mhos
V <sub>GS(th)match</sub>	Gate Threshold Voltage Matching Between Sides	I <sub>D</sub> = 1A	V <sub>DS</sub> = V <sub>GS</sub>			0.1	V
<b>TOTAL DEVICE</b>							
G <sub>PS</sub>	Common Source Power Gain	P <sub>O</sub> = 125W		13			dB
η	Drain Efficiency	V <sub>DS</sub> = 28V I <sub>DQ</sub> = 2A		50			%
VSWR	Load Mismatch Tolerance	f = 400MHz		20:1			—
<b>PER SIDE</b>							
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 28V	V <sub>GS</sub> = -5V f = 1MHz			240	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 28V	V <sub>GS</sub> = 0 f = 1MHz			100	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	V <sub>DS</sub> = 28V	V <sub>GS</sub> = 0 f = 1MHz			10	pF

\* Pulse Test: Pulse Duration = 300 μs , Duty Cycle ≤ 2%

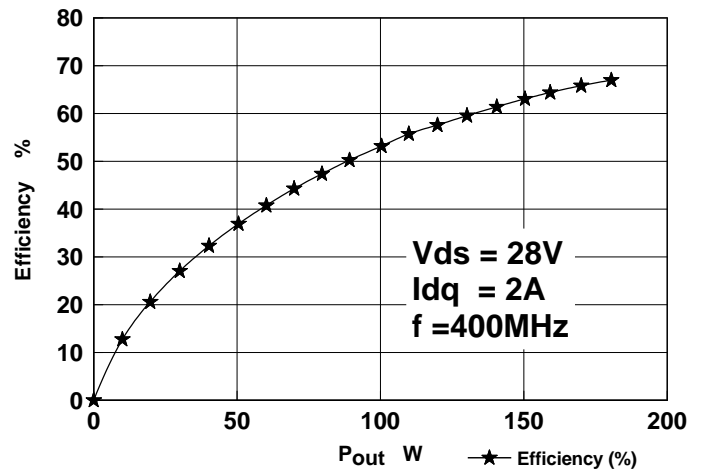
### THERMAL DATA

R <sub>THj-case</sub>	Thermal Resistance Junction – Case	Max. 0.27°C / W 0.45 °C / W -A Version
-----------------------	------------------------------------	---

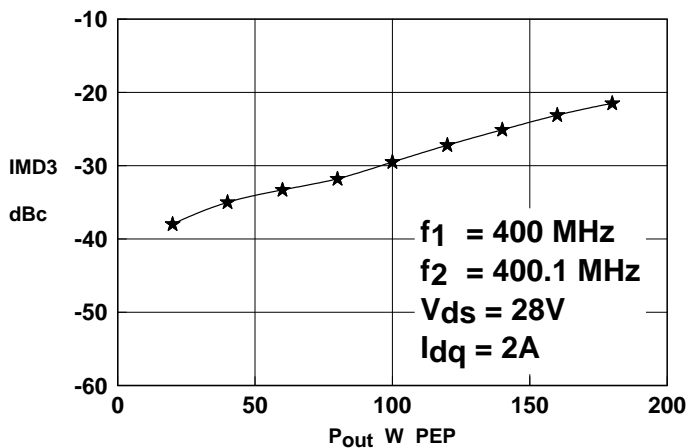
Semelab Plc reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.



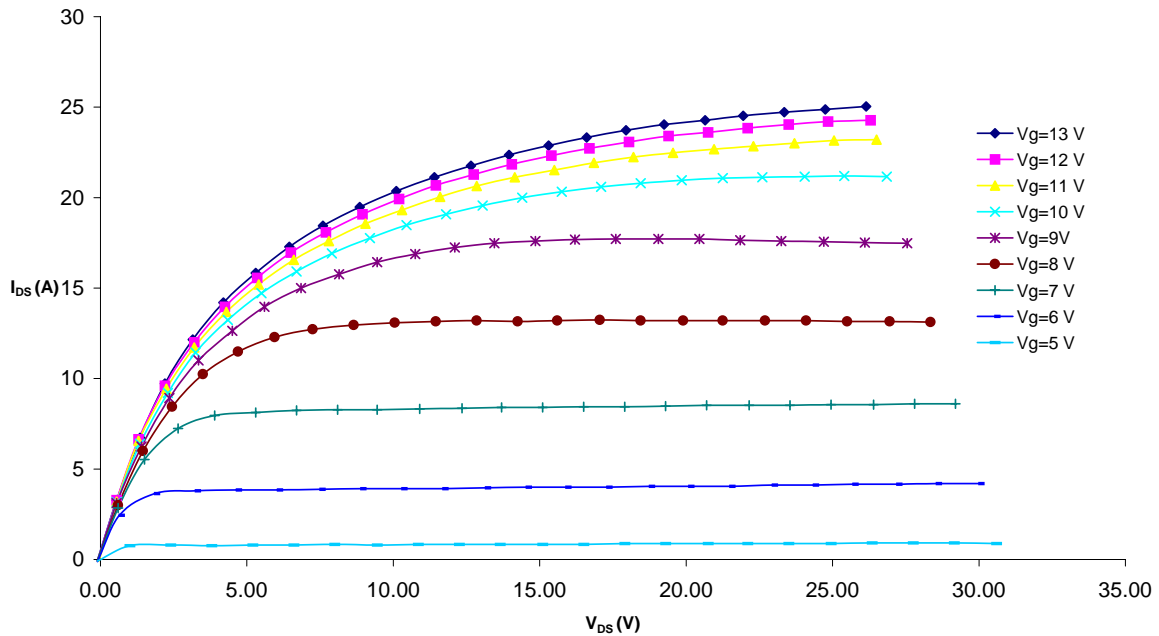
**Figure 1 – Gain vs. Power Output.**



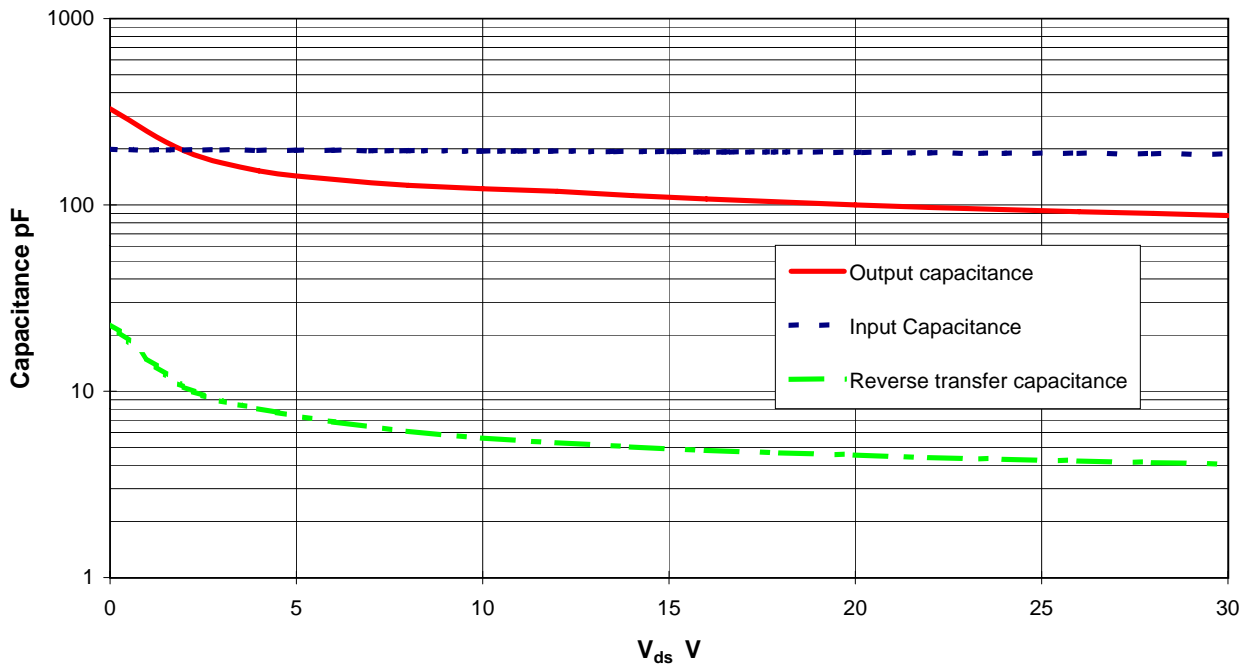
**Figure 2 – Efficiency vs. Power Output.**



**Figure 3 – IMD vs. Power Output**

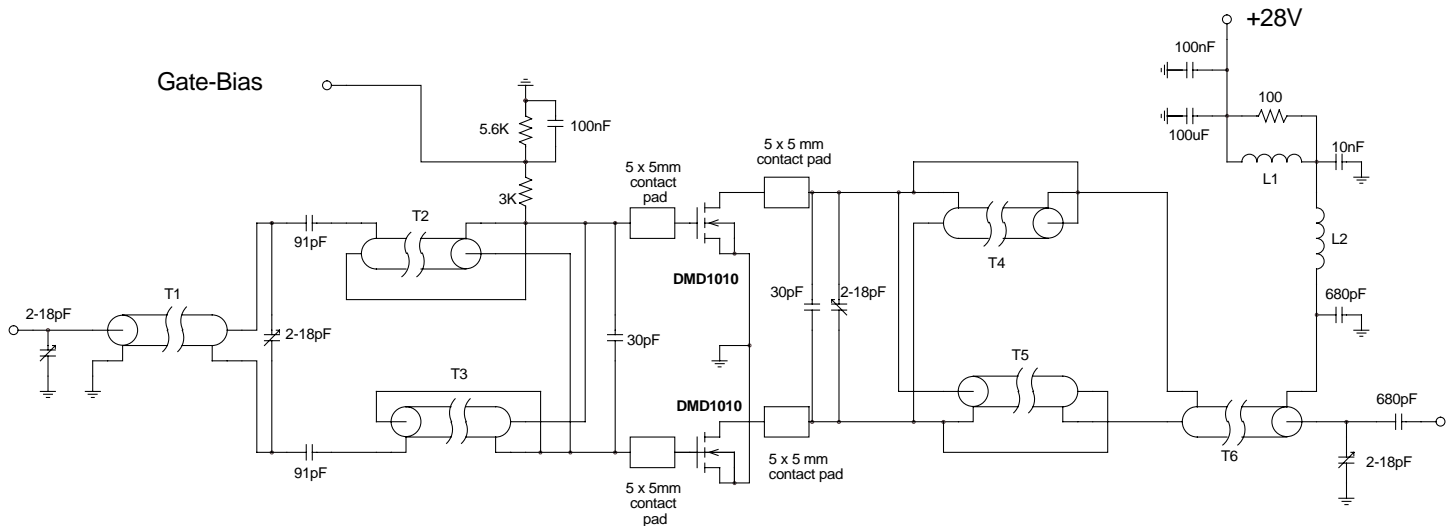


**Figure 4 – Typical IV Characteristics.**



**Figure 5 – Typical CV Characteristics.**

Semelab Plc reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.



## DMD1010 TEST FIXTURE

Substrate 1.6mm PTFE/ glass,  $\epsilon_r = 2.5$   
 All microstrip lines  $W = 4.4\text{mm}$

T1	12cm	50 $\Omega$ UT85 semi-rigid coax on ferrite core
T2,3	7.5cm	15 $\Omega$ UT85-15 semi-rigid coax
T4,5	7cm	15 $\Omega$ UT85-15 semi-rigid coax
T6	11cm	50 $\Omega$ UT85 semi-rigid coax on ferrite core
L1	6.5 turns	25swg enamelled copper wire on Fair-Rite FT50B-43 core
L2	6.5 turns	25swg enamelled copper wire, 4mm internal diameter

Semelab Plc reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.