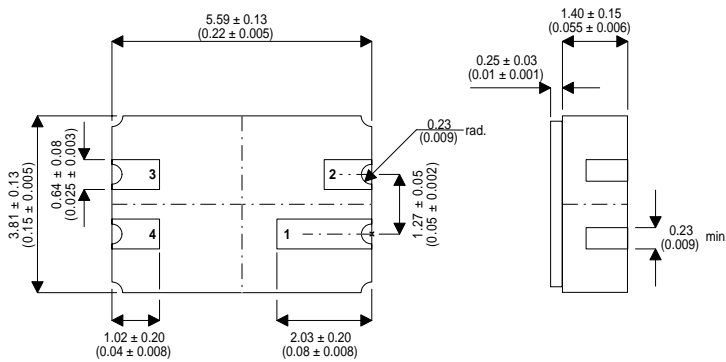


P-CHANNEL ENHANCEMENT MODE MOSFET

MECHANICAL DATA

Dimensions in mm (inches)



LCC3 PACKAGE (MO-041BA) Underside View

PAD 1 - Drain PAD 3 - Source
PAD 2 - N/C PAD 4 - Gate

FEATURES

- $B_{VDSS} = -60V$
- $I_D = -2.5A$
- $R_{DS(ON)} = 0.3\Omega$
- Hermetic Surface Mount Package
- Screening Option Available

The SML2955CSM4 is a very low on state resistance P-Channel enhancement mode mosfet in a Ceramic Surface Mount package designed for high rel applications:

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise stated)

V_{DS}	Drain – Source Voltage	-60V
V_{GS}	Gate – Source Voltage	$\pm 20V$
I_D	Continuous Drain Current @ $T_A = 25^\circ C$	-2.5A
I_{DM}	Pulsed Drain Current ¹	-15A
P_D	Power Dissipation @ $T_A = 25^\circ C$	0.8W
	@ $T_A = 100^\circ C$	0.32W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	156°C/W
T_{STG}, T_J	Maximum Junction and Storage Temperature Range	-55 to +150°C

NOTE:

- 1) Repetitive Rating: Pulse Width limited by maximum junction temperature.

Semelab Plc reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.

ELECTRICAL RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise stated)

Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
STATIC CHARACTERISTICS					
$V_{(BR)DSS}$ Drain – Source Breakdown Voltage	$V_{GS} = 0V$ $I_D = -250\mu A$	-60			V
$V_{GS(TH)}$ Gate Threshold Voltage ¹	$V_{DS} = V_{GS}$ $I_D = -250\mu A$	-2.0	-2.6	-4.0	
I_{GSS} Gate – Source Leakage Current	$V_{GS} = \pm 20V$ $V_{DS} = 0V$			± 100	nA
I_{DSS} Zero Gate Voltage Drain Current	$V_{DS} = -60V$ $V_{GS} = 0V$			-10	μA
$I_{D(ON)}$ On State Drain Current ¹	$V_{DS} = -5.0V$ $V_{GS} = -10V$	-12			A
$R_{DS(ON)}$ Drain Source On-State Resistance ¹	$I_D = -2.0A$ $V_{GS} = -4.5V$			0.55	Ω
	$I_D = -2.5A$ $V_{GS} = -10V$			0.35	
	$T_J = 125^\circ\text{C}$			0.55	
g_{fs} Forward Transconductance ¹	$V_{GS} = -10V$ $I_D = -2.5A$		5.5		S
V_{SD} Diode Forward Voltage ¹	$V_{GS} = 0V$ $I_D = -2.5A$		-0.8	-1.2	V
DYNAMIC CHARACTERISTICS					
C_{iss} Input capacitance	$V_{DS} = -30V$ $f = 1.0\text{MHz}$ $V_{GS} = 0V$		601		pF
C_{oss} Output capacitance			85		
C_{riss} Reverse transfer capacitance			35		
SWITCHING CHARACTERISTICS					
Q_g Total Gate Charge	$V_{DS} = -30V$ $I_D = -2.5A$ $V_{GS} = -10V$		11	15	nC
Q_{gs} Gate-Source Charge			2.4		
Q_{gd} Gate-Drain Charge			2.7		
$t_{d(on)}$ Turn-on Delay Time	$I_D = -1.0A$ $V_{DD} = -30V$ $V_{GS} = -10V$ $R_{GEN} = 6\Omega$		12	21	ns
t_r Rise Time			10	20	
$t_{d(off)}$ Turn-off Delay Time			19	34	
t_f Fall Time			6	12	

NOTES:

- 1) Pulse Test: Pulse Width = $300\mu s$, Duty Cycle $\leq 2\%$