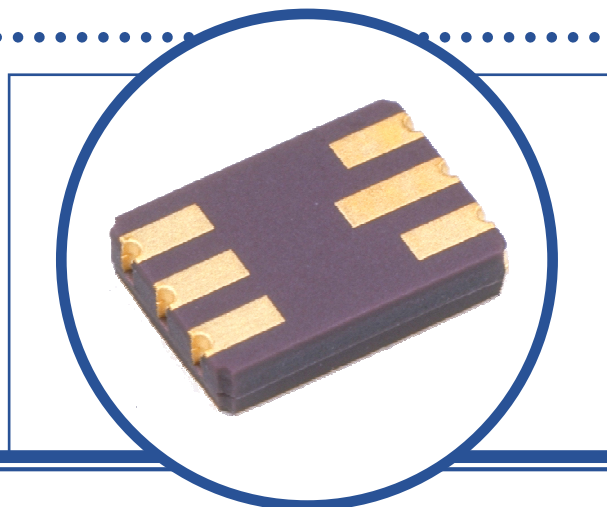


SILICON DUAL MATCHED NPN TRANSISTORS

2N2920ADCSM

- Dual Silicon NPN Matched Transistors
- Hermetic Ceramic Surface Mount Package
- Designed For Low Noise, Differential Amplifier Applications.
- Screening Options Available



ABSOLUTE MAXIMUM RATINGS (Each Side, $T_A = 25^\circ\text{C}$ unless otherwise stated)

		Each Side	Total Device
V_{CBO}	Collector – Base Voltage	60V	
V_{CEO}	Collector – Emitter Voltage	60V	
V_{EBO}	Emitter – Base Voltage	6V	
I_C	Continuous Collector Current	30mA	
P_D	Total Power Dissipation at $T_A = 25^\circ\text{C}$ Derate Above 25°C	300mW 1.71mW/ $^\circ\text{C}$	500mW ⁽¹⁾ 2.86mW/ $^\circ\text{C}$
T_J	Junction Temperature Range	-65 to +200 $^\circ\text{C}$	
T_{stg}	Storage Temperature Range	-65 to +200 $^\circ\text{C}$	

THERMAL PROPERTIES

Symbols	Parameters	Max.	Units
$R_{\theta JA}$	Each Side - Thermal Resistance, Junction To Ambient	583.3	$^\circ\text{C/W}$
$R_{\theta JA}^{(1)}$	Total Device - Thermal Resistance, Junction To Ambient	350	$^\circ\text{C/W}$

Notes

(1) Total device power dissipation limited by package.

SILICON DUAL MATCHED NPN TRANSISTORS 2N2920ADCSM

ELECTRICAL CHARACTERISTICS (Each Side, $T_A = 25^\circ\text{C}$ unless otherwise stated)

Symbols	Parameters	Test Conditions	Min.	Typ.	Max.	Units
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 10\mu\text{A}$ $I_E = 0$	60			V
$V_{(BR)CEO}^{(2)}$	Collector-Emitter Breakdown Voltage	$I_C = 10\text{mA}$ $I_B = 0$	60			
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 10\mu\text{A}$ $I_C = 0$	6			
I_{CEO}	Collector Cut-Off Current	$V_{CE} = 5\text{V}$			2	nA
I_{CBO}	Collector Cut-Off Current	$V_{CB} = 45\text{V}$ $T_A = 150^\circ\text{C}$			10	
I_{EBO}	Emitter Cut-Off Current	$V_{EB} = 5\text{V}$			2	nA
h_{FE}	Forward-current transfer ratio	$I_C = 10\mu\text{A}$ $V_{CE} = 5\text{V}$ $T_A = -55^\circ\text{C}$	150		600	
		$I_C = 100\mu\text{A}$ $V_{CE} = 5\text{V}$	225			
		$I_C = 1.0\text{mA}$ $V_{CE} = 5\text{V}$	300			
$V_{CE(sat)}^{(2)}$	Collector-Emitter Saturation Voltage	$I_C = 1.0\text{mA}$ $I_B = 0.1\text{mA}$			0.35	V
$V_{BE(sat)}^{(2)}$	Base-Emitter Saturation Voltage	$I_C = 1.0\text{mA}$ $I_B = 0.1\text{mA}$	0.5		1.0	

ELECTRICAL MATCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise stated)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$\frac{h_{FE1}}{h_{FE2}}$	Forward-current transfer ratio (gain ratio)	$I_C = 100\mu\text{A}$ $V_{CE} = 5\text{V}$	0.9		1.0	
		$T_A = -55^\circ\text{C}$	0.85		1.18	
		$T_A = 125^\circ\text{C}$	0.85		1.18	
$ V_{BE1} - V_{BE2} $	Base-Emitter Voltage Differential	$I_C = 10\mu\text{A}$ $V_{CE} = 5\text{V}$			2	mV
		$I_C = 100\mu\text{A}$ $V_{CE} = 5\text{V}$			1.5	
		$I_C = 1.0\text{mA}$ $V_{CE} = 5\text{V}$			2	
$ \Delta(V_{BE1} - V_{BE2})_{\Delta T_A} ^{(3)}$	Base-Emitter Voltage Differential Change Due To Temperature	$I_C = 100\mu\text{A}$ $V_{CE} = 5\text{V}$ $T_{A1} = -55^\circ\text{C}$ $T_{A2} = 25^\circ\text{C}$			0.4	
		$I_C = 100\mu\text{A}$ $V_{CE} = 5\text{V}$ $T_{A1} = 25^\circ\text{C}$ $T_{A2} = 125^\circ\text{C}$			0.5	

Notes

- (2) Pulse Width $\leq 300\mu\text{s}$, $\delta \leq 2\%$
(3) By design only, not a production test

SILICON DUAL MATCHED NPN TRANSISTORS 2N2920ADCSM

DYNAMIC CHARACTERISTICS (Each Side, $T_A = 25^\circ\text{C}$ unless otherwise stated)

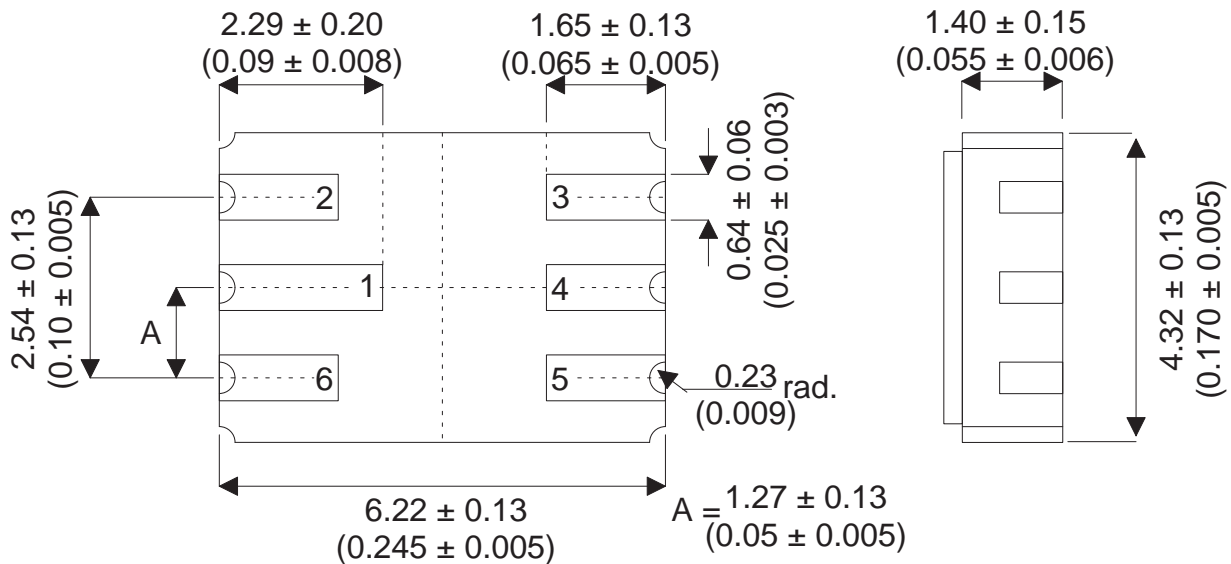
Symbols	Parameters	Test Conditions	Min.	Typ.	Max.	Units
f_T	Transition Frequency	$I_C = 500\mu\text{A}$ $V_{CE} = 5\text{V}$ $f = 20\text{MHz}$	60			MHz
C_{obo}	Output Capacitance	$V_{CB} = 5\text{V}$ $I_E = 0$ $f = 1.0\text{MHz}$			6	pF
$h_{oe}^{(3)}$	Output Admittance	$I_C = 1.0\text{mA}$ $V_{CE} = 5\text{V}$ $f = 1.0\text{KHz}$			40	μmhos
$h_{ie}^{(3)}$	Input Impedance		2		24	$\text{K}\Omega$
$h_{re}^{(3)}$	Reverse Voltage Ratio				800	$\times 10^{-6}$
$N_F^{(3)}$	Spot Noise Figure	$V_{CE} = 5\text{V}$ $I_C = 10\mu\text{A}$			3	dB
	Wide-Band Noise Figure	$R_G = 10\text{K}\Omega$			3	

Notes

(3) By design only, not a production test.

MECHANICAL DATA

Dimensions in mm (inches)



LCC2 (MO-041BB)

Underside View

Pad 1 – Collector 1 Pad 4 – Collector 2
Pad 2 – Base 1 Pad 5 – Emitter 2
Pad 3 – Base 2 Pad 6 – Emitter 1