95230

PROTEK DEVICES
ANALOG PRODUCTS DIVISION

PA5750

Low Power Stereo Audio CODEC With Speaker and Headphone Amplifier.

FEATURES

ADC
- 24-bit, 8 – 96 kHz sampling frequency
- 92dB dynamic range, 92dB signal to noise ratio, -85dB THD+N
- Stereo or Mono microphone interface with microphone amplifier
- Auto level control and noise gate
- 3 to1 analog input selection
- Analog input mixers and amplifiers

DAC
- 24-bit, 8 – 96 kHz sampling frequency
- 93dB dynamic range, 93dB signal to noise ratio, -81dB THD+N
- 500mWatt speaker amplifier
- 40mWatt headphone option, pop free, capless opt.
- Stereo enhancement
- Bass and Treble
- Analog output mixers and amplifiers.

Low Power
- 1.8 to 3.3Volt operation
- 7mWatt playback, 16mWatt playback and record.

System
- I^2C or SPI µC interface
- Headphone Detector
- 256Fs, 384Fs, USB 12MHz or 24MHz
- Master or Slave serial port
- I^2S, Left Justified, DSP/PCM Mode

APPLICATIONS

- MP3 Players / Recorders
- AAC/WMA/Multi Format Players
- Portable Digital Music Systems
- GPS
- Bluetooth

DESCRIPTION

The PA5750 is a high performance, low power and low cost Audio CODEC.

It consists of 2-channel ADC, 2-channel DAC, microphone amplifier, Speaker amplifier, headset amplifier, digital enhancements and analog mixing and amplification functions.

The PA5750 uses advanced multi-bit delta-sigma modulation techniques to convert DATA between digital and analog.
The multi-bit delta-sigma modulations decrease the sensitivity to clock jitter and low out of band noise.

The PA5750 can operate as the Master or the Slave with various clock frequencies including 12 or 24MHz for USB devices. Audio sample rates (44.1, 48 and 96kHz) are generated directly from the master clock.

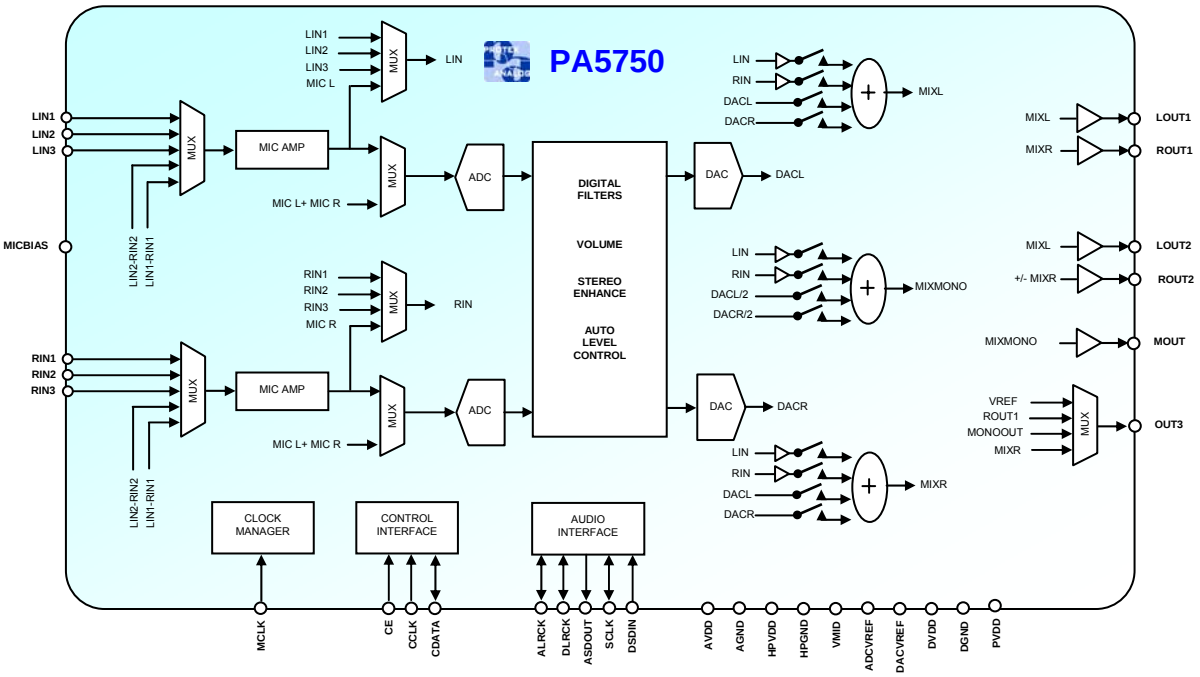
The PA5750 operates from 1.8V to 3.6V. Sections of the chip can be powered down by software control.

The PA5750 is offered in a 5x5mm QFN Package

ORDERING INFORMATION

Device No.	Package
PA5750	QFN-32

BLOCK DIAGRAM



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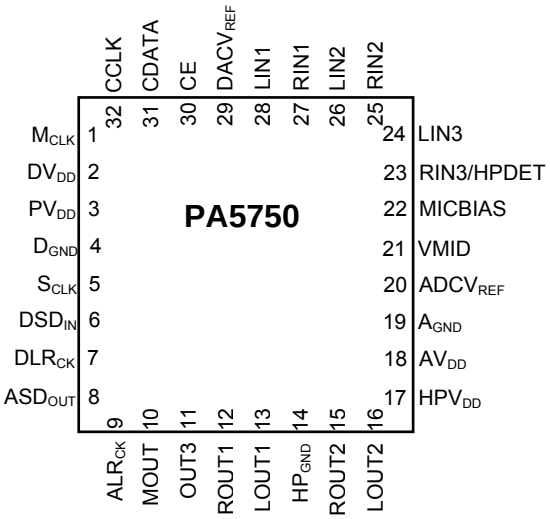
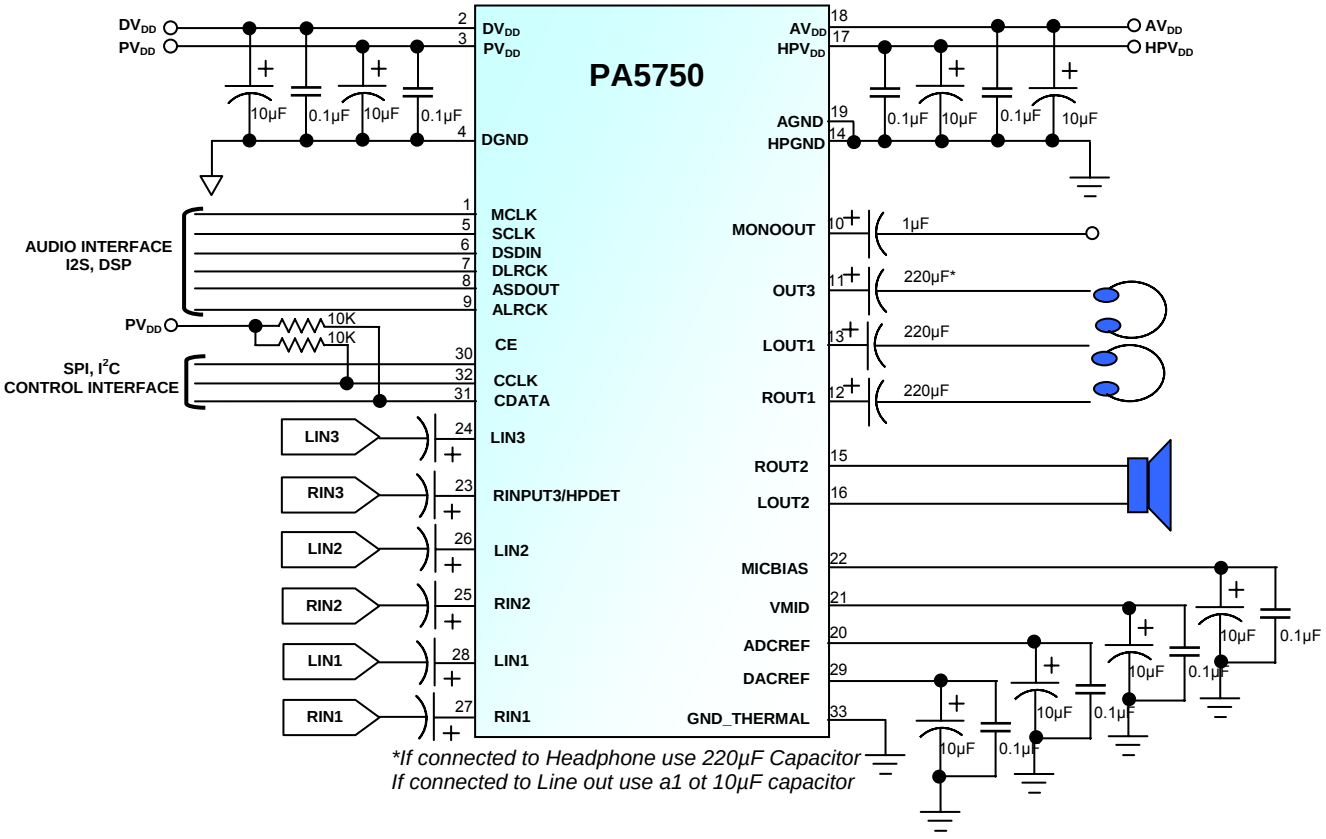
2. 32-PIN QFN LAYOUT AND PIN DESCRIPTIONS.



The PA5750 is PIN to PIN compatible with the WM8750 except PIN 29. Where PA5750 uses it as a reference pin, while the WM8750 uses it as a digital mode pin.

PIN	NAME	Designation	Description
1	MCLK	INPUT	Master Clock
2	DVDD	SUPPLY	Digital Core Supply
3	PVDD	SUPPLY	Digital Input, Output Supply
4	DGND	SUPPLY	Digital Ground (Return Path for DVDD and PVDD)
5	SCLK	I/O	Audio DATA Bit Clock
6	DSDIN	INPUT	DAC Audio DATA
7	DLRCK	I/O	DAC Audio DATA Left and Right Clock
8	ASDOUT	OUTPUT	ADC Audio DATA
9	ALRCK	I/O	ADC Audio Left and Right Clock
10	MOUT	OUTPUT	MONO Output
11	OUT3	OUTPUT	Analog Output 3 *(can be used as Headphone Pseudo Ground)*
12	ROUT1	OUTPUT	Right Output 1 *(line or speaker/headphone)*
13	LOUT2	OUTPUT	Left Output 1 *(line or speaker/headphone)*
14	HPGND	SUPPLY	Ground for Analog Output Drivers (LOUT1/2, ROUT1/2)
15	ROUT2	OUTPUT	Right Output 2 *(line or speaker/headphone)*
16	LOUT2	OUTPUT	Left Output 2 *(line or speaker/headphone)*
17	HPVDD	SUPPLY	Supply for Analog Output Drivers (LOUT1/2, ROUT1/2)
18	AVDD	SUPPLY	Analog Supply
19	AGND	SUPPLY	Analog Ground
20	ADCREF	OUTPUT	Connected to Decoupling Capacitor
21	VMID	OUTPUT	Connected to Decoupling Capacitor
22	MICBIAS	OUTPUT	Microphone Bias
23	RINPUT3/HPDET	INPUT	Right Channel Input 3 or Headphone plug-in detection
24	LIN3	INPUT	Left Channel Input 3
25	RIN2	INPUT	Right Channel Input 2
26	LIN2	INPUT	Left Channel Input 2
27	RIN1	INPUT	Right Channel Input 1
28	LIN1	INPUT	Left Channel Input 1
29	DACREF	OUTPUT	Connected to Decoupling capacitor
30	CE	INPUT	Control Select or Device Address Selection
31	CDATA	I/O	Control DATA Input or Output
32	CCLK	INPUT	Control Clock Input

3. TYPICAL APPLICATION CIRCUIT



4. CLOCK MODES AND SAMPLING FREQUENCIES.

According to the input serial audio DATA sampling frequency, the PA5750 can work in two speed modes. Single or double speed. The range of the sampling frequency in these two modes is listed in Table 1. The PA5750 can work in either master clock mode or in slave clock mode.

In slave mode, LRCK and SCLK are supplied externally. LRCK and SCLK must be synchronously derived from the system clock with a specific rate, The PA5750 can auto detect MCLK/LRCK ratio according to Table 1. The PA5750 only supports the MCLK/LRCK ratios listed in Table 1. The LRCK/SCLK ratio is normally 64.

Table 1 Slave Mode Sampling Frequencies and MCLK/SCLK Ratio.

Speed Mode	Sampling Frequency	MCLK/LRCK Ratio
Single Speed	8 kHz – 50 kHz	256, 384, 512, 768, 1024.
Double Speed	50 kHz – 100 kHz	128, 192, 256, 384, 512.

In master mode, LRCK and SCLK are internally derived from MCLK.
The available MCLK/LRCK ratios are listed in Table 2.

Table 2 Master Mode Sampling Frequencies and MCLK/LRCK Ratio.

MCLK CLKDIV2=0	MCLK CLKDIV2=1	ADC Sample Rate (ALRCK)	ADCFsRatio [4:0]	DAC Sample Rates (DLRCK)	DACFsRatio [4:0]	SCLK Ratio
Normal Mode						
12.288MHz	24.576MHz	8 kHz (MCLK/1536)	01010	8 kHz (MCLK/1536)	01010	MCLK/6
		8 kHz (MCLK/1536)	01010	48 kHz (MCLK/256)	00010	MCLK/4
		12 kHz (MCLK/1024)	00111	12 kHz (MCLK/1024)	00111	MCLK/4
		16 kHz (MCLK/768)	00110	16 kHz (MCLK/768)	00110	MCLK/6
		24 kHz (MCLK/512)	00100	24 kHz (MCLK/512)	00100	MCLK/4
		32 kHz (MCLK/384)	00011	32 kHz (MCLK/384)	00011	MCLK/6
		48 kHz (MCLK/256)	00010	8 kHz (MCLK/1536)	01010	MCLK/4
		48 kHz (MCLK/256)	00010	48 kHz (MCLK/256)	00010	MCLK/4
		96 kHz (MCLK/128)	00000	96 kHz (MCLK/128)	00000	MCLK/2
11.2896 MHz	22.5792 MHz	8.0182 kHz (MCLK/1408)	01001	8.0182 kHz (MCLK/1408)	01001	MCLK/4
		8.0182 kHz (MCLK/1408)	01001	44.1 kHz (MCLK/256)	00010	MCLK/4
		11.025 kHz (MCLK/1024)	00111	11.025 kHz (MCLK/1024)	00111	MCLK/4
		22.05 kHz (MCLK/512)	00100	22.05 kHz (MCLK/512)	00100	MCLK/4
		44.1 kHz (MCLK/256)	00010	8.0182 kHz (MCLK/1408)	01001	MCLK/4
		44.1 kHz (MCLK/256)	00010	44.1 kHz (MCLK/256)	00010	MCLK/4
		88.2 kHz (MCLK/128)	00000	88.2 kHz (MCLK/128)	00000	MCLK/2
18.432 MHz	36.864 MHz	8 kHz (MCLK/2304)	01100	8 kHz (MCLK/2304)	01100	MCLK/6
		8 kHz (MCLK/2304)	01100	48 kHz (MCLK/384)	00011	MCLK/6
		12 kHz (MCLK/1536)	01010	12 kHz (MCLK/1536)	01010	MCLK/6
		16 kHz (MCLK/1152)	01000	16 kHz (MCLK/1152)	01000	MCLK/6
		24 kHz (MCLK/768)	00110	24 kHz (MCLK/768)	00110	MCLK/6
		32 kHz (MCLK/576)	00101	32 kHz (MCLK/576)	00101	MCLK/6
		48 kHz (MCLK/384)	00011	8 kHz (MCLK/2304)	01100	MCLK/6
		48 kHz (MCLK/384)	00011	48 kHz (MCLK/384)	00011	MCLK/6
		96 kHz (MCLK/192)	00001	96 kHz (MCLK/192)	00001	MCLK/3
16.9344 MHz	33.8688 MHz	8.0182 kHz (MCLK/2112)	01011	8.0182 kHz (MCLK/2112)	01011	MCLK/6
		8.0182 kHz (MCLK/2112)	01011	44.1 kHz (MCLK/384)	00011	MCLK/6
		11.025 kHz (MCLK/1536)	01010	11.025 kHz (MCLK/1536)	01010	MCLK/6
		22.05 kHz (MCLK/768)	00110	22.05 kHz (MCLK/768)	00110	MCLK/6
		44.1 kHz (MCLK/384)	00011	8.0182 kHz (MCLK/2112)	01011	MCLK/6
		44.1 kHz (MCLK/384)	00011	44.1 kHz (MCLK/384)	00011	MCLK/6
		88.2 kHz (MCLK/192)	00001	88.2 kHz (MCLK/192)	00001	MCLK/3
USB Mode						
12 MHz	24 MHz	8 kHz (MCLK/1500)	11011	8 kHz (MCLK/1500)	11011	MCLK
		8 kHz (MCLK/1500)	11011	48 kHz (MCLK/250)	10010	MCLK
		8.0214 kHz (MCLK/1496)	11010	8.0214 kHz (MCLK/1496)	11010	MCLK
		8.0214 kHz (MCLK/1496)	11010	44.118 kHz (MCLK/272)	10011	MCLK
		11.0259 kHz (MCLK/1108)	11001	11.0259kHz (MCLK/1108)	11001	MCLK
		12 kHz (MCLK/1000)	11000	12 kHz (MCLK/1000)	11000	MCLK
		16 kHz (MCLK/750)	10111	16 kHz (MCLK/750)	10111	MCLK
		22.0588 kHz (MCLK/544)	10110	22.0588 kHz (MCLK/544)	10110	MCLK
		24 kHz (MCLK/500)	10101	24 kHz (MCLK/500)	10101	MCLK
		32 kHz (MCLK/375)	10100	32 kHz (MCLK/375)	10100	MCLK
		44.118 kHz (MCLK/272)	10011	8.0214 kHz (MCLK/1496)	11010	MCLK
		44.118 kHz (MCLK/272)	10011	44.118 kHz (MCLK/272)	10011	MCLK
		48 kHz (MCLK/250)	10010	8 kHz (MCLK/1500)	11011	MCLK
		48 kHz (MCLK/250)	10010	48 kHz (MCLK/250)	10010	MCLK
		88.235 kHz (MCLK/136)	10001	88.235 kHz (MCLK/136)	10001	MCLK
		48 kHz (MCLK/250)	10000	48 kHz (MCLK/250)	10000	MCLK

5. MICRO-CONTROLLER CONFIGURATION INTERFACE.

The PA5750 supports standard SPI and 2-wire micro-controller configuration interface. An External micro-controller can completely configure the PA5750 through writing to internal configuration registers. Chapter 8 describes in detail the configuration of the registers.

The identical pins are used to configure for either SPI or 2-wire interface.
In SPI mode, CE (Pin 30), CCLK (Pin 32) and CDATA (Pin 31) functions as SPI_CSn, SPI_CLK and SPI_DIN.
In 2-wire mode, CE (Pin 30), CCLK (Pin 32) and CDATA (Pin 31) functions as AD0, SCL and SDA respectively.

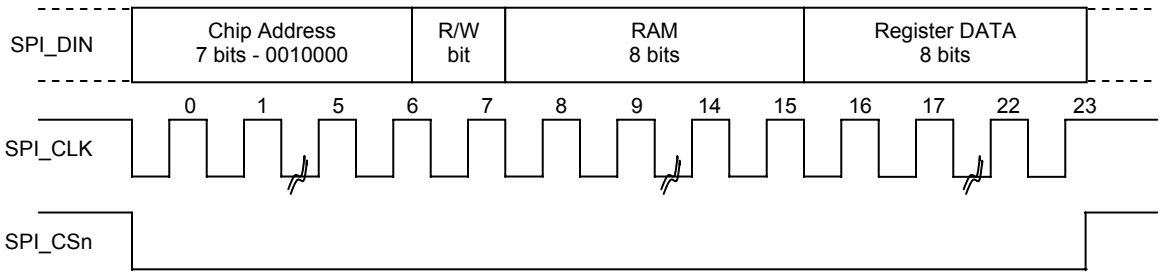
To select SPI mode, apply a high to low transition signal to CE (pin 30). If no signal is applied, the PA5750 will operate in 2-wire interface mode.

5.1 SPI

The PA5750 has a SPI (Serial Peripheral Interface) compliant synchronous serial slave controller internal to the chip. It provides the ability to allow the external master SPI controller to access the internal registers, thereby controlling the operation of the chip.

All lines on the SPI bus are unidirectional: The SPI_CLK is generated by the master controller and is primarily used to synchronize DATA transfer; the SPI_DIN line carries DATA from the master to the slave. SPI_CSn is generated by the master to select the PA5750.

The timing diagram of this interface is given in Fig. 1. The high to low transition at SPI_CSn (pin 30) indicates the SPI interface selected. Each write procedure contains 3 words, i.e. Chip Address plus R/W bit, internal register address and internal register DATA. Every word is fixed at 8 bits. The input SPI_DIN DATA is sampled at the rising edge of SPI_CLK clock. The MSB bit in each word is transferred first. The transfer rate can be up to 10Mbps.



RAM =Register Address Mapping
Fig.1 SPI Configuration Interface Timing Diagram.

5.2 2-wire Interface
2-wire interface is a bi-directional serial BUS that uses a serial data line (SDA) and a serial clock line (SCL) for DATA transfer. The timing diagram for DATA transfer is given in Fig. 2.

DATA is transmitted synchronously to SCL clock on the SDA line in a byte-by-byte basis. Each bit in a byte is sampled during SCL high with the MSB bit transferred first. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low.

The transfer rate of the 2-wire interface can be up to 100kbps.

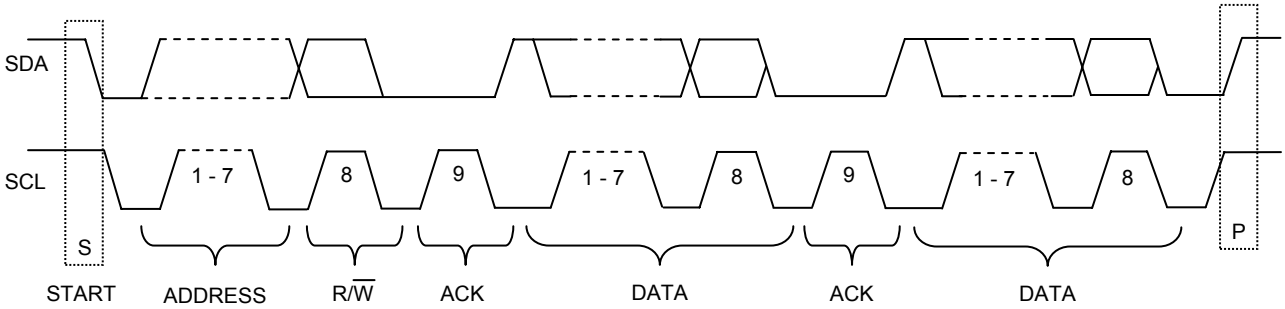


Fig. 2 Complete DATA Transfer for 2-wire Interface

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a R/W bit. The chip address must be 001000x where x = AD0 (pin CE). The R/W bit indicates the slave DATA transfer direction.
Once an acknowledge bit is received, the DATA transfer starts to procede on a byte-by-byte basis in the direction specified by the R/W bit. The master can terminate the communication by generating a “Stop” signal, which is defined as a low-to-high transition at SDA while SCL is high.

In 2-wire interface mode, the registers can be written to and read. The format of “write” and “Read” instructions are shown in Tables 3 and 4. To Read DATA from a register R/W must be set to “0” to access the register address and then set to “1” to read DATA in the register. There is NO acknowledge bit after data to be written or read, this is the only difference from the I^2C protocol.

Table 3 Write DATA to register in 2-wire Interface Mode

Chip Address		R/W		Register Address		DATA to be written
00100	AD0	0	ACK	RAM	ACK	DATA

Table 4 Read DATA from Register in 2-wire Interface Mode

Chip Address		R/W		Register Address
001000	AD0	0	ACK	RAM
Chip Address		R/W		DATA to be Read
001000	AD0	1	ACK	DATA

6. CONFIGURATION REGISTER DEFINITION
SPI and 2-wire configuration interface share the same registers because there is only one interface active at any given time. There are a total of 53 user programmable 8-bit registers in the PA5750. These registers control the operations of ADC and DAC. External master controller can access these registers by using the slave address specified in RAM (Register Address Map) register as shown in Table 5.

Table 5. Bit Content of Register Address Map (RAM)

	B7	B6	B5	B4	B3	B2	B1	B0
Reg. 00	SCPReset	LRCM	DACMCLK	SameFs	SeqEn	EnRef	VMIDSEL	
Reg. 01	TSDN	Pdn_OC	LPVcmMod	LPVrefBuf	Pdn_Ana	Pdn_Ibiasgen	Vrefr_Lo	Pdn_Vrefbuf
Reg. 02	adc_DigPDN	dac_DigPDN	adc_stm_rst	dac_stm_rst	ADCDLL_PDN	DACDLL_PDN	adcVref_PDN	dacVref_PDN
Reg. 03	Pdn_AINL	Pdn_AINR	Pdn_ADCL	Pdn_ADCR	Pdn_MICB	Pdn_ADCBiasgen	flashLP	int1LP
Reg. 04	Pdn_DACL	Pdn_DACR	LOUT1	ROUT1	LOUT2	ROUT2	MONO	OUT3
Reg. 05	LPDACL	LPDACR	LPLOUT1	LPROUT1	LPLOUT2	LPROUT2	LPMONO	LPOUT3
Reg. 06	LPPGA	LPLMIX	LPRMIX	LPMMIX	LPMOUTINV	LPOUT2INV	LPADCvrp	LPDACvrp
Reg. 07		VSEL						

	B7	B6	B5	B4	B3	B2	B1	B0
Reg. 08	MSC	MCLKDIV2	BCLK_INV	BCLKDIV				
Reg. 09	LPGAgain				RPGAgain			
Reg. 10	LINSEL		RINSEL					
Reg. 11	DS	LDCM	RDCM	MONOMIX		TRI	OC	
Reg. 12	DATSEL		ADCLRP	ADCWL			ADCFORMAT	
Reg. 13			ADC_FsMode	ADCFsRatio				
Reg. 14	ADC_invL	ADC-invR	ADC_HPF_L	ADC_HPF_R				
Reg. 15	ADCRampRate		ADCSoftRamp	ADCZeroCrs	ADCLeR	ADCMute		
Reg. 16	ADCGainL(LADCVOL)							
Reg. 17	ADCGainR(RADCVOL)							
Reg. 18	ALCSEL		MAXGAIN			MINGAIN		
Reg. 19	ALCLVL				ALCHLD			
Reg. 20	ALCDCY				ALCATK			
Reg. 21	ALCMODE	ALCZC	TIME_OUT	WIN_SIZE				
Reg. 22	NGTH					NGG		NGAT
Reg. 23	DACLRSWAP	DACLRP	DACWL			DACFORMAT		
Reg. 24			DACFsMode	DACFsRatio				
Reg. 25	DACRampRate		DAC SoftRamp	DACZeroCrs	DACLeR	DACMute	AutoMute	
Reg. 26	DACVolumeL (LDACVOL)							
Reg. 27	DACVolumeR (RDACVOL)							
Reg. 28	DeemphasisMode		DAC_invL	DAC_invR	ClickFree			
Reg. 29	ZeroL	ZeroR	Mono	SE_strength			Vpp_scale	
Reg. 30			Shelving_a[29:24}					
Reg. 31	Shelving_a[23:16}							
Reg. 32	Shelving_a[15:8}							
Reg. 33	Shelving_a[7:0}							
Reg. 34			Shelving_b[29:24}					
Reg. 35	Shelving_b[23:16}							
Reg. 36	Shelving_b[15:8}							
Reg. 37	Shelving_b[7:0}							
Reg. 38			LMIXSEL			RMIXSEL		
Reg. 39	LD2LO	LI2LO	LI2LOVOL					
Reg. 40	RD2LO	RI2LO	RI2LOVOL					
Reg. 41	LD2RO	LI2RO	LI2ROVOL					
Reg. 42	RD2RO	RI2RO	RI2ROVOL					
Reg. 43	LD2MO	LI2MO	LI2MOVOL					
Reg. 44	RD2MO	RI2MO	RI2MOVOL					
Reg. 45	ROUT2INV	OUT3SW		VROI	HPSWEN	HPSWPOL	MOUTINV	
Reg. 46			LOUT1VOL					
Reg. 47			ROUT1VOL					
Reg. 48			LOUT2VOL					
Reg. 49			ROUT2VOL					
Reg. 50			MONOOUTVOL					
Reg. 51	hpLout1_ref1	hpLout1_ref2	hpRout1_ref1	hpRout1_ref2	hpOut3_ref1	hpOut3_ref2	hpMono_ref1	hpMono_ref2
Reg. 52	spkLout2_ref1	spkLout2_ref2	spkRout2_ref1	spkLout2_ref2	mixer_ref1	mixer_ref2	MREF1	MREF2

6.1 Chip Control and Power Management

6.1.1. Register0 - Chip Control 1, Default 0000 0110

Bit Name	Bit	Description
SCPReset	7	0 – Normal (Default). 1 – Reset control Port Register to Default.
LRCM	6	0 – ALRCK disabled when both ADC disabled; DLRCK disabled when both DAC disabled (default). 1 – ALRCK and DLRCK disabled when all ADC and DAC disabled.
DACMCLK	5	0 – when SameFs-1, ADCMCLK is the chip master clock source (default). 1 – when SameFs=1, DACMCLK is the chip master clock source.
SameFs	4	0 – ADC Fs differs from DAC Fs (default). 1 – ADC Fs is the same as DAC Fs.
SeqEn	3	0 – internal up/down sequence disable (default) 1 – internal up/down sequence enable.
EnRef	2	0 – disable reference. 1 – enable reference (default).
VMIDSEL	1:0	00 – VMID disabled. 01 – 50kΩ divider enabled. 10 – 500kΩ divider enabled (default). 11 – 5 kΩ divider enabled.

6.1.2. Register1 – Chip Control 2, Default 0001 1100

Bit Name	Bit	Description
TSDEN	7	0 – thermal shutdown disabled (default). 1 – thermal shutdown enabled.
PdnOC	6	0 – over current shutdown disabled (default). 1 – over current shut down enabled.
LPVcmMOD	5	0 – normal (default). 1 – low power.
LPVrefBuf	4	0 – normal. 1 – low power (default).
PdnAna	3	0 – normal. 1 – entire analog power down (default).
Pdanlbiasgen	2	0 – normal. 1 – ibiasgen power down(default).
VrefLo	1	0 – normal (default). 1 – low power.
PdnVrefbuf	0	0 – normal (default). 1 – low power.

6.1.3. Register2 – Chip Power Management, Default 1100 0011.

Bit Name	Bit	Description
adc_DigPDN	7	0 – normal. 1 – resets ADC DEM, filter and serial DATA port (default).
dac_DigPDN	6	0 – normal. 1 – resets DAC DSM, DEM, filter and serial DATA port (default).
adc_stm_rst	5	0 – normal (default). 1 – reset ADC state machine to power down state.
dac_stm_rst	4	0 – normal (default). 1 – reset DAC state machine to power down state.
ADCDLL_PDN	3	0 – normal (default). 1 – ADC_DLL power down, stop ADC clock.
DACDLL_PDN	2	0 – normal (default). 1 – DAC_DLL power down, stop DAC clock
adcVref_PDN	1	0 – ADC analog reference power up. 1 – ADC analog reference power down (default).
dacVref_PDN	0	0 – DAC analog reference power up. 1 – DAC analog reference power down (default).

6.1.4. Register3 – ADC Power Management, Default 1111 1100

Bit Name	Bit	Description
PdnAINL	7	0 – normal. 1 – left analog input power down (default).
PdnAINR	6	0 – normal. 1 – right analog input power down(default).
PdnADCL	5	0 – left ADC power up. 1 – left ADC power down (default).
PdnADCR	4	0 – right ADC power up. 1 – right ADC power down (default).
PdnMICB	3	0 – microphone bias power on. 1 – microphone bias power down (high impedance output default).
PdnADCBiasgen	2	0 – normal. 1 – power down (default)
flashLP	1	0 – normal (default) 1 – flash ADC low power.
int1LP	0	0 – normal (default) 1 – int1 low power.

6.1.5. Register4 – DAC Power Management, Default 1100 0000

Bit Name	Bit	Description
PdnDACL	7	0 – left DAC power up. 1 – left DAC power down (default).
PdnDACR	6	0 – right DAC power up. 1 – right DAC power down(default).
LOUT1	5	0 – LOUT1 disabled (default). 1 – LOUT1 enabled.
ROUT1	4	0 – ROUT1 disabled (default). 1 – ROUT1 enabled.
LOUT2	3	0 – LOUT2 disabled (default). 1 – LOUT2 enabled.
ROUT2	2	0 – ROUT2 disabled (default). 1 – ROUT2 enabled.
MONO	1	0 – MOUT disabled (default). 1 – MOUT enabled.
OUT3	0	0 – OUT3 disabled (default). 1 – OUT3 enabled.

6.1.6. Register5 – Chip Low Power 1, Default 0000 0000

Bit Name	Bit	Description
LPDACL	7	0 – normal (default). 1 – low power.
LPDACR	6	0 – normal (default). 1 – low power.
LPLOUT1	5	0 – normal (default). 1 – low power.
LPROUT1	4	0 – normal (default). 1 – low power.
LPLOUT2	3	0 – normal (default). 1 – low power.
LPROUT2	2	0 – normal (default). 1 – low power.
LPMONO	1	0 – normal (default). 1 – low power.
LPOUT3	0	0 – normal (default). 1 – low power.

6.1.7. Register6 – Chip Low Power 2, Default 0000 0000

Bit Name	Bit	Description
LPPGA	7	0 – normal (default). 1 – low power.
LPLMIX	6	0 – normal (default). 1 – low power.
LPRMIX	5	0 – normal (default). 1 – low power.
LPMMIX	4	0 – normal (default). 1 – low power.
LPMOUTINV	3	0 – normal (default). 1 – low power.
LPOUT2INV	2	0 – normal (default). 1 – low power.
LPADCvrp	1	0 – normal (default). 1 – low power.
LPDACvrp	0	0 – normal (default). 1 – low power.

6.1.8. Register7 – Analog Voltage Management, Default 0111 1100

Bit Name	Bit	Description
VSEL	6:0	1111100 – normal (default).

6.1.9. Register8 – Master Mode Control, Default 1000 0000

Bit Name	Bit	Description
MSC	7	0 – slave serial port. 1 – master serial port (default).
MCLKDIV2	6	0 – MCLK not divided (default). 1 – MCLK divide by 2.
BCLK_INV	5	0 – normal (default). 1 – BCLK inverted.
BCLKDIV	4:0	00000 – master mode BCLK generated automatically based on clock table (default). others – MCLK/N, N=1~31.

6.2. ADC Control

6.2.1. Register9 – ADC Control 1, Default 0000 0000

Bit Name	Bit	Description
MicAmpL	7:4	Left Channel PGA gain. 0000 – 0dB (default). 0001 - +3dB 0010 - +6dB 0011 - +9dB 0100 - +12dB 0101 - +15dB 0110 - +18dB 0111 - +21dB 1000 - +24dB
MicAmpR	3:0	Right Channel PGA gain. 0000 – 0dB (default). 0001 - +3dB 0010 - +6dB 0011 - +9dB 0100 - +12dB 0101 - +15dB 0110 - +18dB 0111 - +21dB 1000 - +24dB

6.2.2. Register10 – ADC Control 2, Default 0000 0000

Bit Name	Bit	Description
LINSEL	7:6	Left channel input select. 00 – LINPUT1 (default). 01 – LINPUT2 10 – LINPUT3 11 – L-R differential (either LINPUT1 – RINPUT1 or LINPUT2 – RINPUT2, selected by DS)
RINSEL	5:4	Right channel input select. 00 – RINPUT1 (default). 01 – RINPUT2 10 – RINPUT3 11 – L-R differential (either LINPUT1 – RINPUT1 or LINPUT2 – RINPUT2, selected by DS)

6.2.3. Register11 – ADC Control 3, Default 0000 0110

Bit Name	Bit	Description
DS	7	Differential Input Select 0 – LINPUT1 – RINPUT1 (default). 1 – LINPUT2 – RINPUT2.
LDCM	6	0 – normal (default) 1 – Left Channel used for DC Measuement
RDCM	5	0 – normal (default) 1 – Right Channel used for DC Measuement
MONOMIX	4:3	00 – stereo (default). 01 – analog mono mix to left ADC. 10 – analog mono mix to right ADC. 11 - reserved
TRI	2	0 – ASDOUT is ADC normal output (default). 1 – ASDOUT tri-stated, ALRCK, DLRCK and SCLK are inputs.
OC	1:0	00 – normal over current setting (default)

6.2.4. Register12 – ADC Control 4, Default 0000 0000

Bit Name	Bit	Description
DATSEL	7:6	00 - left DATA = left ADC, right DATA = right ADC 01 - left DATA = left ADC, right DATA = left ADC 10 - left DATA = right ADC, right DATA = right ADC 11 - left DATA = right ADC, right DATA = left ADC
ADCLRP	5	I2S, left justified or right justified mode: 0 – left and right normal polarity. 1 – left and right inverted polarity. DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after ALRCK rising edge 1 – MSB is available on 1st BCLK rising edge after ALRCK rising edge
ADCWL	4:2	000 – 24-bit serial audio DATA word length. 001 – 20-bit serial audio DATA word length 010 – 18-bit serial audio DATA word length 011 – 16-bit serial audio DATA word length 100 – 32-bit serial audio DATA word length
ADCFORMAT	1:0	00 – I2C serial audio DATA format 01 – left justify serial audio DATA format 10 – right justify serial audio DATA format 11 – DSP/PCM mode serial audio DATA format.

6.2.5. Register13 – ADC Control 5, Default 0000 0110

Bit Name	Bit	Description
ADC_FsMode	5	0 – single speed mode (default) 1 – double speed mode.
ADC_FsRatio	4:0	Master mode ADC MCLK to sampling frequency ratio: 00000 -128 00001 – 192 00010 – 256 00011 – 384 00100 – 512 00101 – 576 00110 – 768 (default) 00111 – 1024 01000 – 1152 01001 – 1408 01010 – 1536 01011 – 2112 01100 – 2304 Other – Reserved. 10000 - 125 10001 - 136 10010 - 250 10011 - 272 10100 - 375 10101 - 500 10110 - 544 10111 - 750 11000 - 1000 11001 - 1088 11010 - 1496 11011 - 1500

6.2.6. Register14 – ADC Control 6, Default 0011 0000

Bit Name	Bit	Description
ADC_invL	7	0 – normal (default). 1 – left channel polarity inverted.
ADC_invR	6	0 – normal (default). 1 – right channel polarity inverted.
ADC_HP_L	5	0 – disable ADC left channel high pass filter. 1 – enable ADC left channel high pass filter (default).
ADC_HP_R	4	0 – disable ADC right channel high pass filter. 1 – enable ADC right channel high pass filter (default).

6.2.7. Register15 – ADC Control 7, Default 0011 0000

Bit Name	Bit	Description
ADCRampRate	7:6	00 – 0.5dB per 4 LRCK digital volume control ramp rate (default). 01 – 0.5dB per 8 LRCK digital volume control ramp rate. 10 – 0.5dB per 16 LRCK digital volume control ramp rate. 11 – 0.5dB per 32 LRCK digital volume control ramp rate.
ADCSoftRamp	5	0 – disable digital volume control soft ramp. 1 – enable digital volume control soft ramp (default)
ADCZeroCrs	4	0 – disable digital volume control at zero crossing. 1 – enable digital volume control at zero crossing (default).
ADCLeR	3	0 – normal (default) 1 – both channel gain control is set by ADC left gain control register
ADCMute	2	0 – normal (default). 1 – mute ADC digital output.

6.2.8. Register16 – ADC Control 8, Default 1100 0000

Bit Name	Bit	Description
LADCVOL	7:0	Digital volume control attenuates the signal in 0.5dB increments from 0 to -96dB 00000000 – 0dB. 00000001 – -0.5dB 00000010 - -1dB …… 11000000 - -96dB (default).

6.2.9. Register17 – ADC Control 9, Default 1100 0000

Bit Name	Bit	Description
RADCVOL	7:0	Digital volume control attenuates the signal in 0.5dB increments from 0 to -96dB 00000000 – 0dB. 00000001 – -0.5dB 00000010 - -1dB …… 11000000 - -96dB (default).

6.2.10. Register18 – ADC Control 10, Default 0011 1000

Bit Name	Bit	Description
ALSEL	7:6	00 – ALC off 01 – ALC right channel only 10 – ALC left channel only 11 – ALC stereo
MAXGAIN	5:3	Set maximum gain of PGA 000 - -6.5dB 001 - -0.5dB 010 – 5.5dB 011 – 11.5dB 100 – 17.5dB 101 – 23.5dB 110 – 29.5dB 111 – 35.5dB
MINGAIN	2:0	Set minimum gain of PGA 000 - -12dB 001 - -6dB 010 – 0dB 011 – +6dB 100 – +12dB 101 – +18dB 110 – +24dB 111 – +30dB

6.2.11. Register19 – ADC Control 11, Default 1011 0000

Bit Name	Bit	Description
ALCLVL	7:4	ALC target 0000 - -25dBFS 0001 - -21.0bDFS ……. 1100 - -4.5dBFS 1101 - -3dBFS 1110 - -1.5dBFS 1111 - -1.5dBFS
ALCHLD	3:0	AFC hold time before gain is increased 0000 – 0mS 0001 – 2.67mS 0010 – 5.33mS ……time doubles with every step 1001 – 0.68S 1010 or higher – 1.36S

6.2.12. Register20 – ADC Control 12, Default 0011 0010

Bit Name	Bit	Description
ALCDCY	7:4	ALC decay (gain ramp up) time, ALC mode/limiter mode: 0000 – 410 µS/90.8 µS 0001 – 820 µS/182 µS 0010 – 1.64 mS/363 µS ……. time doubles with every step. 1001 – 210 mS/182 µS 1010 or higher – 420 mS
ALCATK	3:0	ALC attack (gain ramp down) time, ALC mode/limiter mode: 0000 – 104 µS/22 µS 0001 – 208 µS/45.4 µS 0010 – 416 µS/90 µS ……time doubles with every step 1001 – 53.2 mS/11.6 mS 1010 or higher – 106 mS/23.2 mS

6.2.13. Register21 – ADC Control 13, Default 0000 0110

Bit Name	Bit	Description
ALCMODE	7	Determines the ALC mode of operation: 0 – ALC mode (normal operation) 1 – limiter mode
ALCZC	6	ALC uses zero cross detection circuit. 0 – disable (recommended). 1 - enable
TIME_OUT	5	Zero Cross time out: 0 – disable (default) 1 – enable.
WIN_SIZE	4:0	window size for peak detector, ste the window size to N*16 samples: 00110 – 96 samples (default) 00111 – 102 samples …… 11111 – 496 samples

6.2.14. Register22 – ADC Control 14, Default 0000 0000

Bit Name	Bit	Description
NGTH	7:3	Noise gate threshold: 00000 – -76.5dBFS. 00001 - -75dBFS. …… 11110 - -31.5dBFS. 11111 - -30dBFS.
NGG	2:1	Noise gate type. x0 – PGA gain held constant. 01 – mute ADC output. 11 – reserved.
NGAT	0	Zero Cross time out: 0 – disable (default) 1 – enable.

6.3 DAC Control

6.3.1. Register23 – DAC Control 1, Default 0000 0000

Bit Name	Bit	Description
DACLRSWAP	7	0 – normal. 1 – left and right channel DATA swap.
DACLRP	6	I^2S, left justified or right justified mode. 0 – left and right normal polarity. 1 – left and right inverted polarity. DSP/PCM mode. 0 – MSB is available on 2nd BCLK rising edge after ALRCL rising edge. 1 – MSB is available on 1st BCLK rising edge after ALRCK rising edge LRCK polarity.
DACWL	5:3	000 – 24-bit serial audio DATA word length. 001 – 20-bit serial audio DATA word length. 010 – 18-bit serial audio DATA word length. 011 – 16-bit serial audio DATA word length. 100 – 32-bit serial audio DATA word length.
DACFORMAT	2.1	00 – I^2S serial audio DATA format. 01 – left justify serial audio DATA format. 10 – right justify serial audio DATA format. 11 – DSP/PCM mode serial audio DATA format.

6.3.2. Register24 – DAC Control 2, Default 0000 0110

Bit Name	Bit	Description
DAC_FsMode	5	0 – single speed mode (default) 1 – double speed mode.
DACFsRatio	4:0	Master mode ADC MCLK to sampling frequency ratio: 00000 -128 00001 – 192 00010 – 256 00011 – 384 00100 – 512 00101 – 576 00110 – 768 (default) 00111 – 1024 01000 – 1152 01001 – 1408 01010 – 1536 01011 – 2112 01100 – 2304 Other – Reserved. 10000 - 125 10001 - 136 10010 - 250 10011 - 272 10100 - 375 10101 - 500 10110 - 544 10111 - 750 11000 - 1000 11001 - 1088 11010 - 1496 11011 - 1500

6.3.3. Register25 – DAC Control 3, Default 0011 0000

Bit Name	Bit	Description
DACRampRate	7:6	00 – 0.5dB per 4 LRCK digital volume control ramp rate (default). 01 – 0.5dB per 8 LRCK digital volume control ramp rate. 10 – 0.5dB per 16 LRCK digital volume control ramp rate. 11 – 0.5dB per 32 LRCK digital volume control ramp rate.
DACSoftRamp	5	0 – disable digital volume control soft ramp. 1 – enable digital volume control soft ramp (default)
DACZeroCrs	4	0 – disable digital volume control at zero crossing. 1 – enable digital volume control at zero crossing (default).
DACLeR	3	0 – normal (default) 1 – both channel gain control is set by DAC left gain control register
DACMute	2	0 – normal (default). 1 – mute analog outputs for both channels.
AutoMute	1	0 – disable. 1 – enable (default).

6.3.4. Register26 – DAC Control 4, Default 1100 0000

Bit Name	Bit	Description
LDACVOL	7:0	Digital volume control attenuates the signal in 0.5dB increments from 0 to -96dB 00000000 – 0dB. 00000001 – -0.5dB 00000010 - -1dB …… 11000000 - -96dB (default).

6.3.5. Register27 – DAC Control 5, Default 1100 0000

Bit Name	Bit	Description
RDACVOL	7:0	Digital volume control attenuates the signal in 0.5dB increments from 0 to -96dB 00000000 – 0dB. 00000001 – -0.5dB 00000010 - -1dB …… 11000000 - -96dB (default).

6.3.6. Register28 – DAC Control 6, Default 0000 1000

Bit Name	Bit	Description
DeemphasisMode (DEEMP)	7:6	00 – de-emphasis frequency disabled (default) 01 – 32 kHz de-emphasis frequency in single speed mode. 10 – 44 kHz de-emphasis frequency in single speed mode. 11 – 48 kHz de-emphasis frequency in single speed mode.
DAC_invL	5	0 – normal DAC left channel output no phase inversion (default) 1 – normal DAC left channel output 180° phase inversion.
DAC_invR	4	0 – normal DAC right channel output no phase inversion (default) 1 – normal DAC right channel output 180° phase inversion.
ClickFree	3	0 – disable digital click free power up and down. 1 – enable digital click free power up and down (default).

6.3.7. Register29 – DAC Control 7, Default 0000 0110

Bit Name	Bit	Description
ZeroL	7	0 – normal (default) 1 – set Left Channel DAC output all zero.
ZeroR	6	0 – normal (default) 1 – set Right Channel DAC output all zero.
Mono	5	0 – normal (default) 1 – mono (L+RE)/2 into DACL and DACR.
SE_Strength	4:2	SE Strength, total 8 settings, L=L+(L-R)*a, R=R+(R-L)*a, where a is from 0 to 7/8 000 – 0 (default) ……. 111 – 7/8
Vpp_scale	1:0	00 – Vpp set at 3.5V (0.7 modulation index) (default). 01 – Vpp set at 4.0V 10 – Vpp set at 3.0V 11 – Vpp set at 2.5V

6.3.8. Register30 – DAC Control 8, Default 0001 1111

Bit Name	Bit	Description
Shelving_a[29:24]	5:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}.

6.3.9. Register31 – DAC Control 9, Default 1111 0111

Bit Name	Bit	Description
Shelving_a[23:16]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}.

6.3.10. Register32 – DAC Control 10, Default 1111 0111

Bit Name	Bit	Description
Shelving_a[15:8]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}.

6.3.11. Register33 – DAC Control 11, Default 1111 1111

Bit Name	Bit	Description
Shelving_a[7:0]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}.

6.3.12. Register34 – DAC Control 12, Default 0001 1111

Bit Name	Bit	Description
Shelving_b[29:24]	5:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}.

6.3.13. Register35 – DAC Control 13, Default 1111 0111

Bit Name	Bit	Description
Shelving_b[23:16]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}.

6.3.14. Register36 – DAC Control 14, Default 1111 1101

Bit Name	Bit	Description
Shelving_b[15:8]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}.

6.3.15. Register37 – DAC Control 15, Default 1111 1111

Bit Name	Bit	Description
Shelving_b[7:0]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}.

6.3.16. Register38 – DAC Control 16, Default 0000 0000

Bit Name	Bit	Description
LMIXSEL	5:3	Left input select for output mix. 00 – LIN1 (default). 01 – LIN2 10 – LIN3 11 – left ADC input (after microphone amplifier)
RMIXSEL	2:0	Right input select for output mix. 00 – RIN1 (default). 01 – RIN2 10 – RIN3 11 – right ADC input (after microphone amplifier)

6.3.17. Register39 – DAC Control 17, Default 0011 1000

Bit Name	Bit	Description
LD2LO	7	0 – left DAC to left mixer disable (default). 1 – left DAC to left mixer enable
LI2LO	6	0 – LIN signal to left mixer disable (default). 1 – LIN signal to left mixer enable
LI2LOVOL	5:3	LIN signal to left mixer gain. 000 – 6dB. 001 – 3dB. 010 – 0dB. 011 – -3dB. 100 – -6dB. 101 – -9dB. 110 – -12dB. 111 – -15dB (default).

6.3.18. Register40 – DAC Control 18, Default 0011 1000

Bit Name	Bit	Description
RD2LO	7	0 – right DAC to left mixer disable (default). 1 – right DAC to left mixer enable
RI2LO	6	0 – RIN signal to left mixer disable (default). 1 – RIN signal to left mixer enable
RI2LOVOL	5:3	RIN signal to left mixer gain. 000 – 6dB. 001 – 3dB. 010 – 0dB. 011 – -3dB. 100 – -6dB. 101 – -9dB. 110 – -12dB. 111 – -15dB (default).

6.3.19. Register41 – DAC Control 19, Default 0011 1000

Bit Name	Bit	Description
LD2RO	7	0 – left DAC to right mixer disable (default). 1 – left DAC to right mixer enable
LI2RO	6	0 – LIN signal to right mixer disable (default). 1 – LIN signal to right mixer enable
LI2ROVOL	5:3	LIN signal to right mixer gain. 000 – 6dB. 001 – 3dB. 010 – 0dB. 011 – -3dB. 100 – -6dB. 101 – -9dB. 110 – -12dB. 111 – -15dB (default).

6.3.20. Register42 – DAC Control 20, Default 0011 1000

Bit Name	Bit	Description
RD2RO	7	0 – right DAC to right mixer disable (default). 1 – right DAC to right mixer enable
RI2RO	6	0 – RIN signal to right mixer disable (default). 1 – RIN signal to right mixer enable
RI2ROVOL	5:3	RIN signal to right mixer gain. 000 – 6dB. 001 – 3dB. 010 – 0dB. 011 – -3dB. 100 – -6dB. 101 – -9dB. 110 – -12dB. 111 – -15dB (default).

6.3.21. Register43 – DAC Control 21, Default 0011 1000

Bit Name	Bit	Description
LD2MO	7	0 – left DAC to mono mixer disable (default). 1 – left DAC to mono mixer enable
LI2MO	6	0 – LIN signal to mono mixer disable (default). 1 – LIN signal to mono mixer enable
LI2MOVOL	5:3	LIN signal to mono mixer gain. 000 – 6dB. 001 – 3dB. 010 – 0dB. 011 – -3dB. 100 – -6dB. 101 – -9dB. 110 – -12dB. 111 – -15dB (default).

6.3.22. Register44 – DAC Control 22, Default 0011 1000

Bit Name	Bit	Description
RD2MO	7	0 – right DAC to right mixer disable (default). 1 – right DAC to right mixer enable
RI2MO	6	0 – RIN signal to right mixer disable (default). 1 – RIN signal to right mixer enable
RI2MOVOL	5:3	RIN signal to mono mixer gain. 000 – 6dB. 001 – 3dB. 010 – 0dB. 011 – -3dB. 100 – -6dB. 101 – -9dB. 110 – -12dB. 111 – -15dB (default).

6.3.23. Register45 – DAC Control 23, Default 0000 0000

Bit Name	Bit	Description
ROUT2INV	7	0 – ROUT2 no inversion (default). 1 – ROUT2 signal inverted
OUT3SW	6:5	OUT3 select 00 – VREF (default). 01 – ROUT1 signal (volume controlled by ROUT1VOL) 10 – MONOOUT 11 – right mixer output (no volume controlled by ROUT1VOL)
VROI	4	0 – 1.5k VREF to analog output resistance (default) 1 – 40k VREF to analog output resistance
HPSWEN	3	0 – headphone switch disabled (default) 1 – headphone switch enabled
HPSWPOL	2	0 – HPDETECT high = headphone (default) 1 – HPDETECT high = speaker
MOUTINV	1	0 – MOUT no inversion (default). 1- MOUT signal inverted

6.3.24. Register46 – DAC Control 24, Default 0000 0000

Bit Name	Bit	Description
LOUT1VOL	5:0	LOUT1 volume 000000 - -30dB (default). 000001 - -29dB 000010 - -28dB …….. 011110 – 0dB 011111 – 1dB ……. 100100 – 6dB

6.3.25. Register47 – DAC Control 25, Default 0000 0000

Bit Name	Bit	Description
ROUT1VOL	5:0	ROUT1 volume 000000 - -30dB (default). 000001 - -29dB 000010 - -28dB …….. 011110 – 0dB 011111 – 1dB ……. 100100 – 6dB

6.3.26. Register48 – DAC Control 26, Default 0000 0000

Bit Name	Bit	Description
LOUT2VOL	5:0	LOUT2 volume 000000 - -30dB (default). 000001 - -29dB 000010 - -28dB …….. 011110 – 0dB 011111 – 1dB ……. 100100 – 6dB

6.3.27. Register49 – DAC Control 27, Default 0000 0000

Bit Name	Bit	Description
ROUT2VOL	5:0	ROUT2 volume 000000 - -30dB (default). 000001 - -29dB 000010 - -28dB …….. 011110 – 0dB 011111 – 1dB ……. 100100 – 6dB

6.3.28. Register50 – DAC Control 28, Default 0000 0000

Bit Name	Bit	Description
MONOOUTVOL	5:0	MONOOUT volume 000000 - -30dB (default). 000001 - -29dB 000010 - -28dB …….. 011110 – 0dB 011111 – 1dB ……. 100100 – 6dB

6.3.29. Register51 – DAC Control 29, Default 0000 0000

Bit Name	Bit	Description
hpLout_ref1	7	Reserved
hpLout_ref2	6	Reserved
hpRout_ref1	5	Reserved
hpRout_ref2	4	Reserved
hpOut3_ref1	3	Reserved
hpOut3_ref2	2	Reserved
hpMono_ref1	1	Reserved
hpMono_ref2	0	Reserved

6.3.30. Register52 – DAC Control 30, Default 0000 0000

Bit Name	Bit	Description
spkLout_ref1	7	Reserved
spkLout_ref2	6	Reserved
spkRout_ref1	5	Reserved
spkRout_ref2	4	Reserved
spkOut3_ref1	3	Reserved
spkOut3_ref2	2	Reserved
spkMono_ref1	1	Reserved
spkMono_ref2	0	Reserved

7. Digital Audio Interface.

The PA5750 provides four formats of serial DATA interface to the input of the DAC through LRCK, SCLK and SDIN/SDOUT pins.
They are I^2S, left justified, right justified and DSP/PCM mode. DAC input DSDIN is sampled by PA5750 on the rising edge of DSCLK. ADC DATA is moved out on ASDOUT and changes on the falling edge od ASCLK. The relation of SDATA (SDIN/SDOUT), SCLK and LRCK with the three formats is shown in Fig. 3 through Fig. 7.

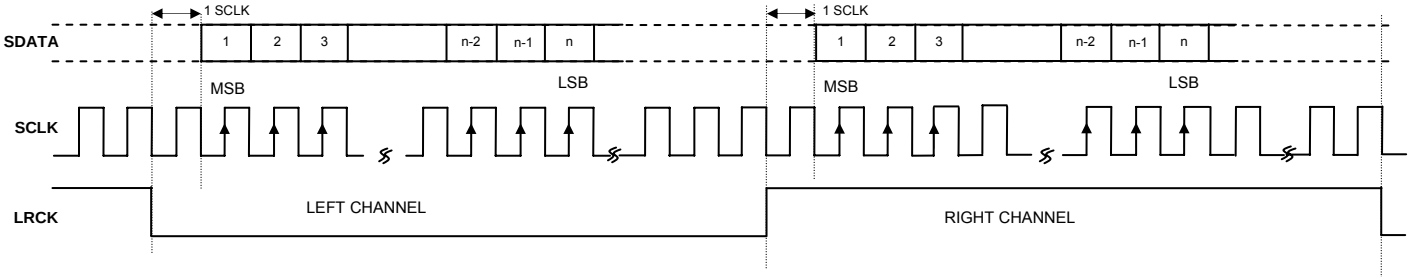


Fig. 3 I2S Serial Audio DATA Format up to 24-bit

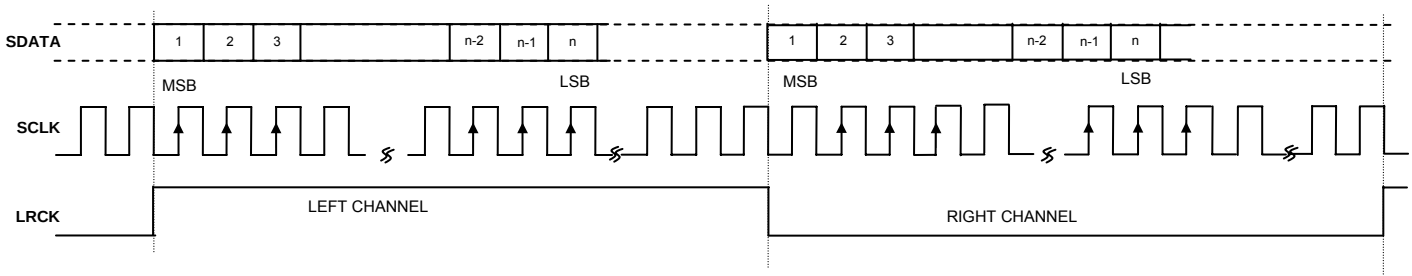


Fig. 4 Left Justified Serial Audio DATA Format up to 24-bit

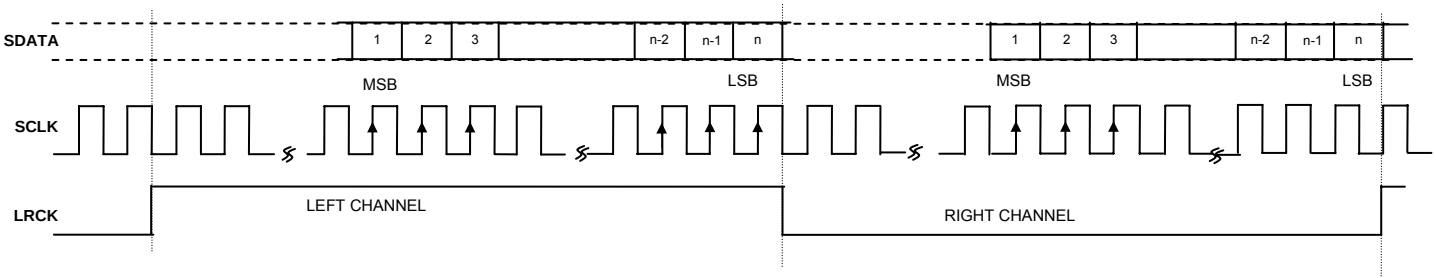


Fig. 5 Right Justified Serial Audio DATA Format up to 24-bit

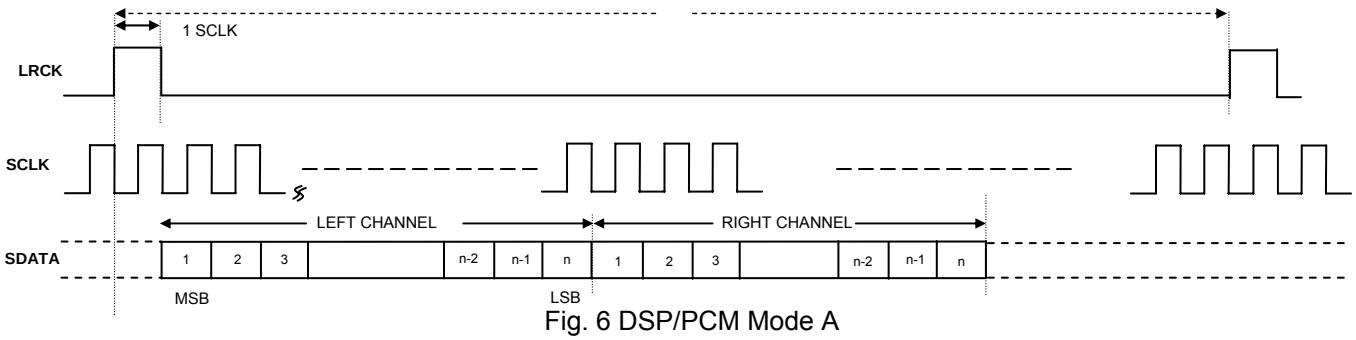


Fig. 6 DSP/PCM Mode A

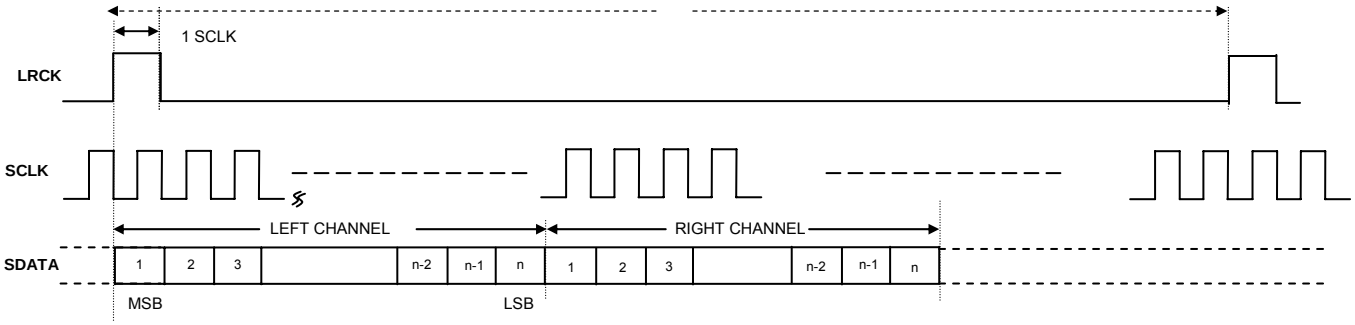


Fig. 7 DSP/PCM Mode B

8. ELECTRCAL CHARACTERISTICS.

8.1. Absolute Maximum Ratings

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MINIMUM	MAXIMUM
Analog Supply Voltage	-0.3V	+5.0V
Digital Supply Voltage	-0.3V	+5.0V
Input Voltage Range	D_{GND} – 0.3V	D_{VDD} + 0.3V
Operating Temperature Range	-40°C	+80°C
Storage Temperature Range	-65°C	+150°C

8.2 Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNIT
Analog Supply Voltage	1.7	3.3	3.6	V
Digital Supply Voltage	1.5	1.8	3.6	V

8.3. ADC Analog and Filter Characteristics and Specifications

Test Conditions are as follows unless otherwise specified.
AV_{DD} = +3.3V, DV_{DD} = +1.8V, A_{GND} = 0V, D_{GND} = 0V, Ambient 25°C, Fs = 48, 96 or 192 kHz, MCLK/LRCK = 256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Dynamic Range *(note 1)*	82	92	95	dB
THD+N	-88	-85	-75	dB
Channel Separation (1 kHz)	80	85	90	dB
Signal to Noise Ration	82	92	95	dB
Interchannel Gain Mismatch		01		dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	50			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	50			dB
Analog Input				
Full Scale Input Level		AV_{DD}/3.3		V_{RMS}
Input Impedance		20		KΩ

Note.1; Measured using A-weighted filter.

8.4. DAC Analog and Filter Characteristics and Specifications

Test Conditions are as follows unless otherwise specified.
AV_{DD} = +3.3V, DV_{DD} = +1.8V, A_{GND} = 0V, D_{GND} = 0V, Ambient 25°C, Fs = 48, 96 or 192 kHz, MCLK/LRCK = 256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Dynamic Range *(note 1)*	83	93	98	dB
THD+N	-85	-81	-75	dB
Channel Separation (1 kHz)	80	85	90	dB
Signal to Noise Ration	83	93	98	dB
Interchannel Gain Mismatch		0.05		dB
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	40			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	40			dB
De-emphasis Error at 1 kHz (Single Speed Mode Only)				
Fs = 32 kHz Fs = 44.1 kHz Fs = 4832 kHz			0.002 0.013 0.0009	dB
Analog Output				
Full Scale Output Level		AV_{DD}/3.3		V_{RMS}

Note.1; Measured using A-weighted filter.

8.5. Power Consumption Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD = 1.8V, AVDD = 1.8V Play Back Play Back and Record DVDD = 3.3V, AVDD = 3.3V Play Back Play Back and Record		 7 16 31 59		mW
Power Down Mode				
DVDD = 1.8V, AVDD = 1.8V DVDD = 3.3V, AVDD = 3.3V		0.3 1.9		mW

8.6 Serial Audio Port Switching Specifications

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	kHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SCLKL}	15		nS
SCLK pulse width high	T_{SCLKH}	15		nS
SCLK falling to LRCK edge	T_{SLR}	-10	10	nS
SCLK falling to SDOUT valid	T_{SDO}	0		nS
SDIN valid to SCLK rising setup time	T_{SDIS}	10		nS
SCLK rising to SDIN hold time	T_{SDIH}	10		nS

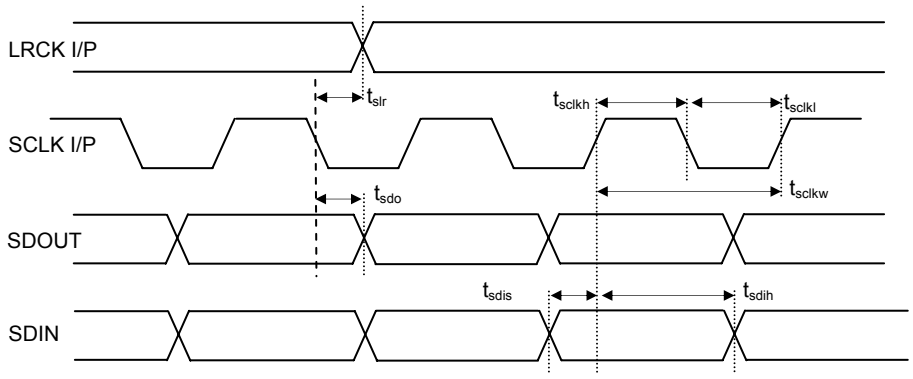


Fig. 8 Serial Audio Port Timing

8.7. Serial Control Port Switching Specifications

PARAMETER	Symbol	MIN	MAX	UNIT
SPI Mode				
SPI_CLK frequency			10	MHz
SPI_CLK edge to SPI_CSn falling	T_{SPICS}	5		nS
SPI_CSn High time between transmissions	T_{SPISH}	500		nS
SPI_CSn trailing to SPI_CLK edge	T_{SPISC}	10		nS
SPI_CLK low time	T_{SPICL}	45		nS
SPI_CLK high time	T_{SPICH}	45		nS
SPI_DIN to SPI_CLK rise setup time	T_{SPIDS}	10		nS
SPI_CLK rise to DATA hold time	T_{SPIDH}	15		nS
2-Wire Mode				
SCL clock frequency	F_{SCL}		100	kHz
BUS free time between transmissions	T_{TWID}	4.7		µS
Start condition hold time	T_{TWSSTH}	4.0		µS
Clock low time	T_{TWCL}	4.0		µS
Clock high time	T_{TWCH}	4.0		µS
Setup time for repeated start condition	T_{TWSTS}	4.7		µS
SDA hold time from SCL falling	T_{TWDH}	0.1		µS
SDA setup time to SCL rising	T_{TWDS}	100		nS
Rise time of SCL	T_{TWR}		25	µS
Fall time of SCL	T_{TWF}		25	µS

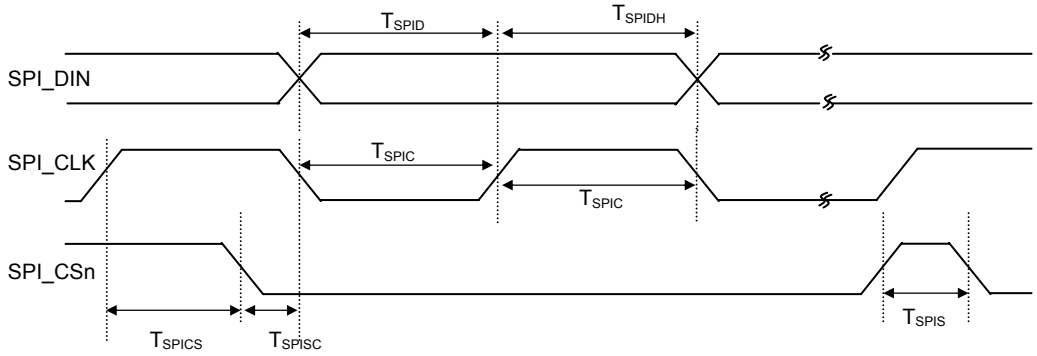


Fig.9 Serial Control Port SPI Timing

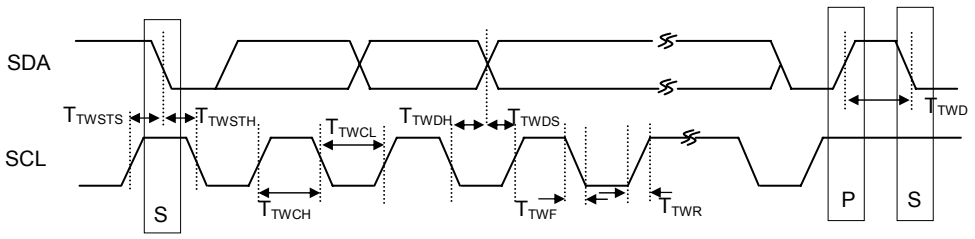
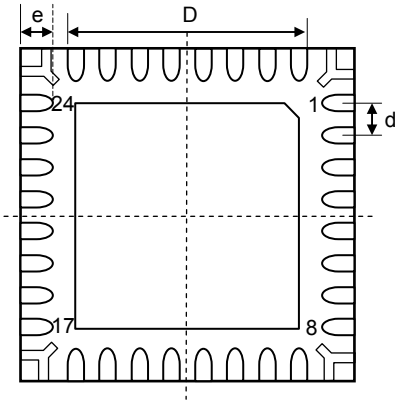


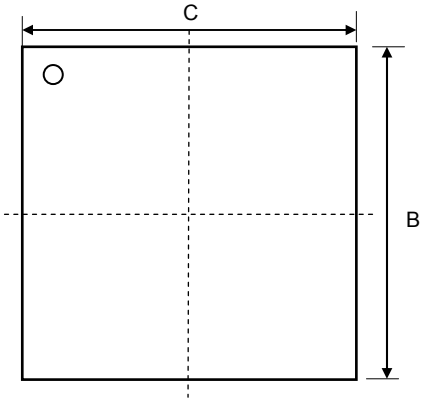
Fig.10 Serial Control Port 2-wire Timing

9. PACKAGE INFORMATION

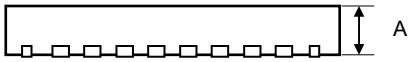
32-Pin QFN Plastic Package 5x5x0.9mm Body, 0.5mm Lead Pitch



Bottom View



Top View



Side View

Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	0.85	0.90	1.00
B	4.90	5.00	5.10
C	4.90	5.00	5.10
D	3.2	3.3	3.4
e	0.35	0.4	0.45
d	0.50BSC		

Tape and Reel Specifications

Reel Dia	A0	B0	K0	D	E	F	W	P0	P2	P	t-max
178 (7")	5.10±0.05	5.10±0.05	1.00±0.05	1.50±0.10	1.75±0.10	5.50±0.05	12.00±0.30	4.00±0.10	2.00±0.05	8.00±0.10	0.30