

FEATURES

- 95 dB dynamic range
- -85 dB THD+N
- Up to 200 kHz sampling frequency
- I²S audio data format, 16-24 bits
- Single power supply 3.0V to 5.5V

APPLICATIONS

- DVD players
- Portable audio players
- Set top boxes
- Digital TVs

GENERAL DESCRIPTION

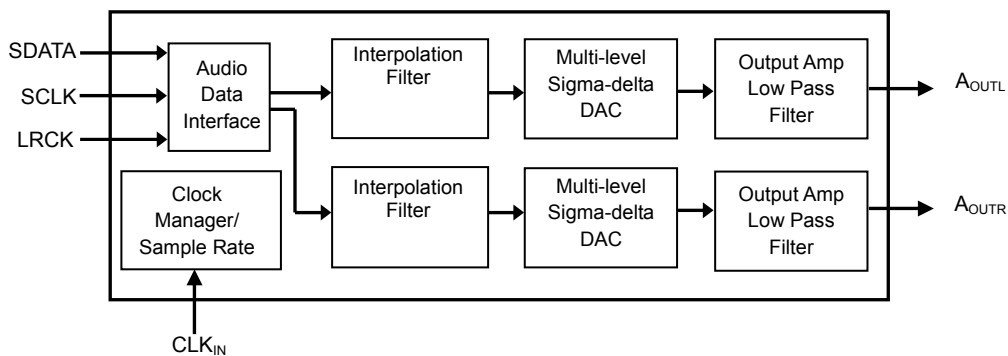
The PA5134LV is a low cost 8-pin stereo digital to analog converter.

The PA5134LV can accept I²S serial audio data format up to 24-bit word length.

The device uses advanced multi-bit Δ - Σ modulation technique to convert data into two channel analog outputs.

The multi-bit Δ - Σ modulator makes the device with very low sensitivity to clock jitter and very low out of band noise.

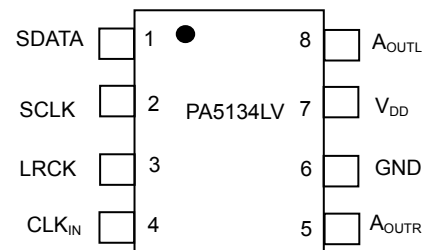
BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN	VALUE	DESCRIPTION
1	SDATA	Serial audio data input
2	SCLK	Bit clock input
3	LRCK	Left and right channel clock input indicating input data sampling rate (Fs) and channel selection
4	CLK _{IN}	System clock input
5	A _{OUTR}	Analog output of right channel
6	GND	Ground
7	VDD	Device power supply
8	A _{OUTL}	Analog output of left channel

PIN CONFIGURATION



ORDERING INFORMATION

Temperature Range	Package	Part Number
-40 to 85 °C	SO8-IC	PA5134LV-T7

ABSOLUTE MAXIMUM RATINGS

 Supply Voltage MIN-0.3V MAX +7.0V
 Input Voltage MIN GND-0.3V MAX $V_{DD}+0.3V$
 Operating Temperature.....MIN -40°C MAX +85°C
 Storage Temperature.....MIN -65°C MAX +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage MIN 3.0 MAX 5.5V

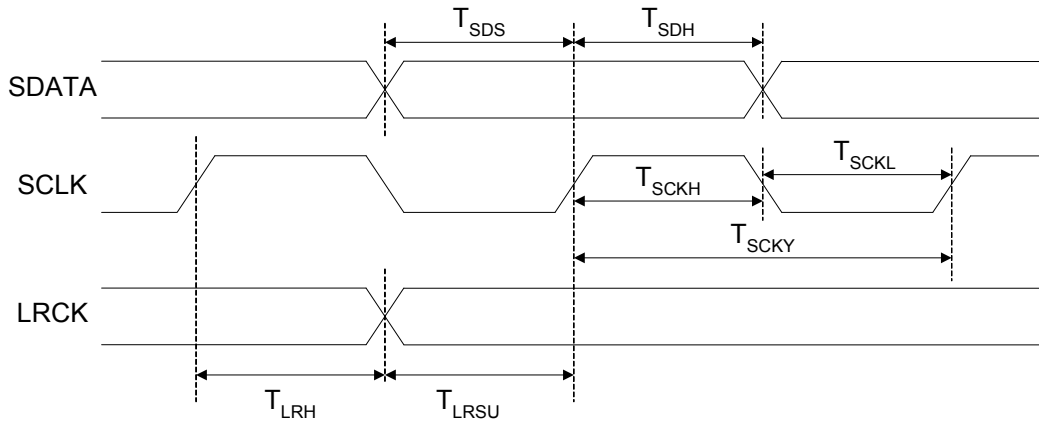
ANALOG CHARACTERISTICS
Test conditions: VDD=5.0V, GND=0V, ambient temperature=25°C, Fs=48KHz, CLKIN/LRCK=256, input 0dB 1KHz sinewave

PARAMETERS	MINIMUM	TYPICAL	MAXIMUM	UNIT
DAC Performance				
Dynamic Range (<i>Note 1</i>)	90	95		dB
THD+N		-85	-80	dB
Channel Separation (1KHz)		100		dB
Signal to Noise Ratio		95		dB
Interchannel Gain Mismatch		0		dB
Frequency Response (20Hz-20KHz)	-0.02		+0.08	dB
Filter Frequency Response Characteristics				
Single Speed				
Passband	0		0.454	Fs
Stopband	0.547			Fs
Passband Ripple		±0.05		dB
Stopband Attenuation	-53			dB
Double Speed				
Passband	0		0.417	Fs
Stopband	0.583			Fs
Passband Ripple		±0.005		dB
Stopband Attenuation	-56			dB
Quad Speed				
Passband	0		0.2083	Fs
Stopband	0.792			Fs
Passband Ripple		±0.006		dB
Stopband Attenuation	-50			dB
Analog Output Characteristics				
Full Scale Output Level	3.25	3.5	3.75	Vpp
Output Impedance		120		Ω
Minimum Load Resistance		2		KΩ
Maximum Capacitance		100		pF

Note 1. A-weighted filter is used in measurement.


SERIAL AUDIO PORT SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
CLKIN Frequency			51.2	MHz
CLKIN Duty Cycle		40	60	%
LRCK Frequency			200	KHz
LRCK Duty Cycle		40	60	%
SCLK Frequency			26	MHz
SCLK Pulse Width Low	T_{SCKL}	15		ns
SCLK Pulse Width High	T_{SCKH}	15		ns
SCLK Rising to LRCK Edge Delay	T_{LRH}	10		ns
SCLK Rising to LRCK Edge Setup Time	T_{RSU}	10		ns
SDATA Valid to SCLK Rising Setup Time	T_{SDS}	10		ns
SCLK Rising to SDATA Hold Time	T_{SDH}	10		ns



Serial Audio Port Timing Diagram

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
VDD Current $V_{DD}=3.3V$		15.0	20.0	mA
Power Dissipation $V_{DD}=3.3V$		50.0	70.0	mW
Digital Voltage Level				
Input High-level Voltage	2.0			V
Input Low-level Voltage			0.8	V
Output High-level Voltage		V_{DD}		V
Output Low-level Voltage		0		V



RECOMMENDED APPLICATION CIRCUIT

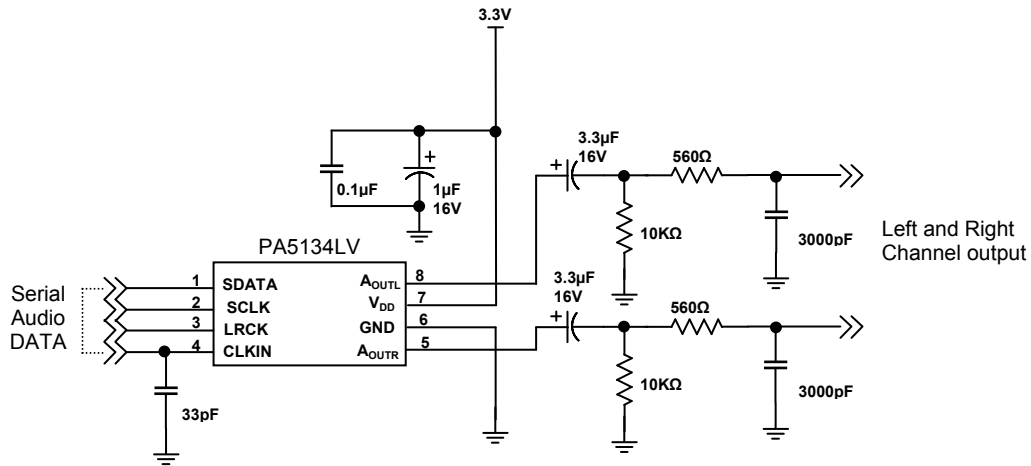


Figure 1 Recommended Application Circuit.

APPLICATION DESCRIPTIONS

Sampling Rate and Input Clocks

The serial audio input data is transmitted to the device at SDATA pin. According to the sampling rate, the device can work in three speed modes, single speed, double speed and quad speed. The device can detect the speed mode of the input data stream automatically when the sampling rate falls into the auto detection ranges listed in Table1. If the sampling rate is outside the auto detection ranges, the device will not work properly.

MODE	Fs Auto Detection Range	CLKIN/LRCK Ratio
Single Speed	8kHz – 50kHz	256, 384, 512, 768, 1024
Double Speed	84kHz – 100kHz	128, 192, 256, 384, 512
Quad Speed	167kHz – 200kHz	128, 192, 256

The device works with the input system clock CLKIN, sample data clock LRCK and bit clock SCLK. The data clock and bit clock must be synchronously derived from the system clock with some specific rates. The device only supports the CLKIN/LRCK ratios listed in Table1. The LRCK/SCLK ratio is normally 64. The device detects clock ratios automatically, and it will not work properly if any ratio is incorrect.

Audio Data Input

The PA5134LV can accept I²S serial audio input data from 16-bit to 24-bit. The device can detect the data word length automatically. The relationship of SDATA, SCLK and LRCK for the format is illustrated through Figures 2.

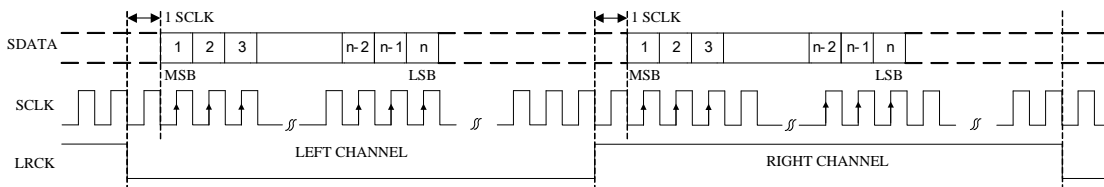


Figure 2. I²S Serial Audio Data Format up to 24-bit

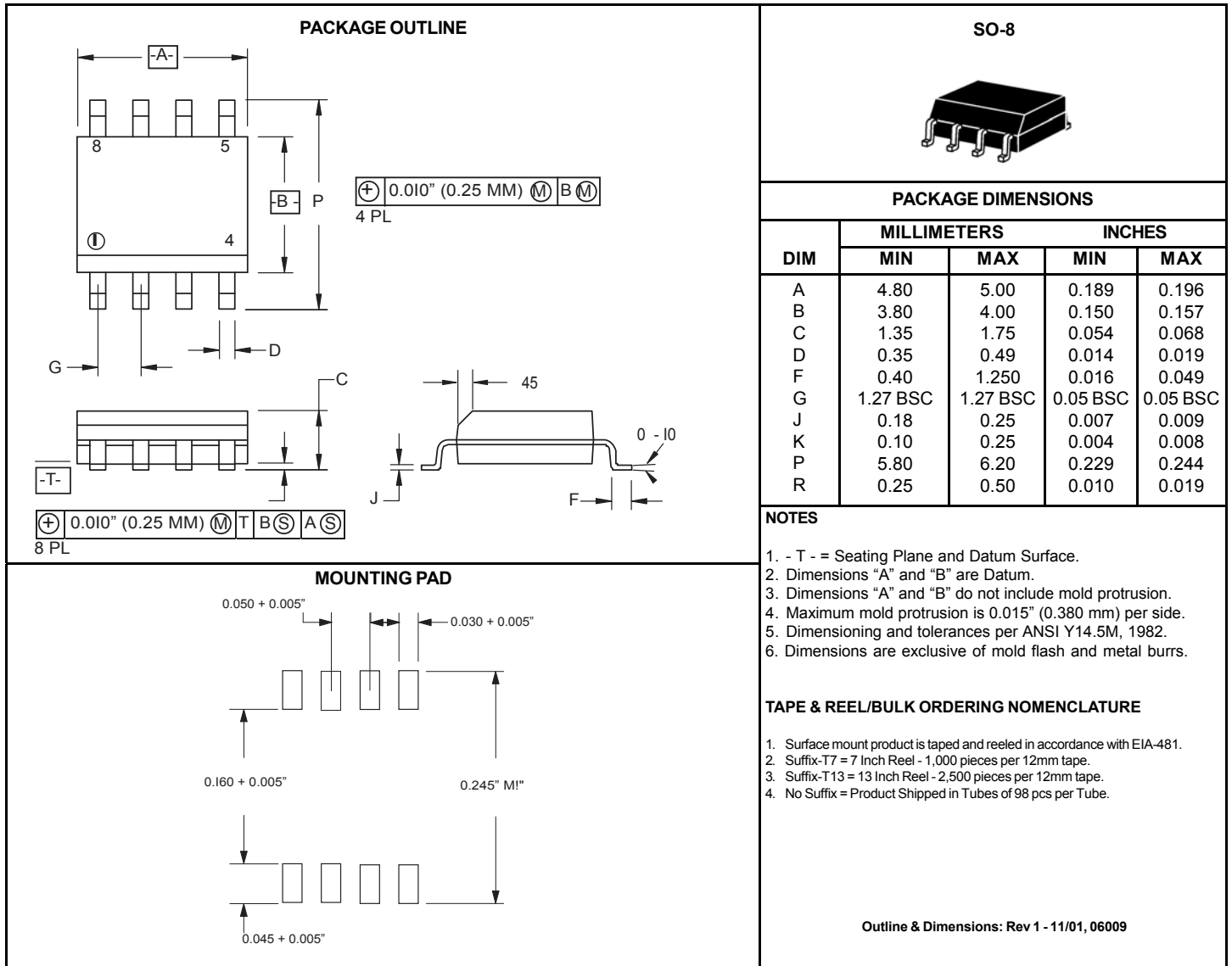


Power Up and Power Down

Upon applying VDD, the device will reset itself and enter power down state. During this state, the device clamps outputs to ground and power down the device operation except for clock management unit.

Once proper CLKIN and LRCK clocks are applied, the device will leave power down state, and the device outputs ramp from ground to common mode voltage softly.

Then the device enters the normal operation.

PACKAGE DIMENSIONS AND MEASUREMENTS

Life Support Policy

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