

FEATURES

- 16-channel constant-current output.
- Output constant current: 2 - 80mA
- Current accuracy (All output ON)
- Between BITS $\pm 1\%$
- Between IC's $\pm 1\%$
- Output Current 2~80mA adjustable
- Output current adjustable through an external resistor.
- Interleave time delay of output channel
- Fast response for output port ($t_r/t_d=50ns$)
- 25MHz clock frequency

DESCRIPTION

PA5026 contains a serial buffer and data latches which convert serial input data into parallel output format. At PA5026 output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LED's within a large range of V_f variations.

PA5026 provides users with great flexibility and device performance in their system design for LED display applications, e.g. LED panels.

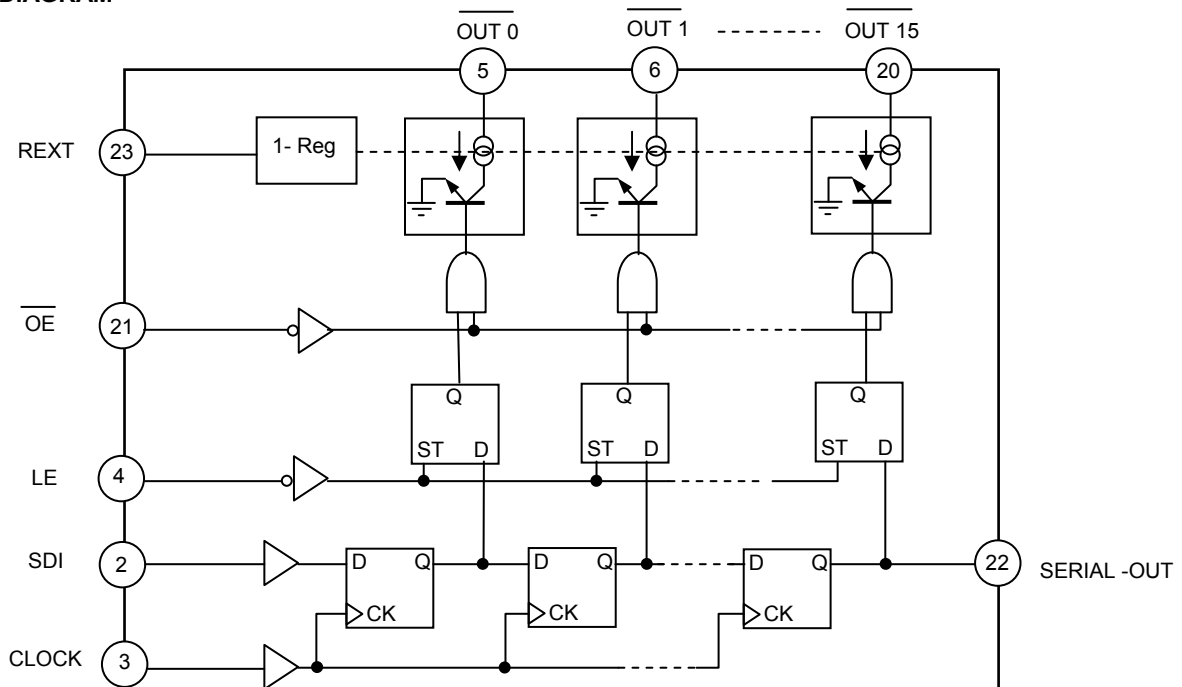
Users may adjust the output current from 2 mA to 80 mA through an external resistor, R_{ext} , which gives them the flexibility in controlling the light intensity of LED's.

PA5026 guarantees a maximum of 17V at the output port.

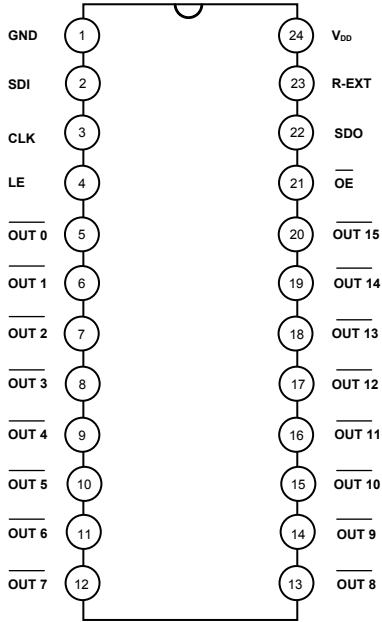
The high clock frequency, 25 MHz, satisfies the system requirements of high volume data transmission.

ORDERING INFORMATION

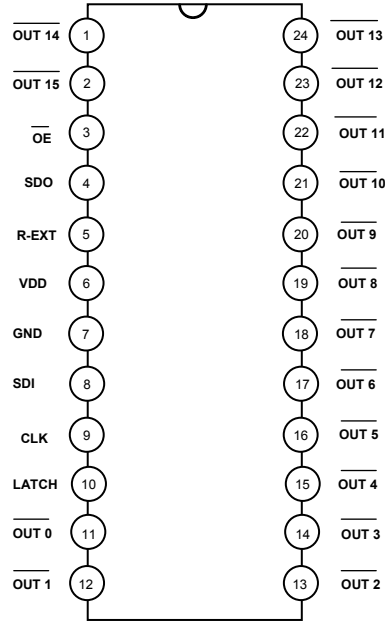
Device No.	Package
PA5026P	SSOP-24-300-1.0
PA5026S PA5026R	SSOP-24-150-0.635
PA5026QN	QFN-24

BLOCK DIAGRAM


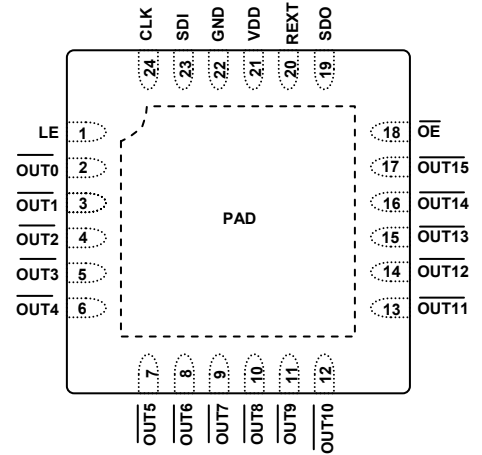
PIN CONFIGURATIONS



PA5026P (SSOP-24-300-1.0)
AND
PA5026R (SSOP-24-150-0.635)



PA5026S (SSOP-24-150-0.635)

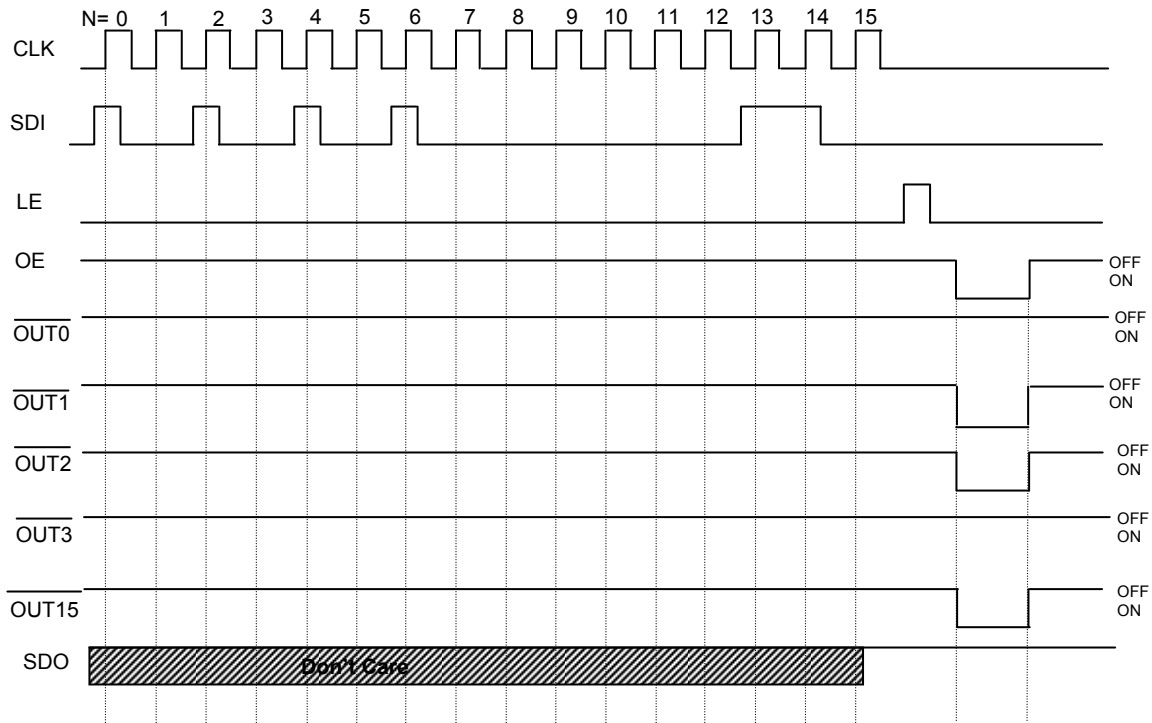


PA5026QN (QFN-24)






PIN DESCRIPTIONS

Pin Number			Pin Name	Description
PA5026QN	PA5026P PA5026R	PA5026S		
22	1	7	GND	Ground
23	2	8	SDI	Shift register Data Input Pin
24	3	9	CLK	Shift Register Clock Input Pin,
1	4	10	LATCH ENABLE	Data Strobe Input Pin,
2~9	5~12	11~18	$\overline{\text{OUT0}}\sim\overline{\text{OUT7}}$	Output Port
10~15	13~18	19~24	$\overline{\text{OUT8}}\sim\overline{\text{OUT13}}$	
16~17	19~20	1~2	$\overline{\text{OUT14}}\sim\overline{\text{OUT15}}$	
18	21	3	$\overline{\text{OE}}$	Output Enable
19	22	4	SDO	Shift Register Data Output Pin
20	23	5	R-EXT	External Resistor Input Port
21	24	6	V _{DD}	Power Supply

TIMING DIAGRAM



TRUTH TABLE

CLK	LE	OE	SDI	$\overline{\text{OUT0}} \dots \overline{\text{OUT7}} \dots \overline{\text{OUT15}}$	SDO
	H	L	D_N	$\overline{D_N} \dots \overline{D_{N-7}} \dots \overline{D_{N-15}}$	D_{N-15}
	L	L	D_{N+1}	No Change	D_{N-14}
	H	L	D_{N+2}	$\overline{D_N} \dots \overline{D_{N-5}} \dots \overline{D_{N-13}}$	D_{N-13}
	X	L	D_{N+3}	$\overline{D_N} \dots \overline{D_{N-5}} \dots \overline{D_{N-13}}$	D_{N-13}
	X	H	D_{N+3}	Off	D_{N-13}

MAXIMUM RATINGS

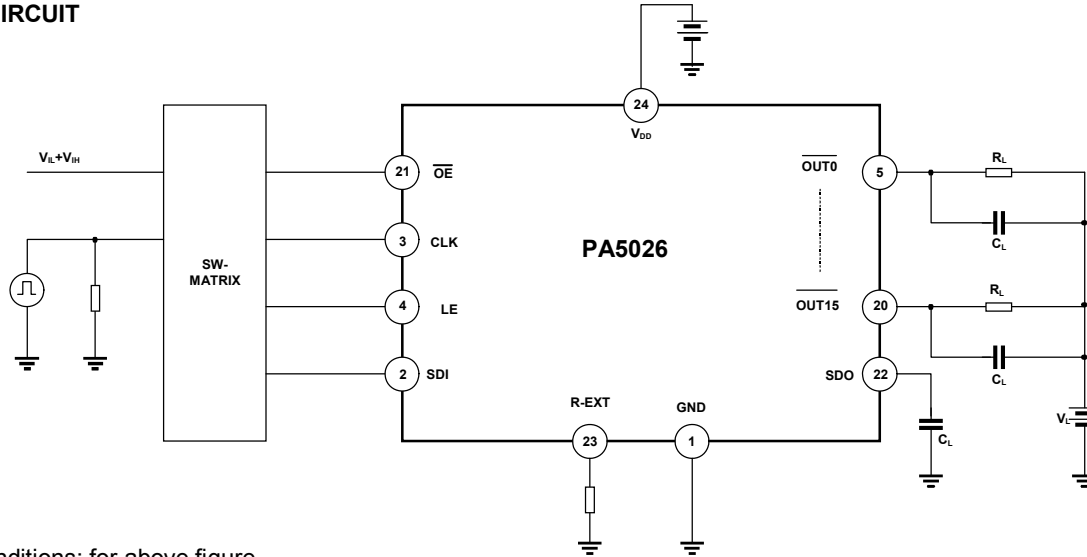
Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7.0	V
Input Voltage		V_{IN}	-0.4~ V_{DD} + 0.4	V
Output Current		I_{OUT}	+90	mA
Output Voltage		V_{DS}	-0.5~+17.0	V
Clock Frequency		F_{CLK}	25	MHz
GND Terminal Current		I_{GND}	1440	mA
Power Dissipation (On PCB, $T_a=25^\circ\text{C}$)	CN – type	P_D	2.32	W
	CNS – type		1.87	
	CD – type		2.51	
	CF – type		2.12	
	CP – type		1.73	
	CPA – type		1.73	
Thermal Resistance (On PCB, $T_a=25^\circ\text{C}$)	CN – type	$R_{th(j-a)}$	53.82	$^\circ\text{C/W}$
	CNS – type		66.74	
	CD – type		49.81	
	CF – type		59.01	
	CP – type		72.43	
	CPA – type		72.43	
Operating Temperature		T_{opr}	-40~+85	$^\circ\text{C}$
Storage Temperature		T_{stg}	-55~+150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-	2.5*	5.0	5.5	V
Output Voltage		V_{DS}	$\overline{OUT0} \sim \overline{OUT15}$	-	-	17.0	V
Output Current		I_{OUT}	DC Test Circuit	2	-	80	mA
		I_{OH}	SDO	-	-	-1.0	mA
		I_{OL}	SDO	-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	$T_a = -40 \sim 85^\circ C$	0.8VDD	-	VDD	V
	"L" level	V_{IL}	$T_a = -40 \sim 85^\circ C$	GND	-	0.3VDD	V
Output Leakage Current		I_{OH}	$V_{OH}=17.0V$	-	-	0.5	μA
Output Voltage	SDO	V_{OL}	$I_{OL}=+1.0mA$	-	-	0.4	V
		V_{OH}	$I_{OH}=-1.0mA$	4.6	-	-	V
Output Current 1		I_{OUT1}	$V_{DS}=0.6V$ $R_{ext}=720 \Omega$	-	26.25	-	mA
Current Skew		dI_{OUT1}	$I_{OL}=26.25mA$ $V_{DS}=0.6V$ $R_{ext}=720 \Omega$	-	± 1	± 3	%
Output Current 2		I_{OUT2}	$V_{DS}=0.8V$ $R_{ext}=360 \Omega$	-	52.5	-	mA
Current Skew		dI_{OUT2}	$I_{OL}=52.5mA$ $V_{DS}=0.8V$ $R_{ext}=360 \Omega$	-	± 1	± 3	%
Output Current vs. Output Voltage Regulation		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V	-	± 0.1	-	% / V
Output Current vs. Supply Voltage Regulation		$\%/dV_{DD}$	V_{DD} within 4.5V and 5.5V	-	± 1	-	% / V
Pull-up Resistor		$R_{IN(up)}$	\overline{OE}	250	500	800	K Ω
Pull-down Resistor		$R_{IN(down)}$	LE	250	500	800	K Ω
Supply Current	"OFF"	$I_{DD(off) 1}$	$R_{ext}=\text{Open}, \overline{OUT0} \sim \overline{OUT15} =\text{Off}$	-	7	12	mA
		$I_{DD(off) 2}$	$R_{ext}=720 \Omega, \overline{OUT0} \sim \overline{OUT15} =\text{Off}$	-	10	12	
		$I_{DD(off) 3}$	$R_{ext}=360 \Omega, \overline{OUT0} \sim \overline{OUT15} =\text{Off}$	-	12	15	
	"ON"	$I_{DD(on) 1}$	$R_{ext}=720 \Omega, \overline{OUT0} \sim \overline{OUT15} =\text{On}$	-	10	18	
		$I_{DD(on) 2}$	$R_{ext}=360 \Omega, \overline{OUT0} \sim \overline{OUT15} =\text{On}$	-	12	20	

* 2.5V min for RED LED only Green and Blue LED require up to 4.0V

TEST CIRCUIT



Test conditions: for above figure

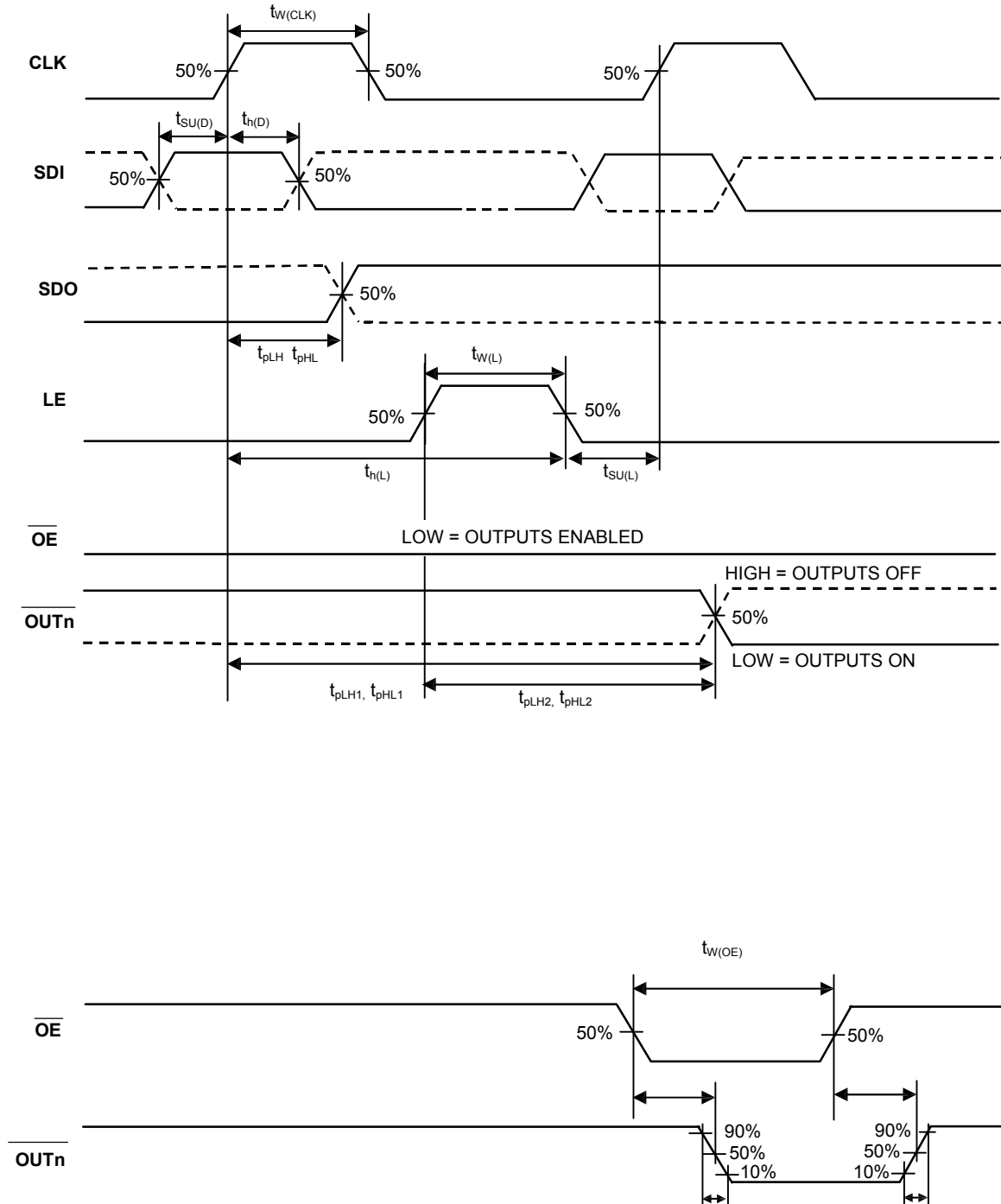
$T_{amb}=25^{\circ}C, V_{DD}=V_{IH}=3.3V$ and $5V, V_{OUT}=0.7V, V_{IL}=0V, R_{EXT}=490\Omega, V_L=3.0V, R_L=60\Omega, C_L=10.5pF$

SWITCHING CHARACTERISTICS

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	CLK - OUTn	t_{pLH1}	$V_{DD}=5.0 V$ $V_{DS}=0.8 V$ $V_{IH}=V_{DD}$ $V_{IL}=GND$ $R_{ext}=300 \Omega$ $V_L=4.0 V$ $R_L=52 \Omega$ $C_L=10 pF$	-	100	150	ns
	LE - OUTn	t_{pLH2}		-	100	150	ns
	OE - OUTn	t_{pLH3}		-	50	150	ns
	CLK - SDO	t_{pL}		15	20	-	ns
Propagation Delay Time ("H" to "L")	CLK - OUTn	t_{pHL1}		-	50	100	ns
	LE - OUTn	t_{pHL2}		-	50	100	ns
	OE - OUTn	t_{pHL3}		-	20	100	ns
	CLK - SDO	t_{pHL}		15	20	-	ns
Pulse Width	CLK	$t_w(CLK)$		20	-	-	ns
	LE	$t_w(L)$		20	-	-	ns
	OE	$t_w(OE)$	200	-	-	ns	
Hold Time for LE		$t_h(L)$	5	-	-	ns	
Setup Time for LE		$t_{su}(L)$	5	-	-	ns	
Hold Time for SDI		$t_h(D)$	10	-	-	ns	
Setup Time for SDI		$t_{su}(D)$	5	-	-	ns	
Clock Frequency		F _{CLK}	Cascade Operation	-	-	25.0	MHz
Maximum CLK Rise Time		t_r^{**}	-	-	500	ns	
Maximum CLK Fall Time		t_f^{**}	-	-	500	ns	
Output Rise Time of Vout (turn off)		t_{or}	-	70	200	ns	

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Output Fall Time of Vout (turn on)	t_{of}		-	40	120	ns
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TIMING WAVEFORM


APPLICATION NOTE

In LED applications, the PA5026 can maintain the current with almost no variation, across different channels and chips. The maximum current accuracy between bits is $\pm 3\%$, and between chips is $\pm 6\%$.

There is only one ground pin for signal ground, constant current source ground and power ground.

We recommend adopting minimum inductance in layout to reduce the switch noise and chip faults. In order to prevent driver damage by over current, do not turn off the driver and scan the triode at the same time.

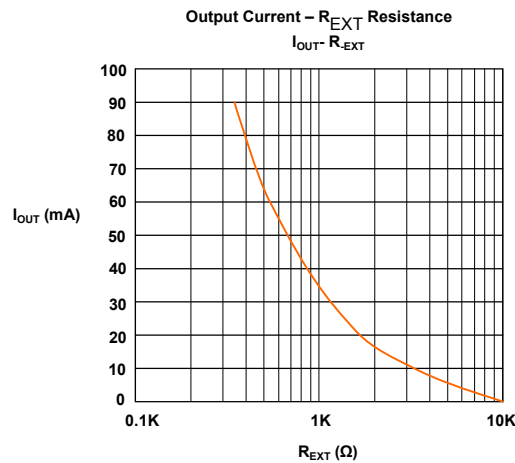
The resistor should be placed near the R-EXT pin.

The output current of each channel (I_{OUT}) is set by an external resistor, R_{EXT} .

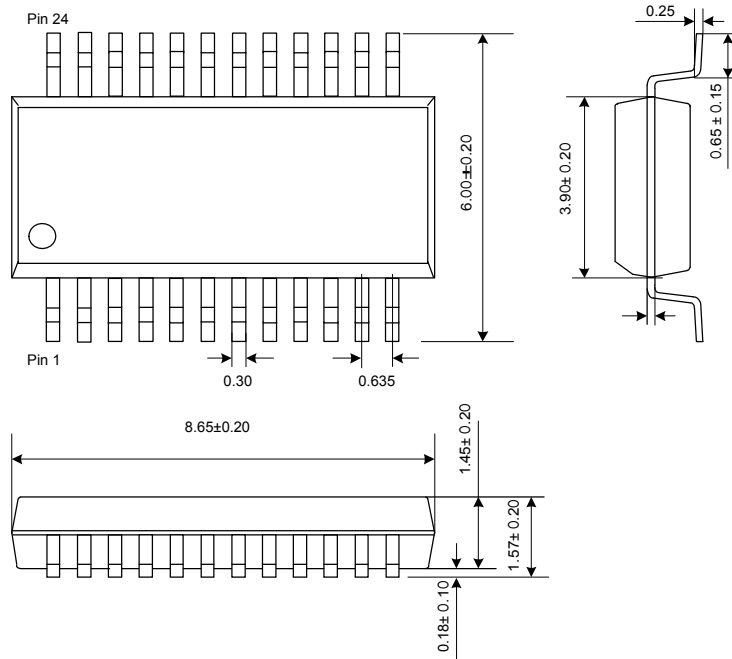
The output current can be calculated from the equation: $V_{R-EXT} = 1.26V$; $I_{OUT} = (V_{R-EXT} / R_{EXT}) \times 15$ where R_{EXT} is the resistance of the external resistor connected to R_{EXT} terminal and V_{R-EXT} is the voltage of R_{EXT} terminal.

The magnitude of current (as a function of R_{EXT}) is around 52.5mA at 360Ω and 26.25mA at 720Ω.

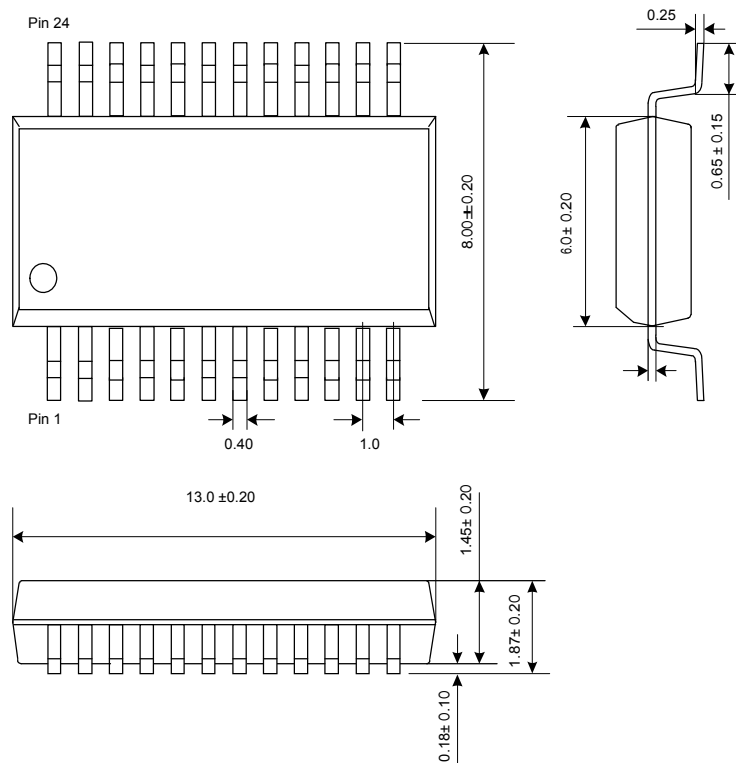
ELECTRICAL CHARACTERISTIC CURVE

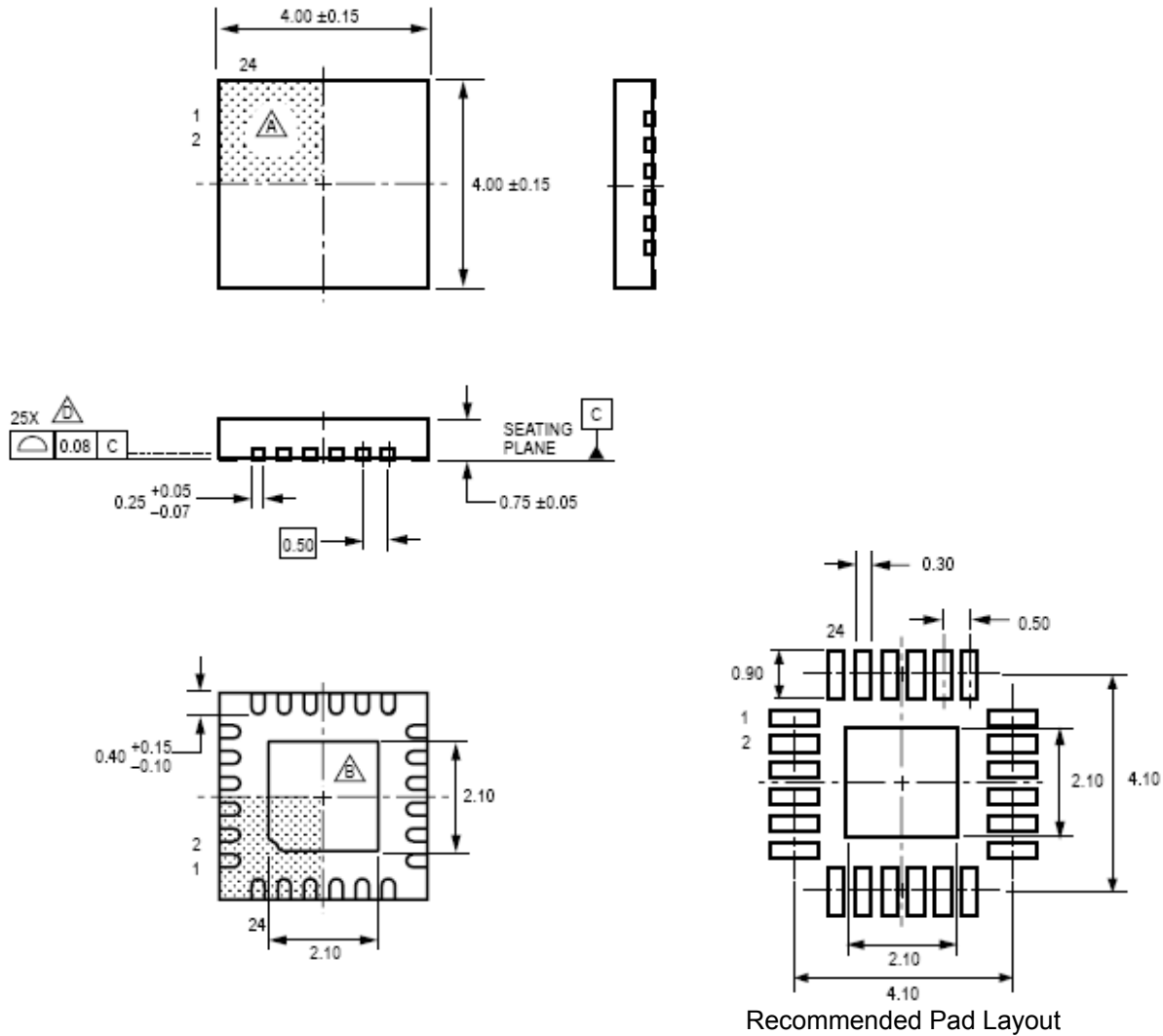


PACKAGE OUTLINE AND DIMENSIONS (*Measurements shown in mm*)
SSOP-24-150-0.635 FOR PA5026S AND THE PA5026R



PACKAGE OUTLINE AND DIMENSIONS
SSOP-24-300- 1.00 FOR PA5026P



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PACKAGE OUTLINE AND DIMENSIONS
QFN-24 FOR PA5026QN

Recommended Pad Layout
Tape and Reel Specifications

Reel Dia	A0	B0	K0	D	E	F	W	P0	P2	P	t-max
178 (7")	4.10 ± 0.10	4.10 ± 0.10	0.85 ± 0.10	1.50 ± 0.10	1.75 ± 0.10	3.50 ± 0.05	12.00 ± 0.30	4.00 ± 0.10	2.00 ± 0.05	4.00 ± 0.10	0.25

